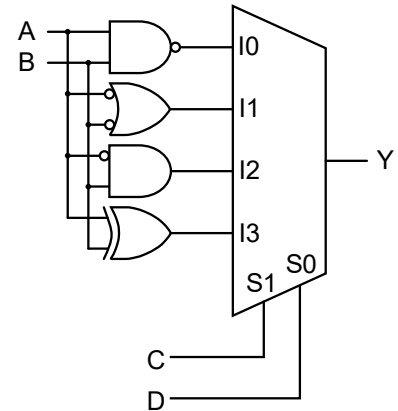Hand-write Verilog code for the following problems.

1. (8 points) Complete Verilog code for a multiplexor-based circuit that performs according to the circuit sketch below.

```verilog
module P1 (
    input A, B, C, D,
    output Y);


assign Y =


endmodule
```
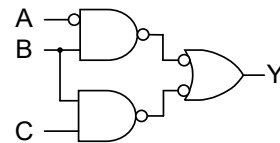

2. (8 points) Compete Verilog code to define a circuit that implements the minterm equation:
   $F = \Sigma m(0, 2, 4, 5, 6)$.

```verilog
module P2 (
    input
    output F);


assign F =




endmodule
```

3. (8 points) Compete Verilog code to define the circuit shown.

```verilog
module P3 (
    input A, B, C,
    output Y);


assign Y =




endmodule
```

4. (10 points) Compete Verilog code to define a 3:8 decoder. Include all required Verilog statements, including the "module" and "endmodule" statements.

5. (15 points) Complete Verilog code to define a circuit that can shift an 8-bit input data value "D" left or right by up to three bits as defined by the 2-bit "A" input, and drive an output bus "R" with the result (note: if A is '00', then the data simply passes through).

```
module P5 (
    input [7:0] D, LnR, [1:0] A,
    output [7:0] R);


assign Y =
```

```
    endmodule
```