Digital Systems Problem Set #2

Revision: August 5, 2025

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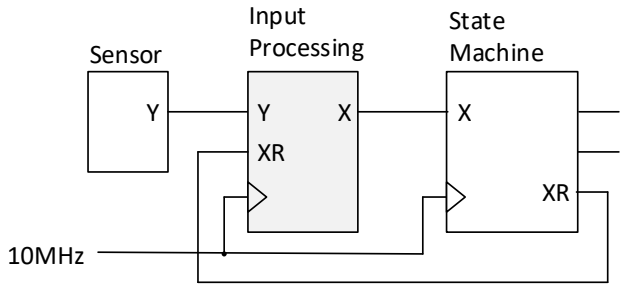
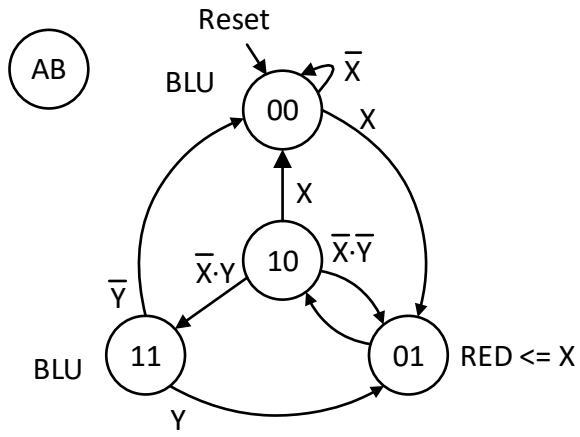
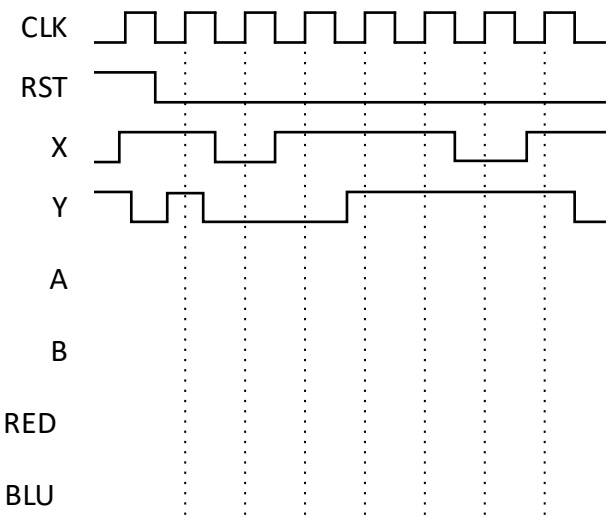
1. (6 points) A signal “Y” arising from a sensor can be asserted for an amount of time between 1us and 1ms. Design a state diagram for an input processing circuit that asserts an output signal “X” on the next rising edge of clock after Y has been received. X must remain asserted until after the input signal Y is no longer asserted, and until the feedback signal “XR” has been received to indicate the signal X has been processed by the state machine.



2. (10 points) After creating the previous state machine, you learned the sensor signal Y can bounce for up to 10us. Sketch a new state diagram for a circuit that can debounce the signal in addition to meeting the previous requirements.

3. (12 points) In the timing diagram below, show the time courses of the flip-flops (labeled A and B) and output signals defined by the state diagram. Then complete the following sentences.





Can RED suffer from a negative output race glitch? [Yes / No]
If you circled yes, on what transition? Leaving state ____ and going to state ____.

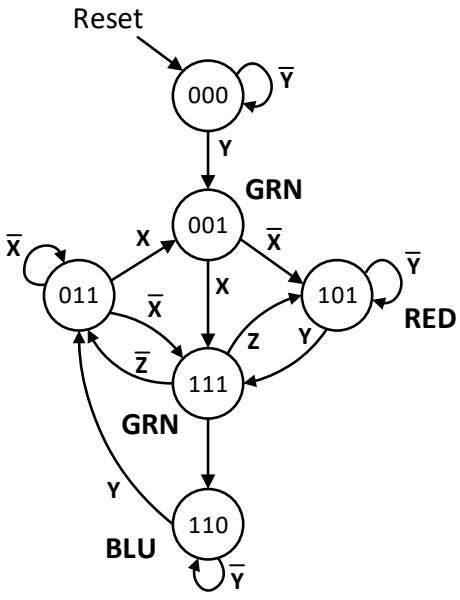
Can RED suffer from a positive output race glitch? [Yes / No]
If you circled yes, on what transition? Leaving state ____ and going to state ____.

Can BLUE suffer from a negative output race glitch? [Yes / No]
If you circled yes, on what transition? Leaving state ____ and going to state ____.

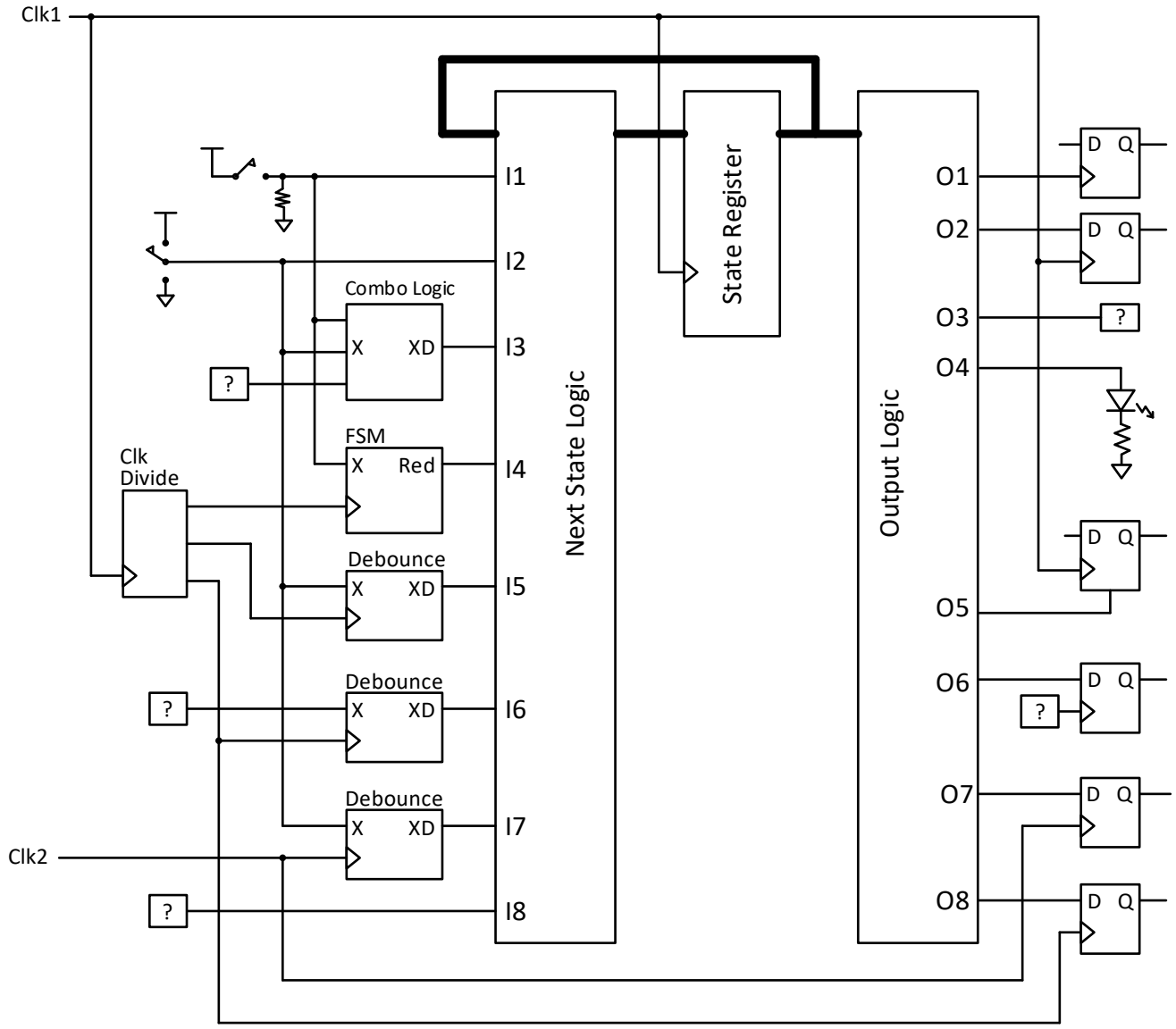
Can BLUE suffer from a positive output race glitch? [Yes / No]
If you circled yes, on what transition? Leaving state ____ and going to state ____.

4. (10 points) Complete the table below to document any possible output race glitches. One entry has been provided as an example. I didn't count the number of glitches that are possible, so don't read anything into the number of rows in the table.

Output	From State	To State	Pos. or Neg
GRN	001	111	Neg

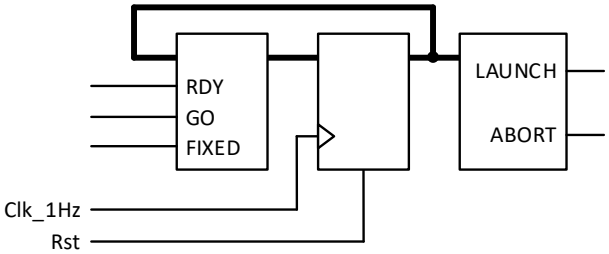


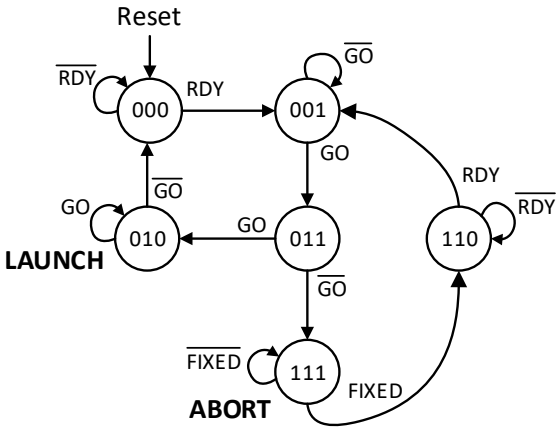
5. (20 points) Complete the table below by identifying the inputs and outputs that meet the described conditions.



These inputs are synchronous to the controller, and so do not need to use the go/no-go configuration	
These inputs may arrive at the controller with timing defects like bouncing or glitches	
These outputs should be free from glitches	
These outputs are in a different clock domain	

6. (12 points) A simple launch control system uses a slow clock (1Hz) and three pushbutton inputs GO, RDY and FIXED. After the system is ready (RDY), if GO is asserted for two consecutive clock cycles, the LAUNCH output is asserted. But if GO is de-asserted before the next consecutive clock, the launch ABORTs and the system waits for FIXED and then RDY again. Answer the following questions for the system.

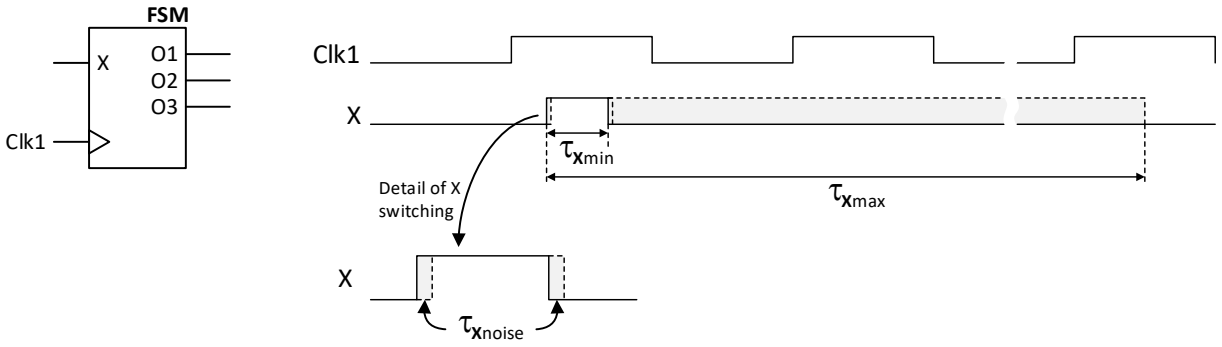




Could a launch still happen if GO is sampled high, but then transitions low before the second consecutive clock? Explain.

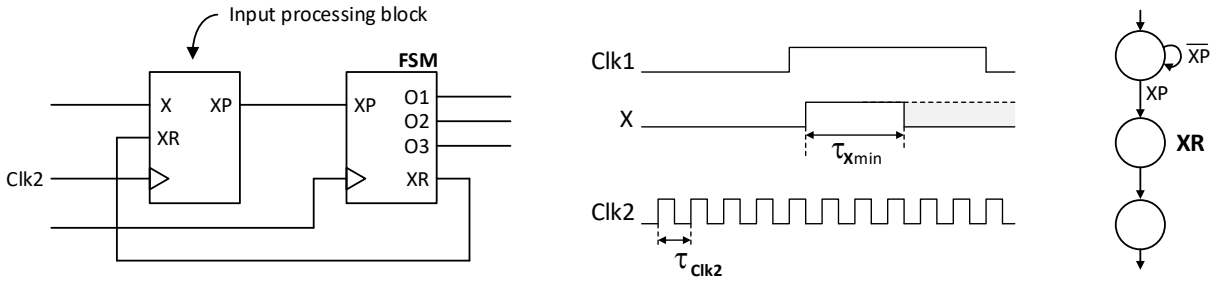
If there is a problem, discuss how it could be fixed – if you can think of more than one fix, mention both.

7. (20 points) You are tasked with designing a state machine that receives a single input X and clock signal Clk1, and produces three outputs O1, O2, and O3. The input X is from an unknown clock domain; it may bounce or have glitches for up to time τ_{Xnoise}; it may be asserted for a time τ_{Xmin} that is shorter than the Clk1 period; and it may be asserted for a time τ_{Xmax} that is indeterminate.



You decide to add an input processing block that uses a new clock (Clk2) that has a period less than τ_{Xmin} but greater than time τ_{Xnoise} (Clk2 can be used to sample X, because at least one rising edge will occur during the time X is asserted, and it will filter out the logic/switching noise). But because τ_{Xmax} isn't specified, there could be any number of rising edges on Clk2 during the time X is asserted.

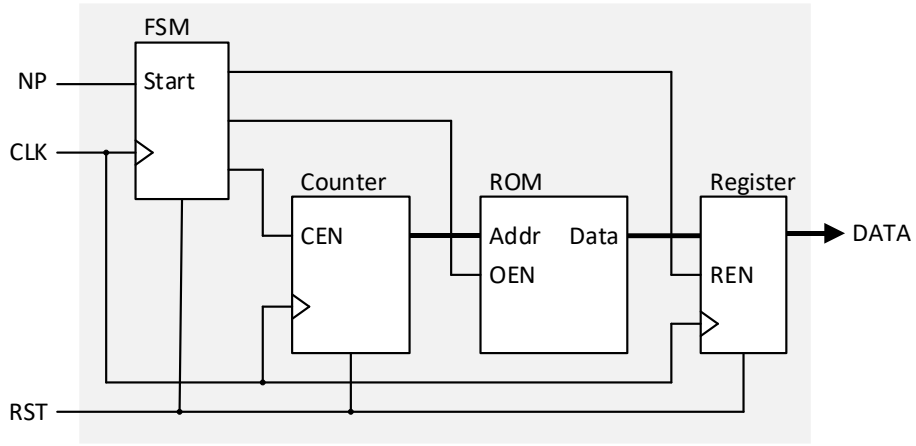
The signal XP should be asserted long enough to ensure the FSM receives it, and it should be de-asserted after the FSM has received it, so that the FSM only responds once for each assertion of X, regardless of how long it is asserted. To accommodate dealing with X appropriately, you decide to modify FSM by adding a feedback signal XR that will be asserted on the next rising edge of Clk1 after the "processed X" signal XP has been received.



(16 points) Sketch a state diagram for the input processing block that meets all the requirements.

(4 points) Can the output XR be generated as a Mealy/conditional output? Briefly explain your answer.

8. (15 points) A data system produces new data from a ROM in response to each assertion of the "Next Point" (NP) signal. NP is generated from another digital system in the same clock domain, and it is asserted for 5 to 10 clock periods every 100 – 200 clock periods. Your system should generate one new data point for assertion of NP, and drive that data point on the data bus until the next assertion of NP. Data points are generated from successive ROM addresses generated by a counter, with the first point coming from address 0. After an address is presented to the ROM, the ROM's OE signal must be driven for at least two clock periods to allow enough time for the ROM to drive it's output bus. Sketch a state diagram for the FSM block below that can drive the system as required. Choose state codes that will let your state machine run at the fastest possible clock speed.



Given your choice of state codes, can any of your outputs have timing defects (just yes or no)?

Given your choice of state codes, does your circuit need any output logic? If so, what outputs are driven by what logic functions?

9. (15 points) Sketch a state diagram for a traffic light controller that cycles continuously through RED (90s), YEL (3s), and GRN (90s). If the CAR input is asserted while GRN is being output, then after GRN has been asserted for at least 9s, output YEL for 3 seconds and re-enter the main cycle by asserting RED for 90 seconds. Assume you have access to a timer circuit that puts out phase-aligned 1us pulses on three separate signals every 3, 9, and 90 seconds.