

RFSoc 4X2 Gen3

Variant: Prototype

5/23/2024 V3I1

RELEASED

| Page | Index | Page | Index | Page | Index | Page | Index |
|------|--------------------|------|------------------------|------|------------------------|------|-----------------------------|
| 1 | COVER PAGE | 13 | ETHERNET 1Gbit | 25 | PL Banks 84, 87 | 37 | PWR I 0V85 |
| 2 | BLOCK DIAGRAM | 14 | QSFP | 26 | PL GTY | 38 | PWR II 1V8, 3V3 and GTY PWR |
| 3 | POWER DIAGRAM | 15 | CLOCK I | 27 | RF ADC | 39 | PWR III RF DC AND 5V0 |
| 4 | USER IO, LEDs | 16 | CLOCK II | 28 | RF DAC | 40 | PWR IV RF LDO |
| 5 | PMOD HEADERS | 17 | CLOCK III RF ADC CLOCK | 29 | RFSoc POWER PINS | 41 | PWR V DDR4 |
| 6 | SYZYGY HEADER | 18 | CLOCK IV RF DAC CLOCK | 30 | RFSoc DECOUPLING | 42 | PWR VI SYZYGY |
| 7 | USB-JTAG, USB-UART | 19 | RFSoc CONFIG | 31 | RFSoc GND PINS | 43 | CURRENT MONITOR |
| 8 | USB 3.0 SLAVE | 20 | PS 500-502 | 32 | DDR4 MEMORY PS I | 44 | SEQUENCER |
| 9 | USB 3.0 HOST | 21 | PS 504 | 33 | DDR4 MEMORY PS II | 45 | MECH AND PWR SEQUENCING |
| 10 | 1PPS | 22 | PS MGT | 34 | DDR4 MEMORY PL I | 46 | DOC REVISION HISTORY |
| 11 | DISPLAY PORT | 23 | PL Banks 64-66 | 35 | DDR4 MEMORY PL II | 47 | |
| 12 | SD CARD AND EEPROM | 24 | PL Banks 67-69 | 36 | PWR INPUT AND FAN CTRL | 48 | |

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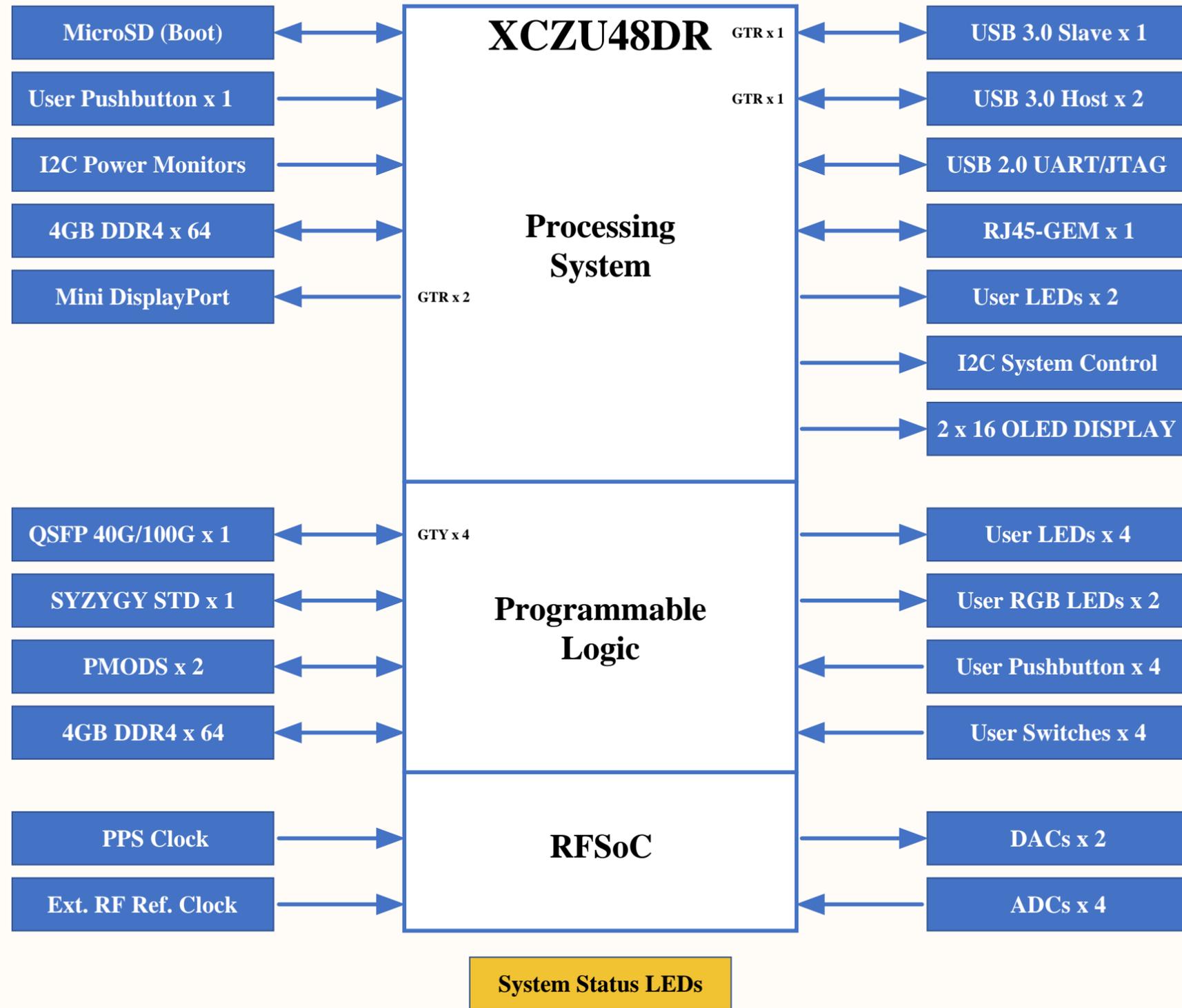
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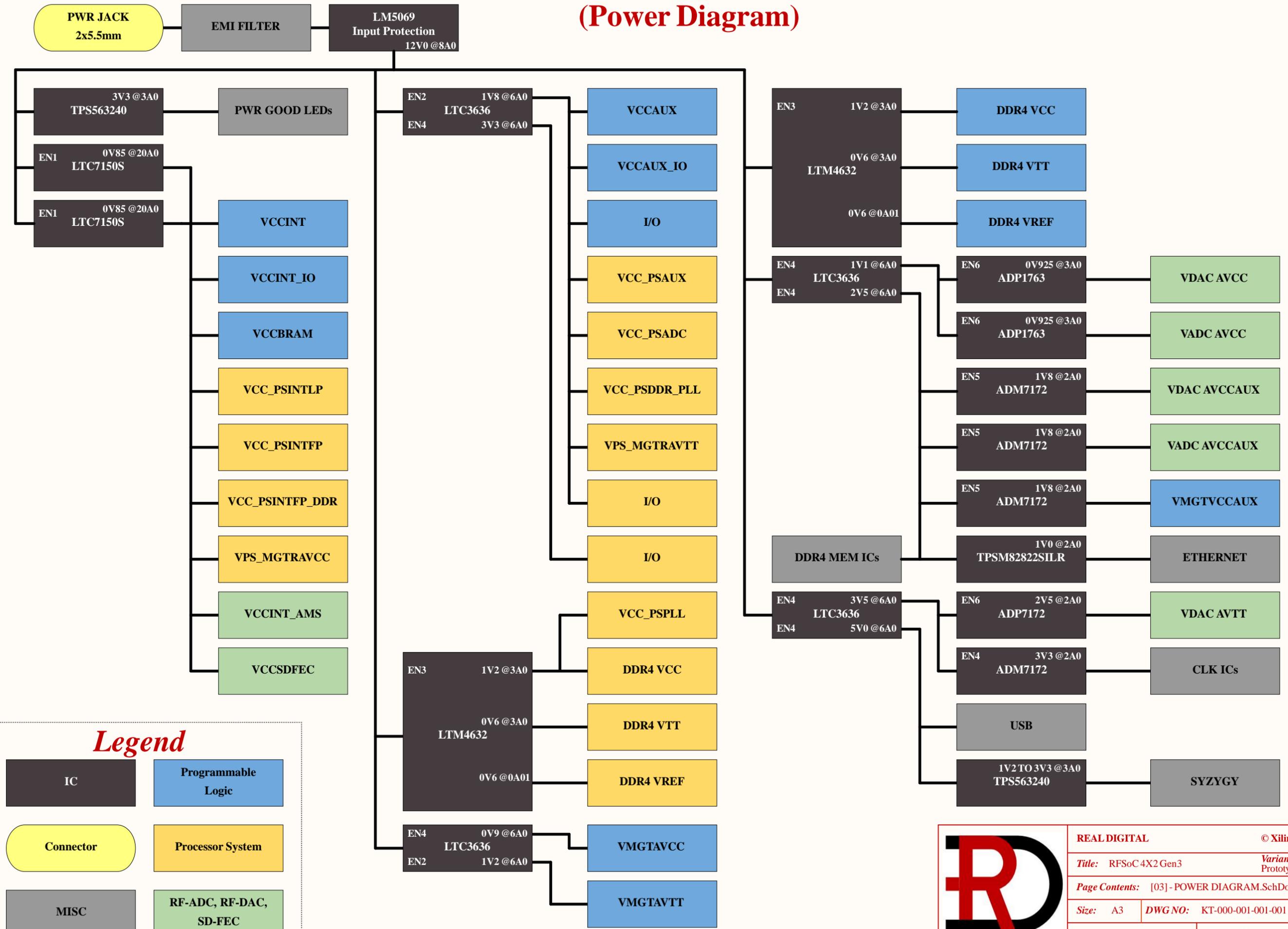
RFSoc 4X2 Gen3

(Block Diagram)



| | | | |
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| <i>Date:</i> 5/23/2024 | <i>Checked by:</i> * | <i>Sheet</i> 2 <i>of</i> 46 | |

RFSoc 4X2 Gen3 (Power Diagram)



Legend

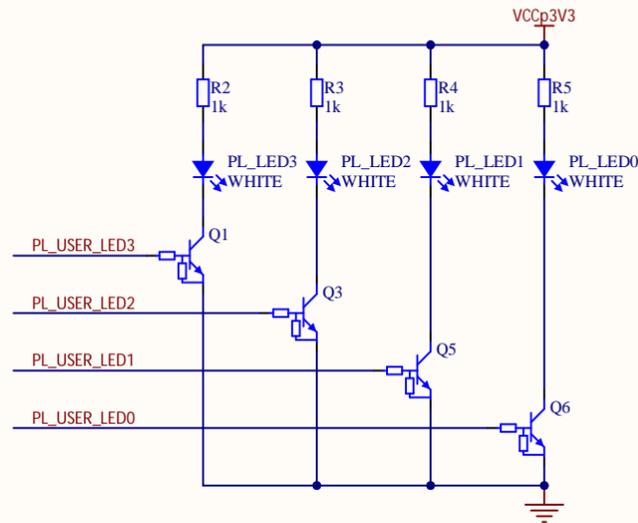
| | |
|-----------|------------------------|
| IC | Programmable Logic |
| Connector | Processor System |
| MISC | RF-ADC, RF-DAC, SD-FEC |



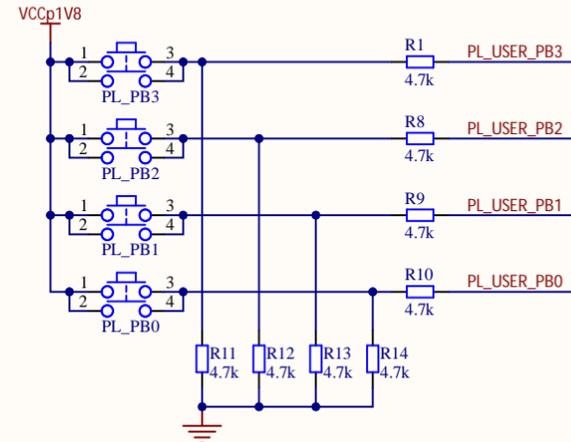
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USER IO, LEDs

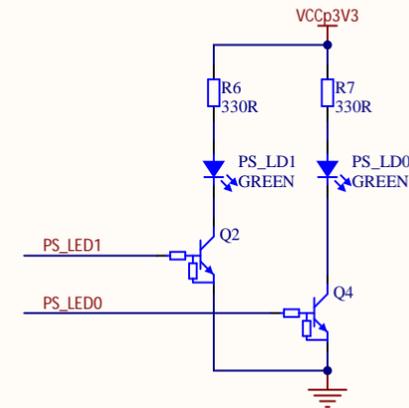
PL user-defined white LEDs



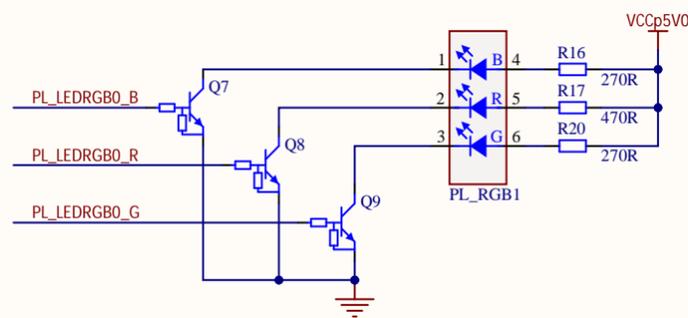
PL user-defined pushbuttons



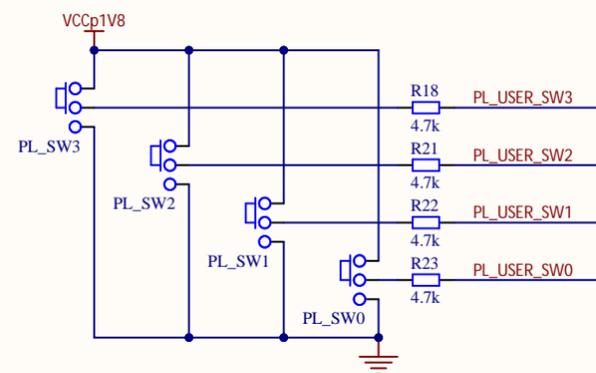
PS user-defined green LEDs



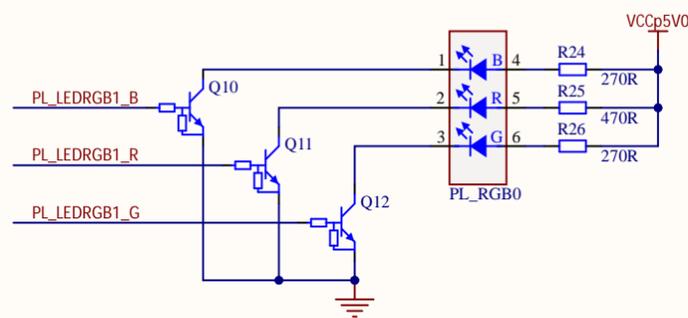
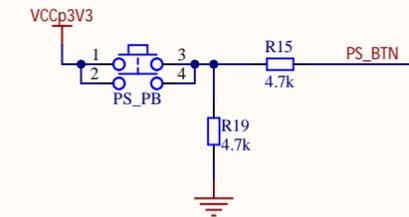
PL user-defined RGB LEDs



PL user-defined switches

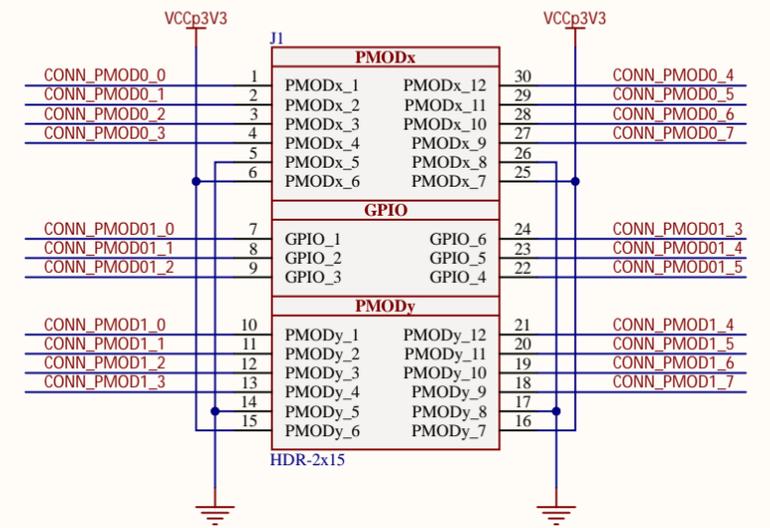
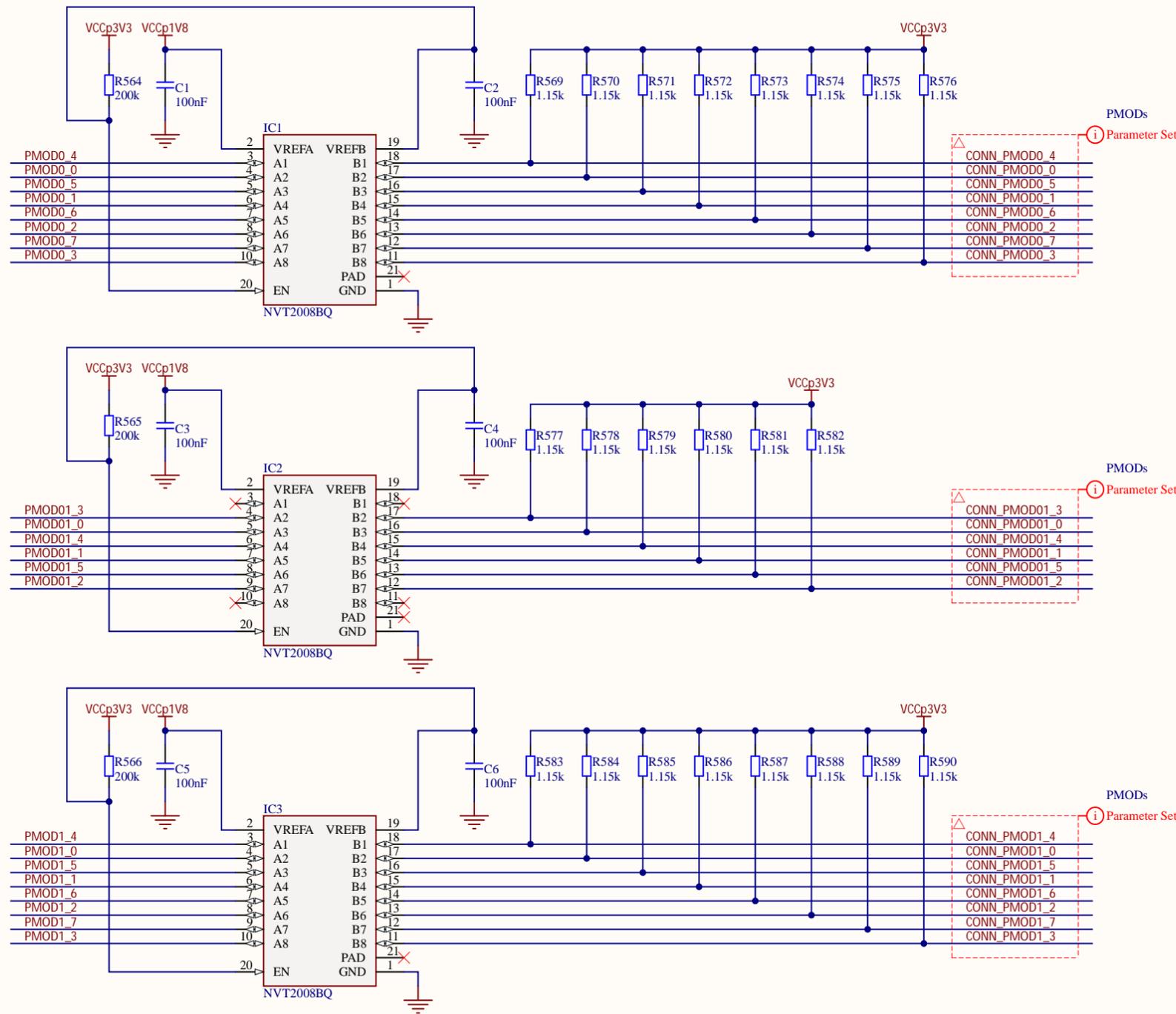


PS user-defined pushbutton



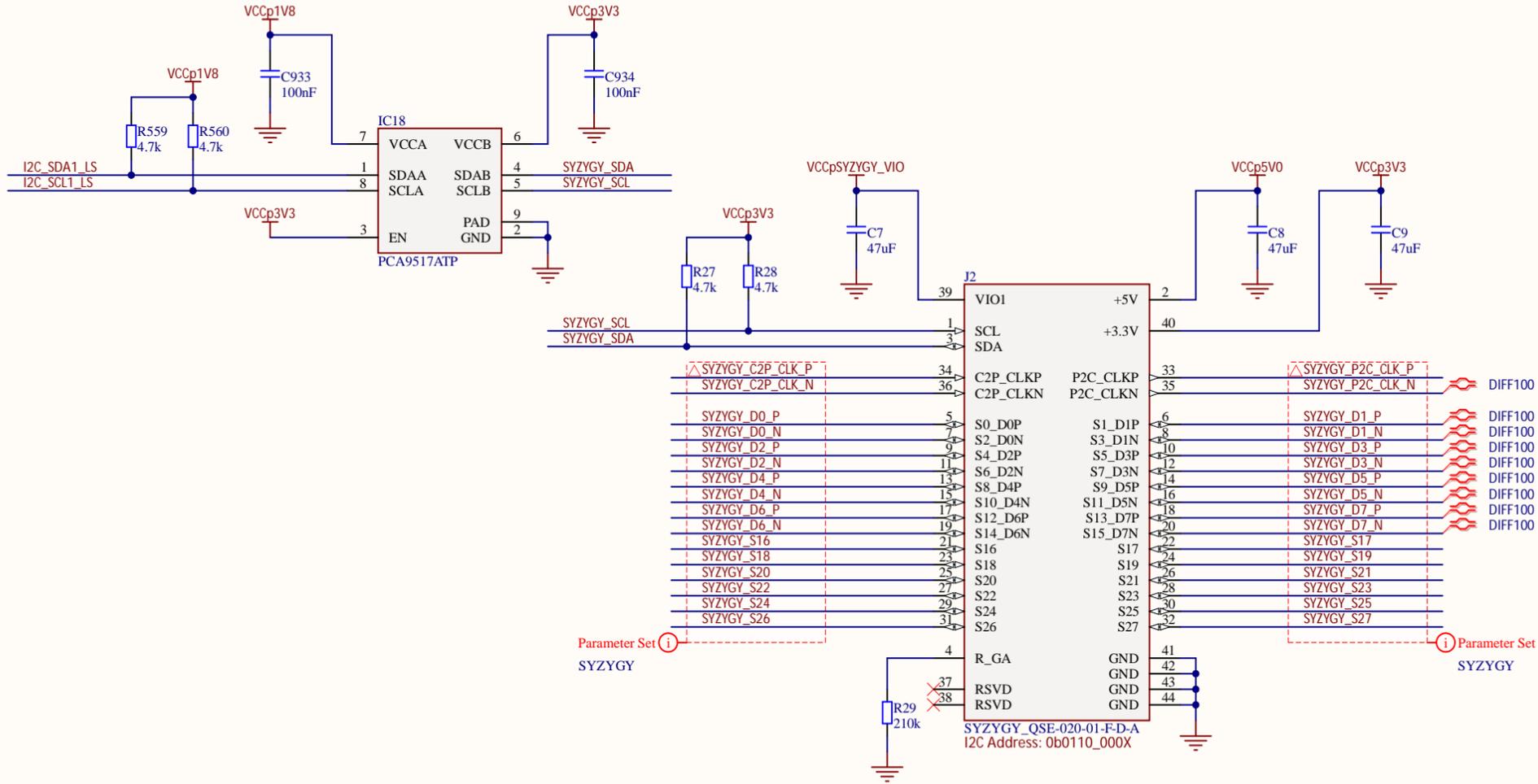
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PMOD HEADERS



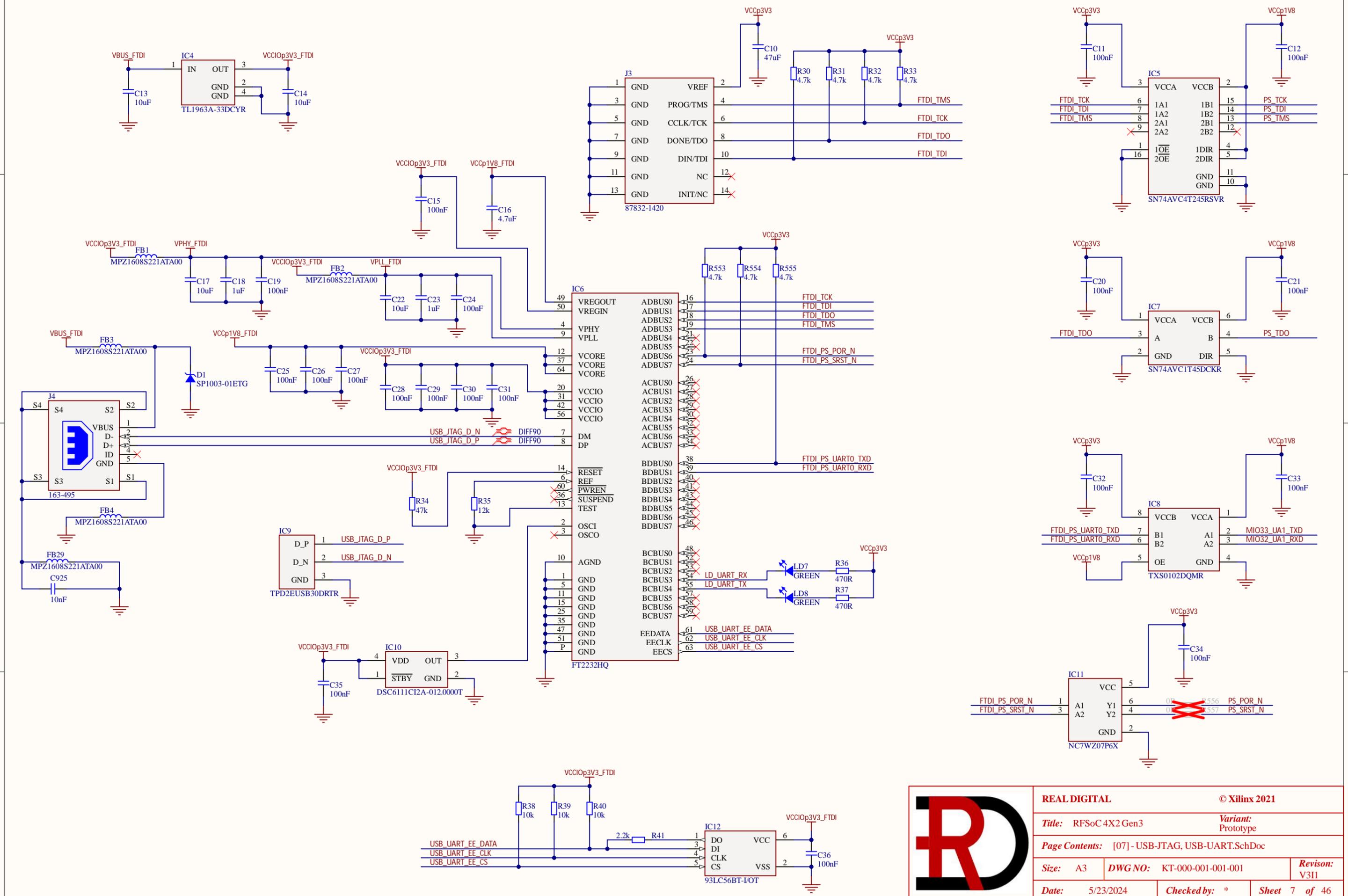
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SYZYGY HEADER



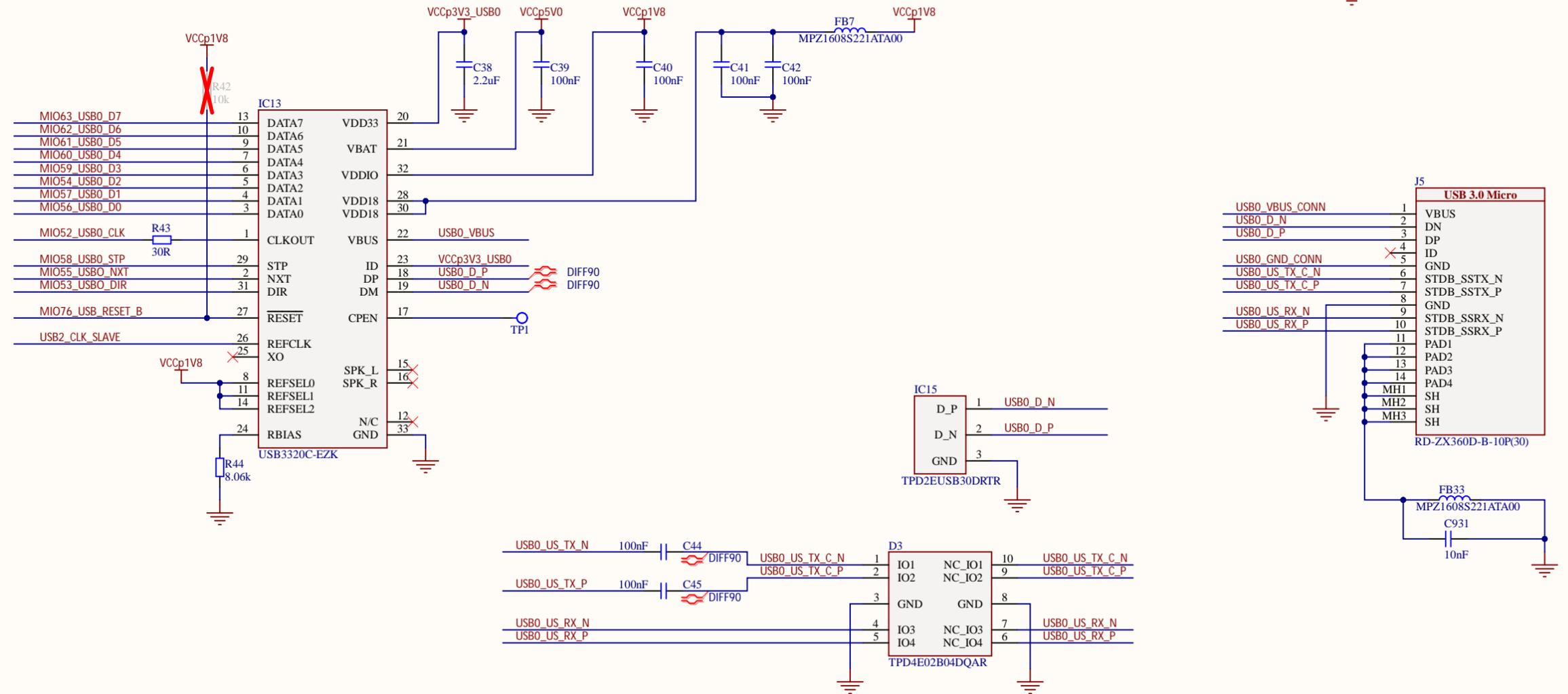
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USB-JTAG, USB-UART



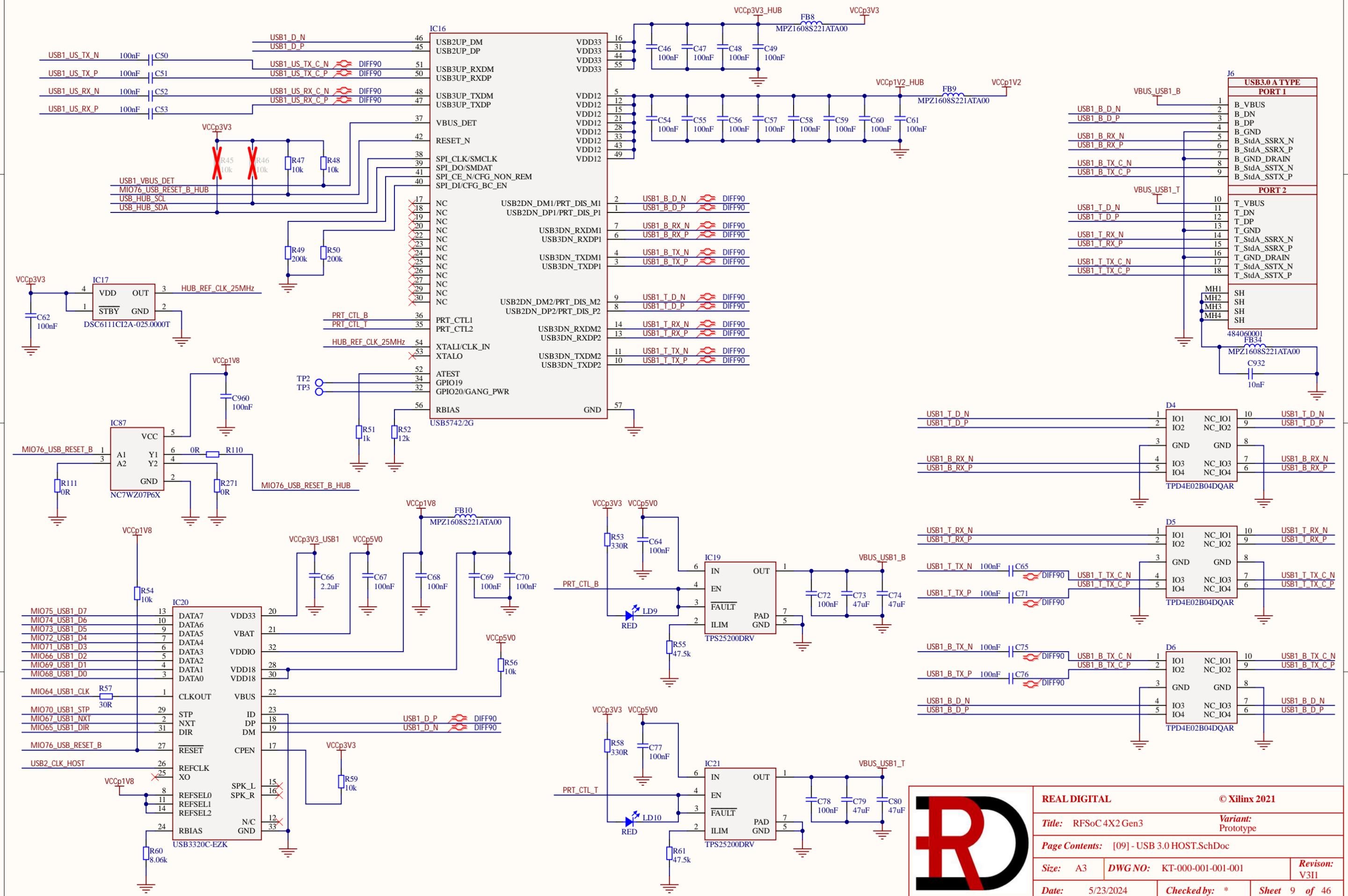
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| Date: 5/23/2024 | Checked by: * | Sheet 7 of 46 | |

USB 3.0 SLAVE



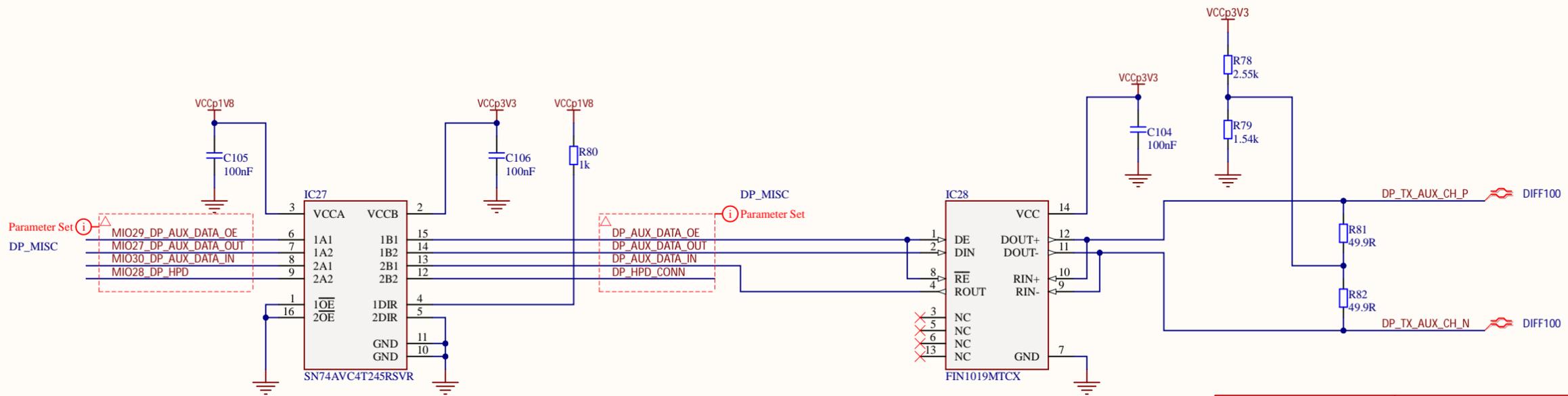
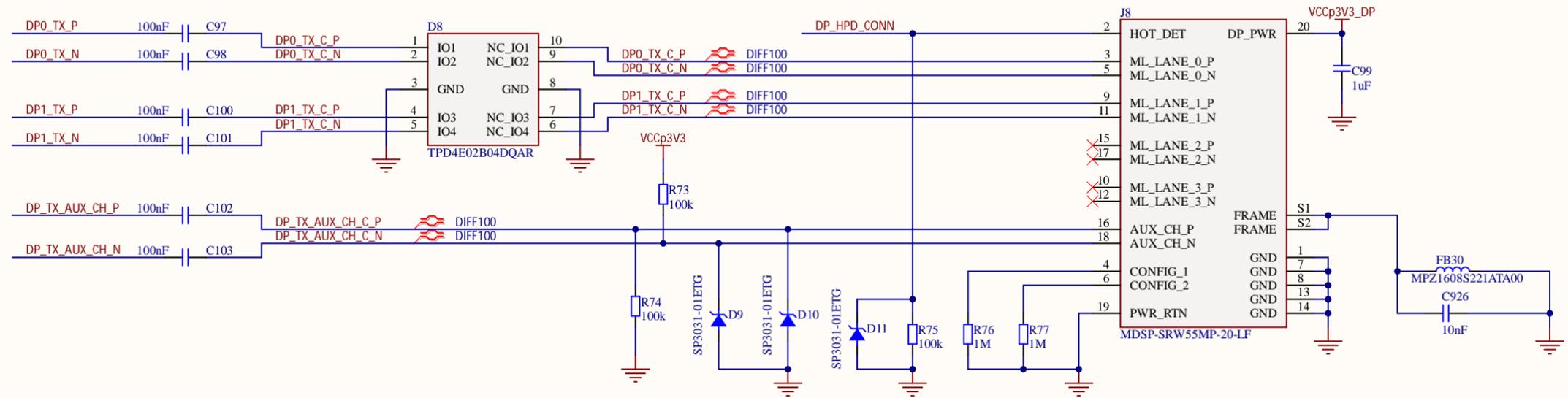
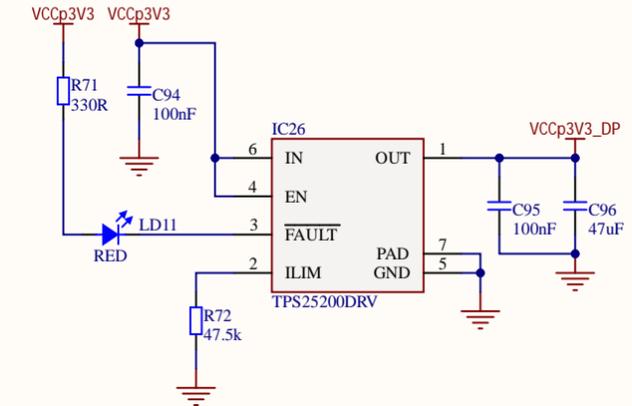
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USB 3.0 HOST



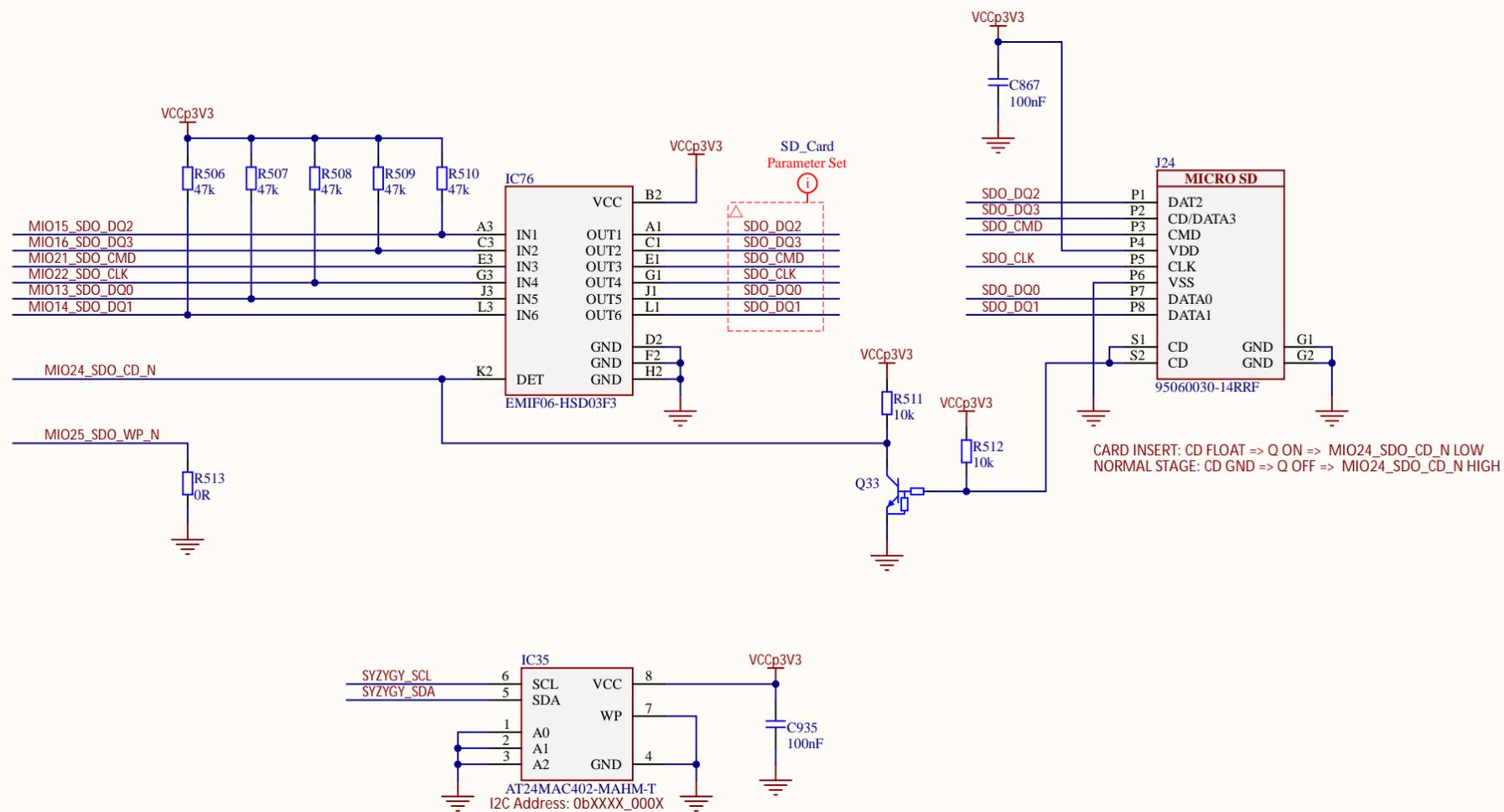
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DISPLAY PORT



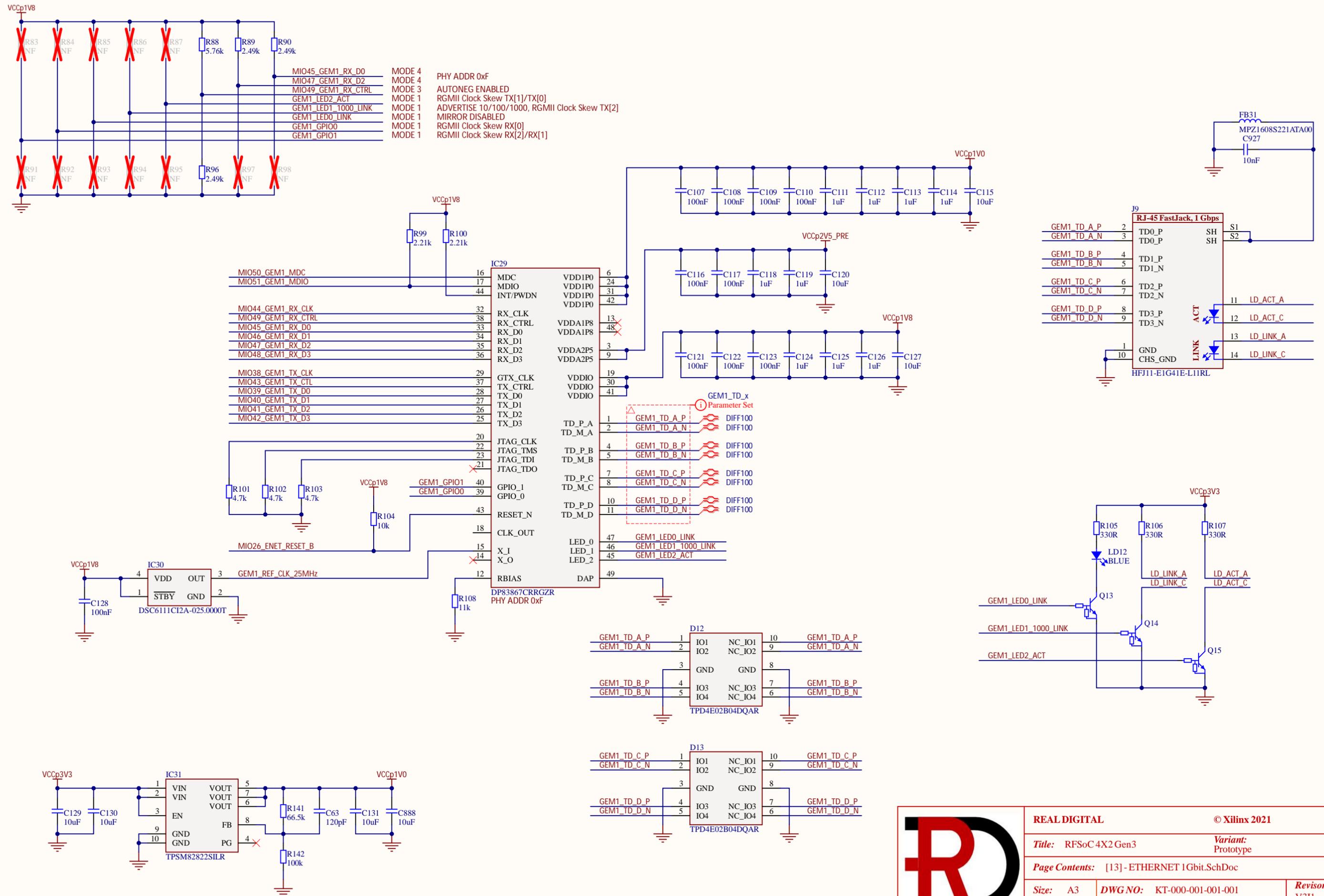
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SD CARD



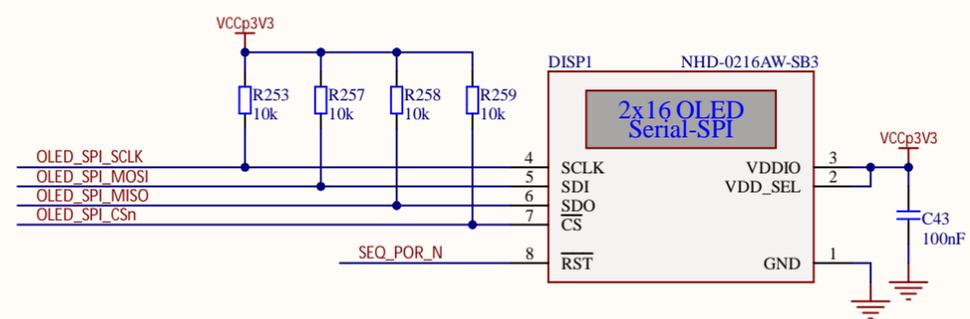
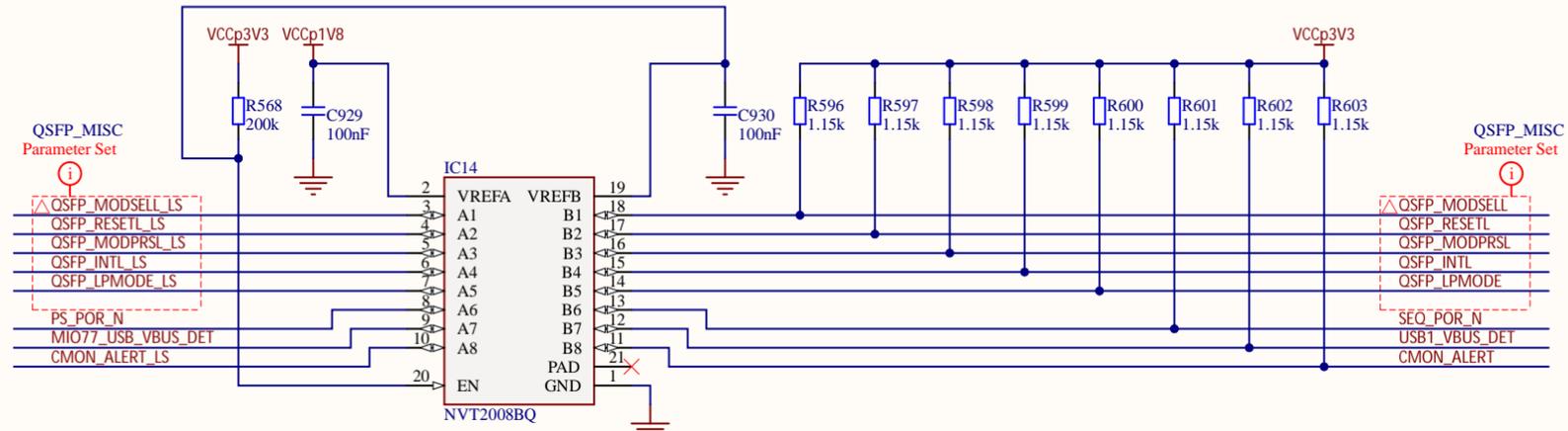
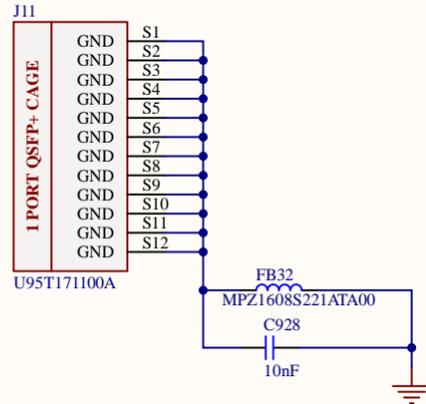
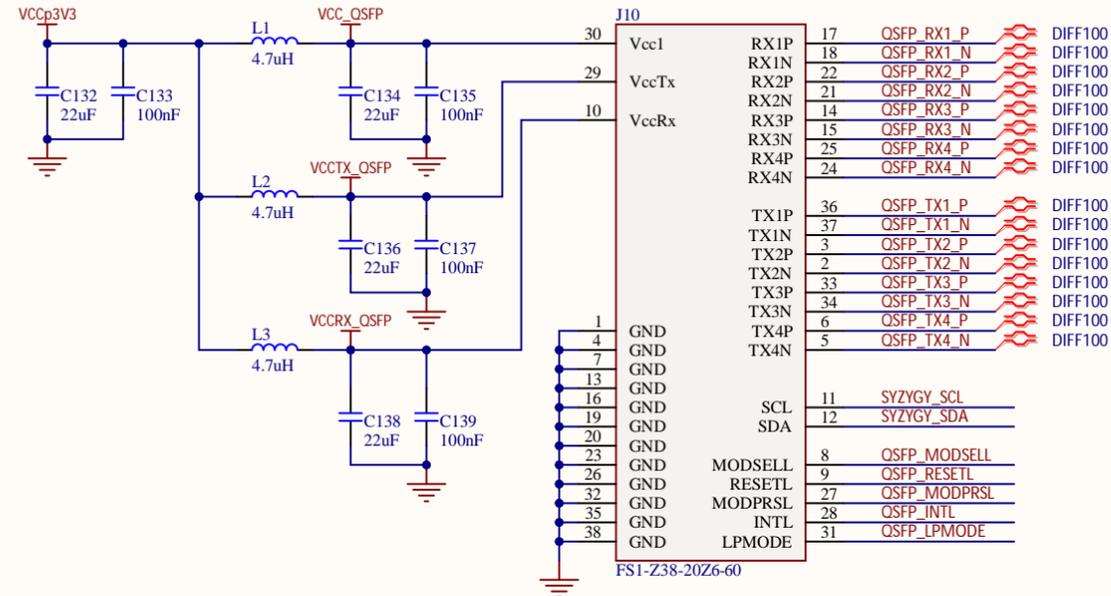
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ETHERNET 1Gbit

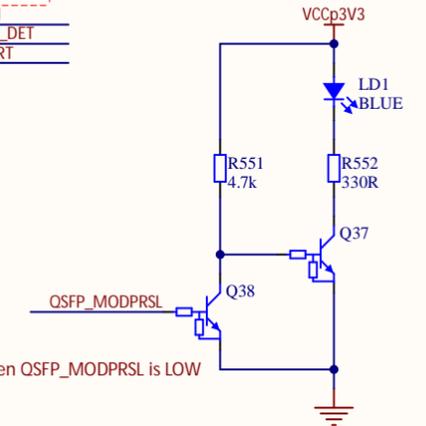


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QSFP

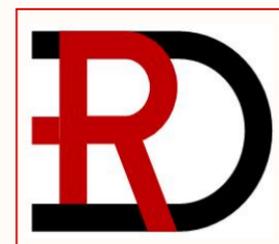
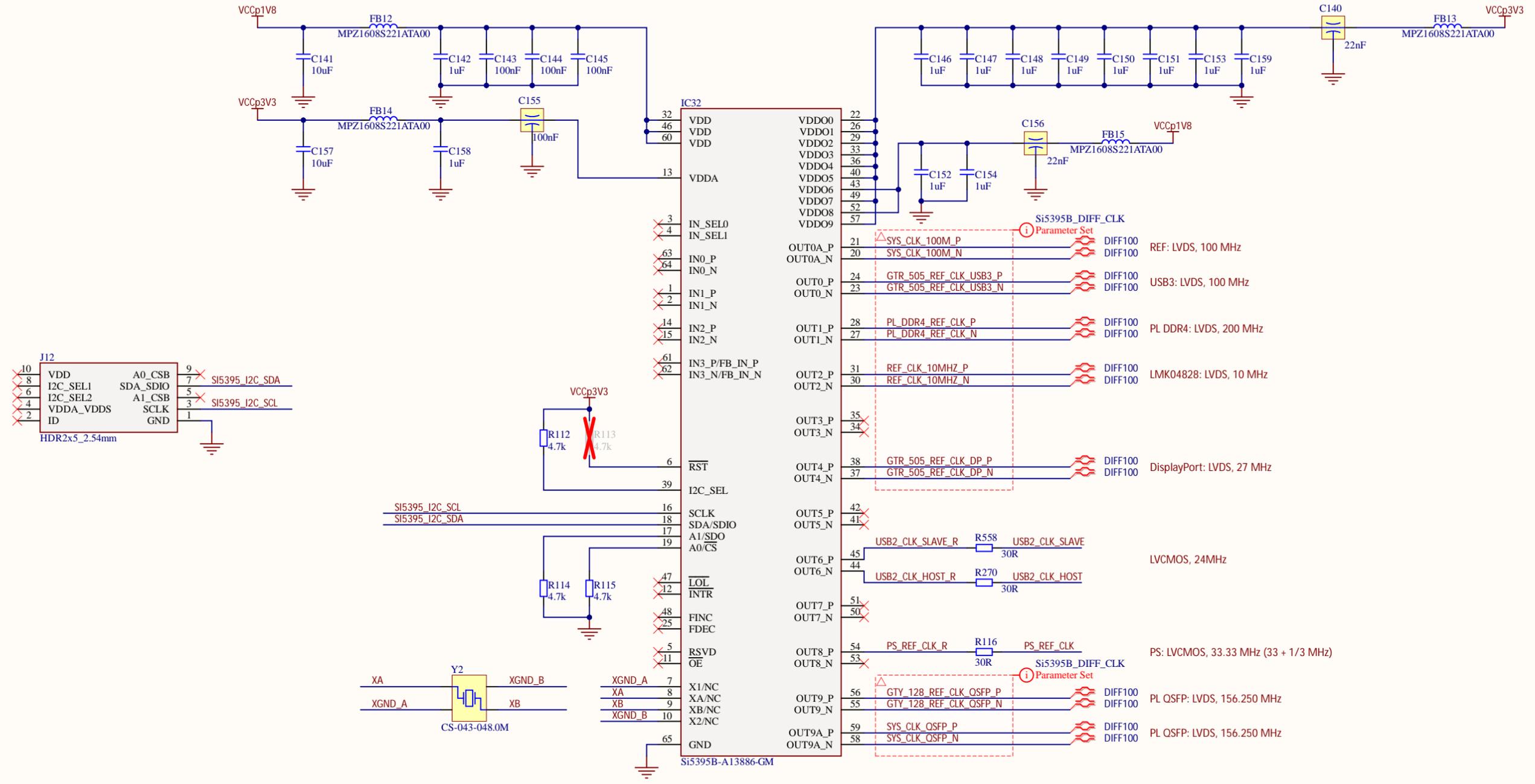


- | | | | |
|---------|--------------------------|-------------|---------------------------|
| SC1 | Screw, Phillips, M2, 6mm | STDF1 | SMD Standoff, M2, L:2.5mm |
| M2, 6mm | | 9774025243R | |
| SC2 | Screw, Phillips, M2, 6mm | STDF2 | SMD Standoff, M2, L:2.5mm |
| M2, 6mm | | 9774025243R | |
| SC3 | Screw, Phillips, M2, 6mm | STDF3 | SMD Standoff, M2, L:2.5mm |
| M2, 6mm | | 9774025243R | |
| SC4 | Screw, Phillips, M2, 6mm | STDF4 | SMD Standoff, M2, L:2.5mm |
| M2, 6mm | | 9774025243R | |



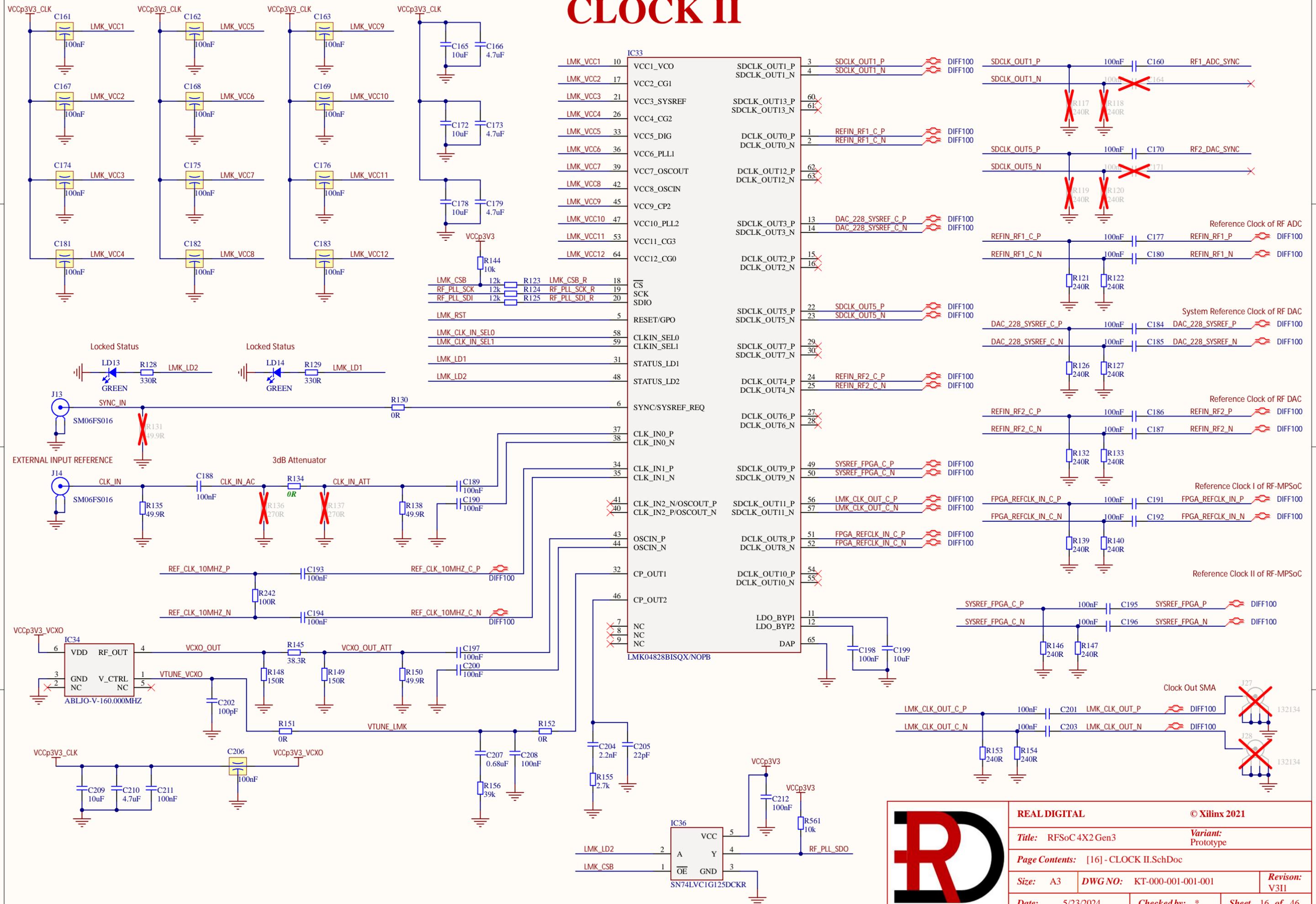
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CLOCK I: SYS, DDR4, MGT, GTY AND USER



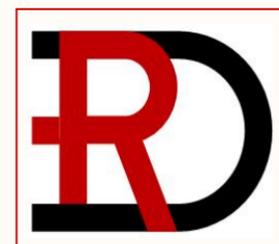
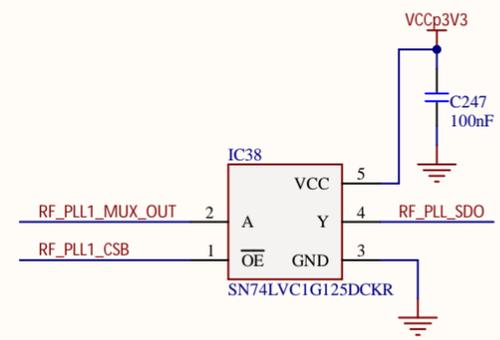
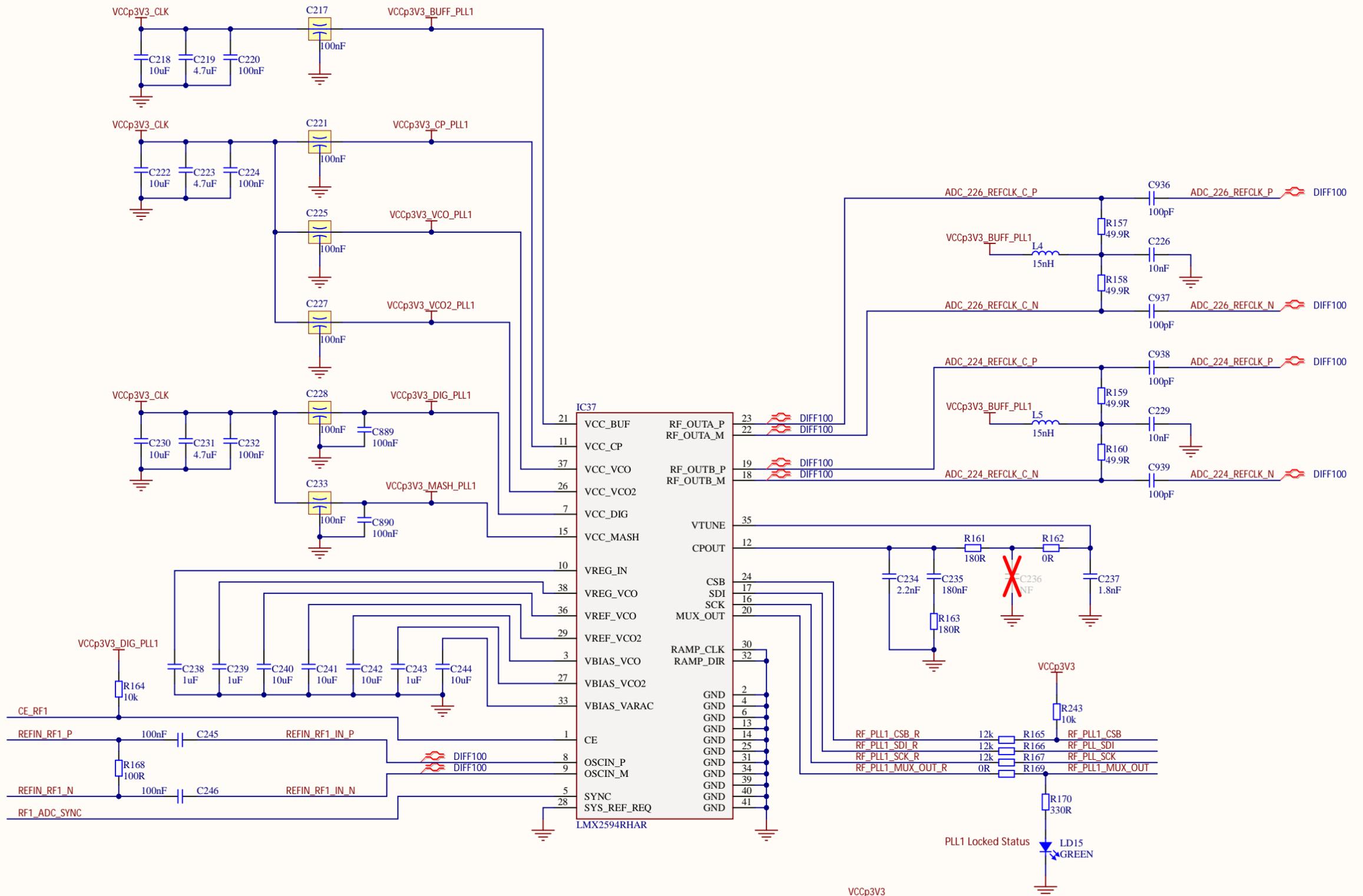
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CLOCK II



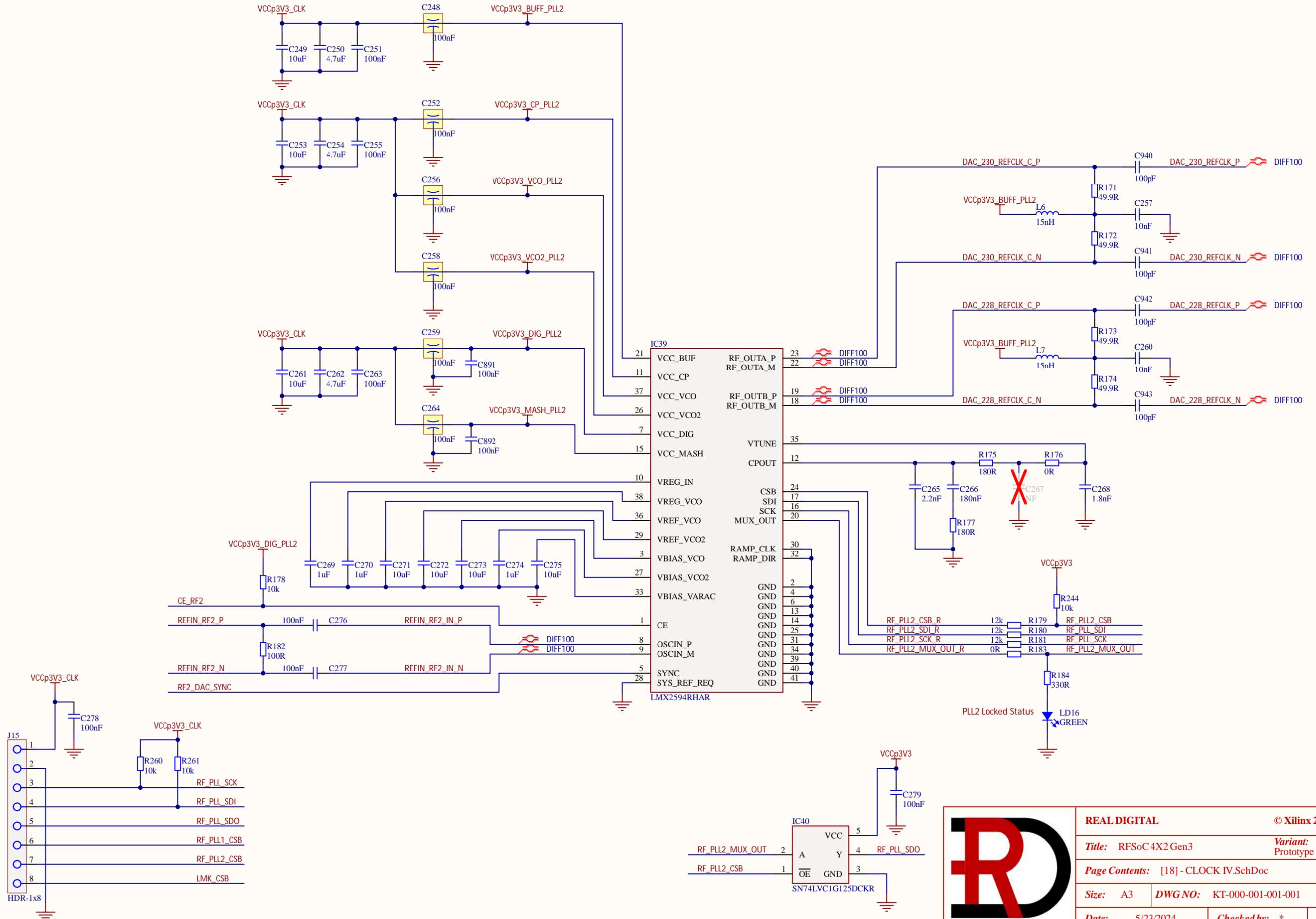
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CLOCK III: RF ADC CLOCK



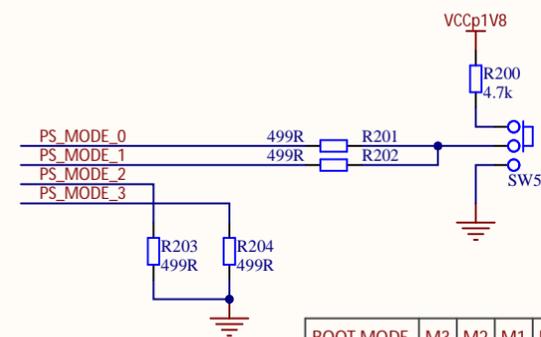
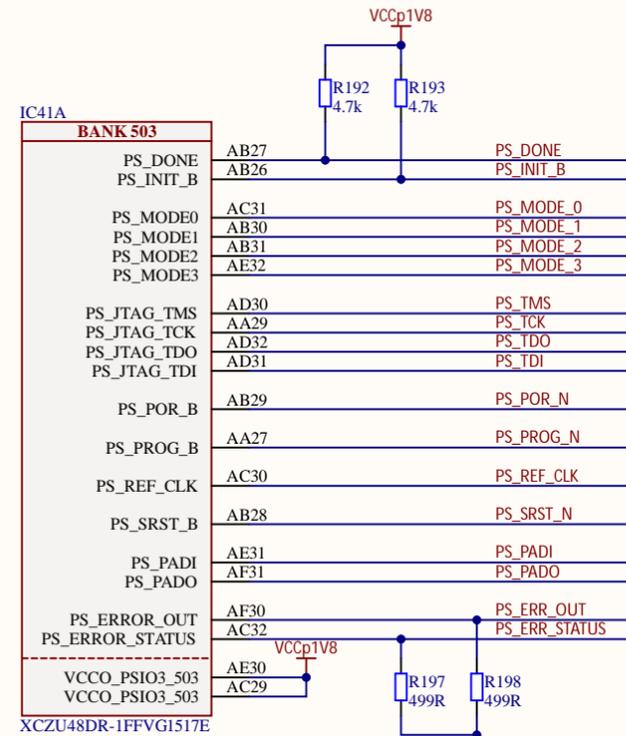
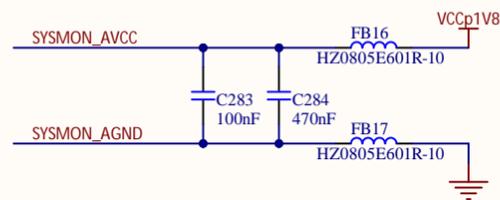
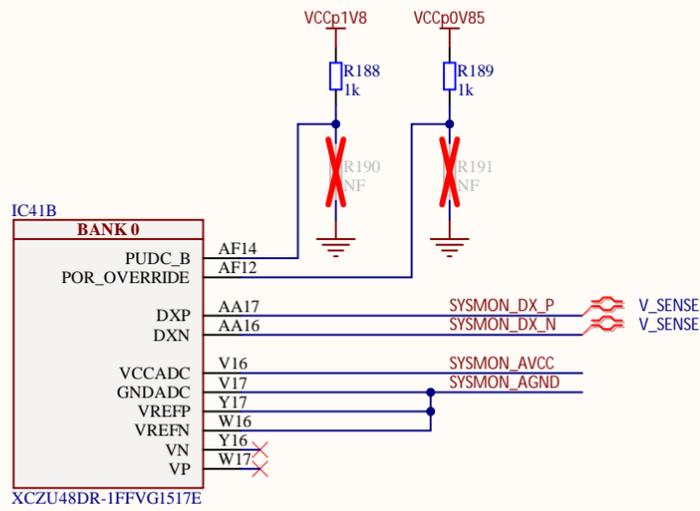
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CLOCK IV: RF DAC CLOCK

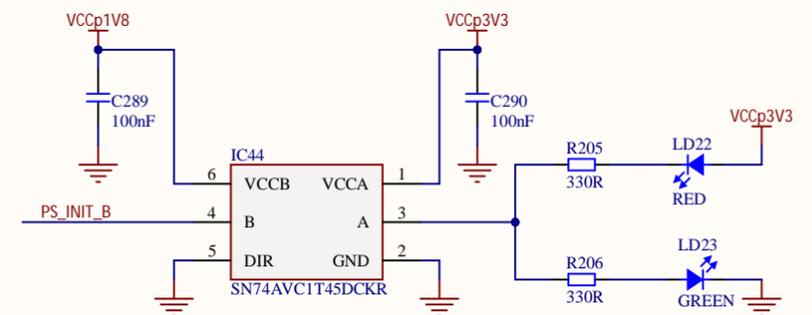
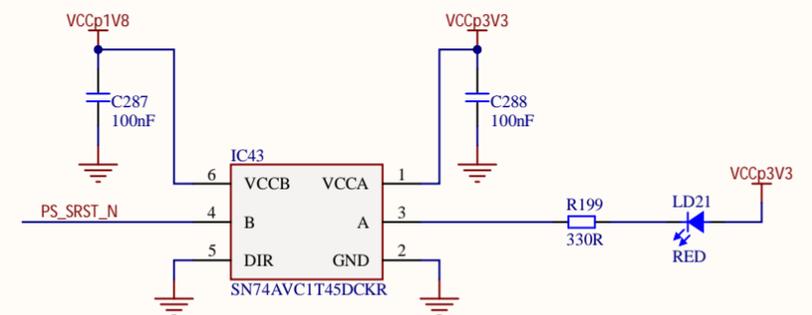
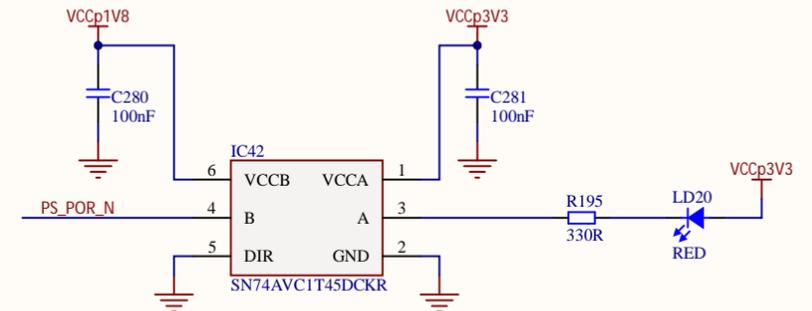
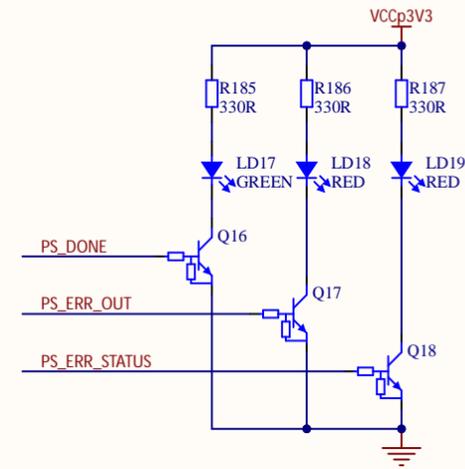
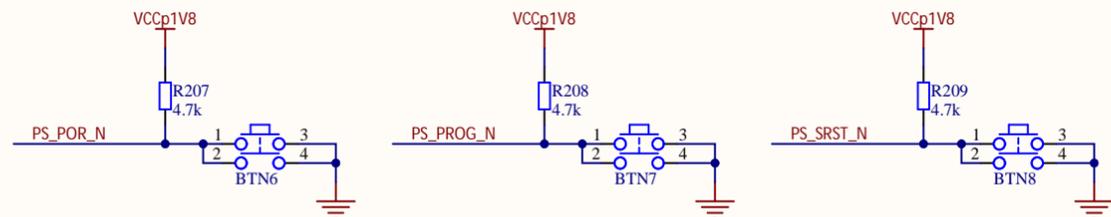


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RFSOC CONFIG

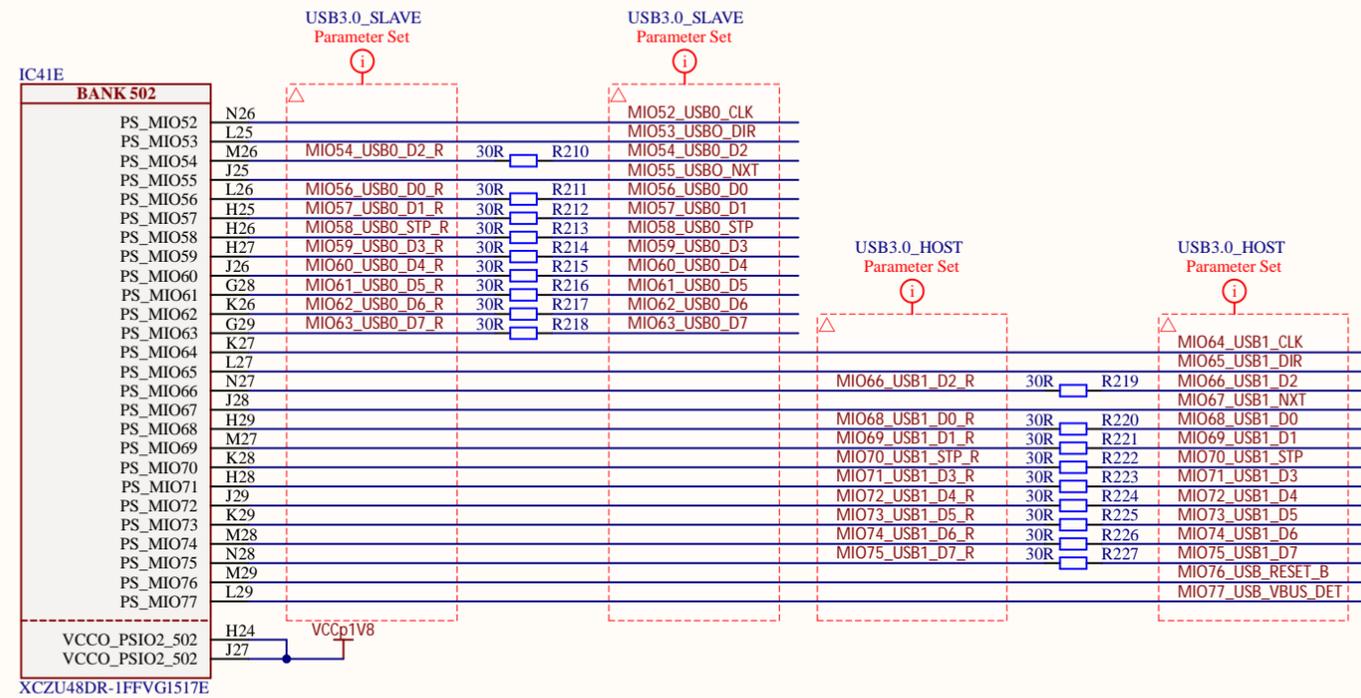
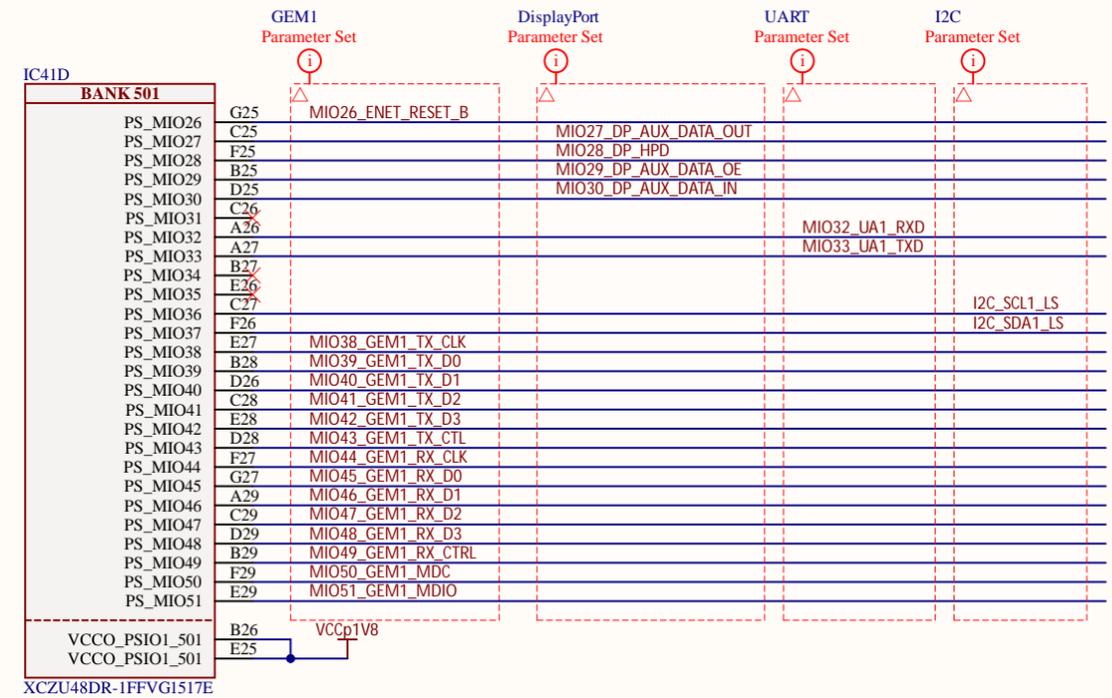
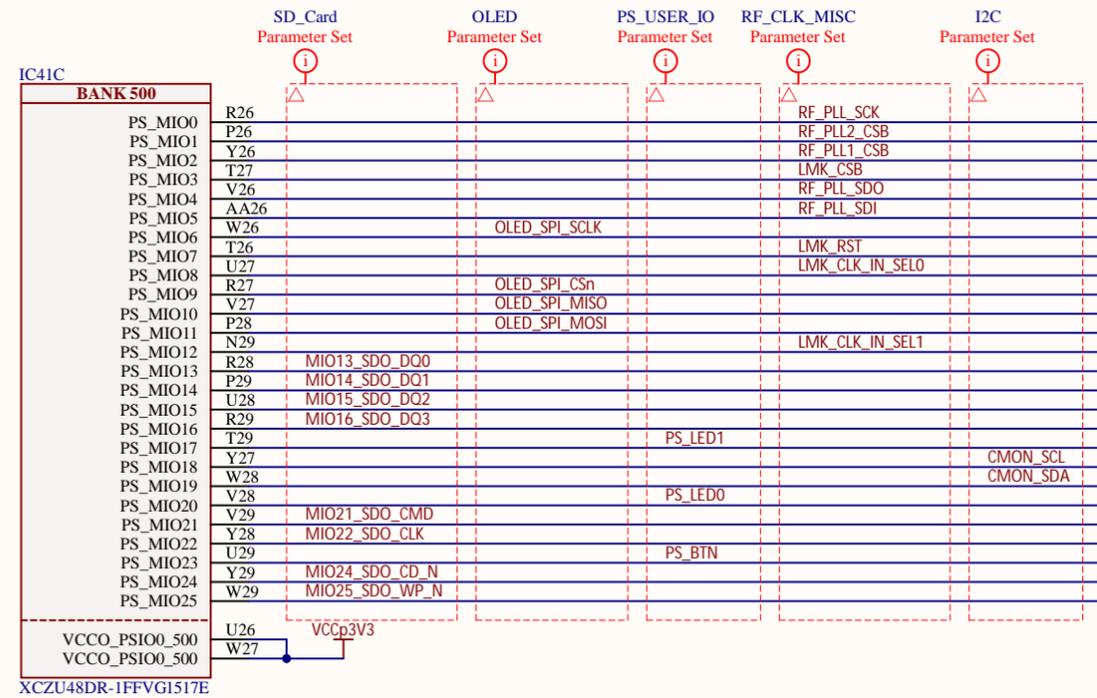


| BOOT-MODE | M3 | M2 | M1 | M0 |
|-----------|----|----|----|----|
| JTAG | L | L | L | L |
| SD Card | L | L | H | H |



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PS: BANKS 500-502



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| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
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| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 20 of 46 | |

PS: BANK 504

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BANK 504 1 OF 2

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| PS_DDR_BG0 | AN32 | PS_DDR4_BG0 |
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| PS_DDR_PARITY | AN31 | PS_DDR4_PARITY |
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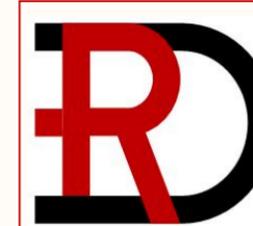
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BANK 504 2 OF 2

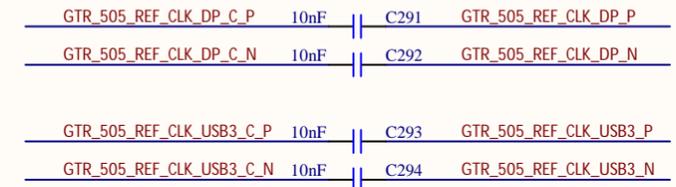
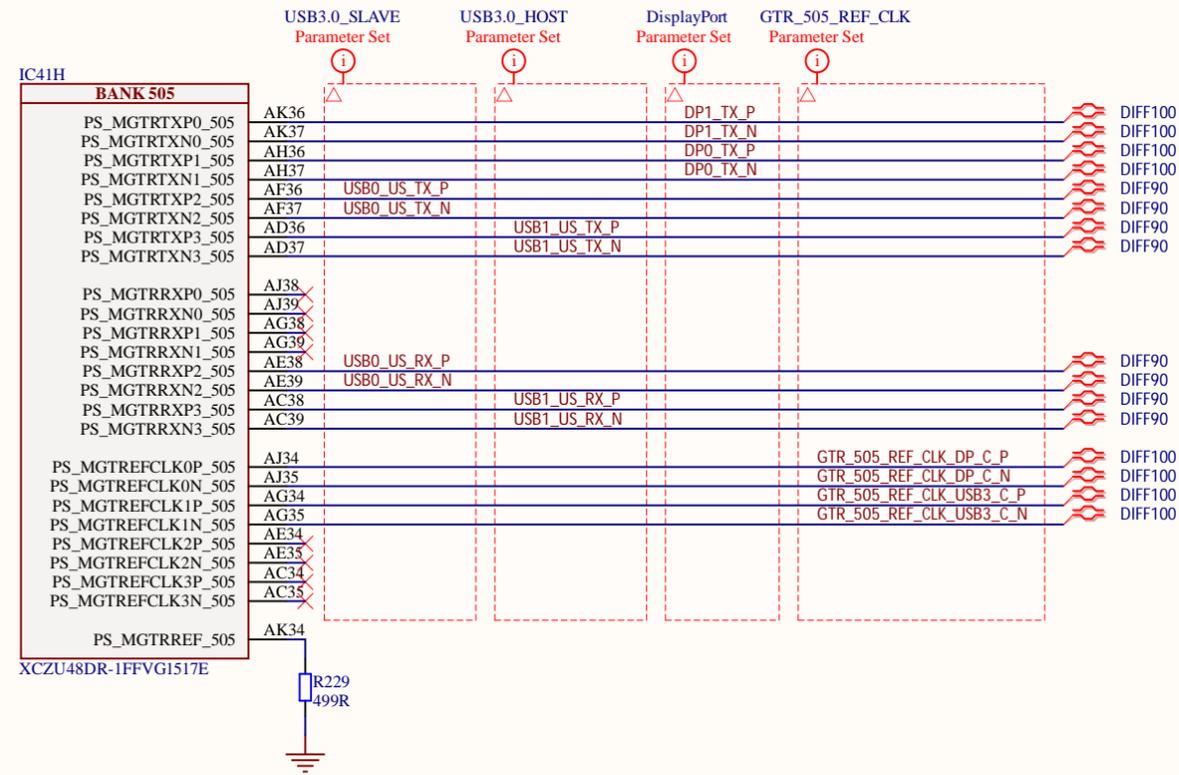
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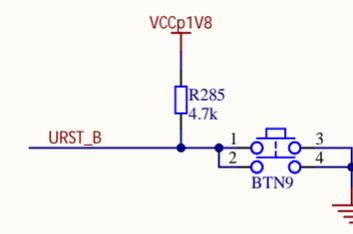
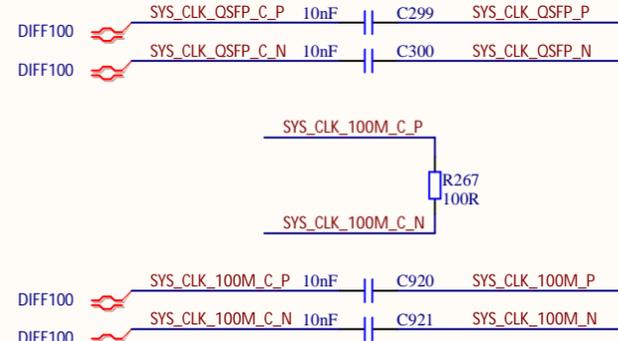
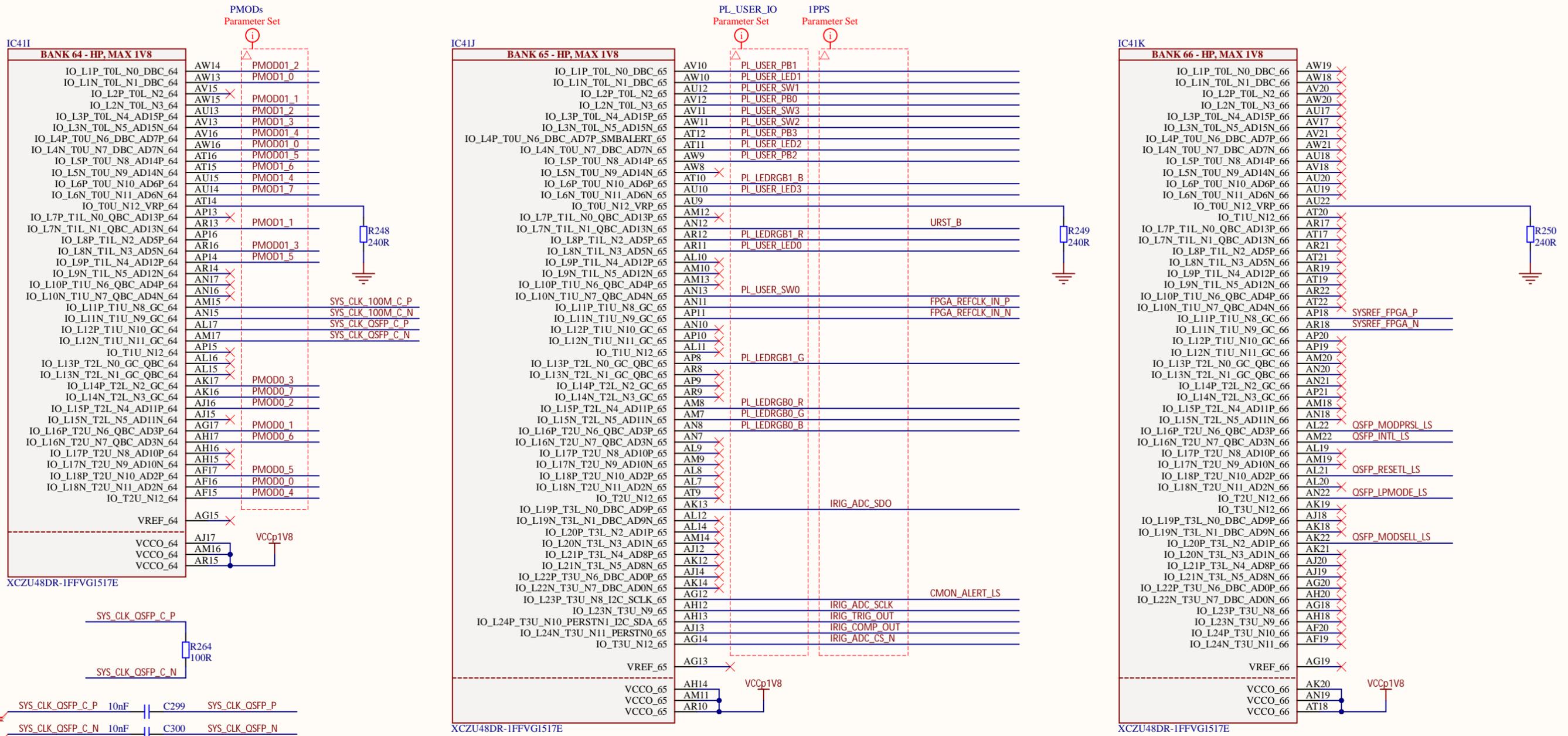
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PS: MGT



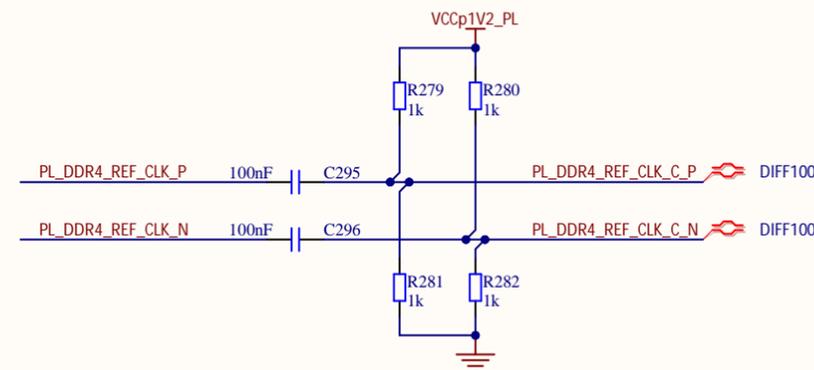
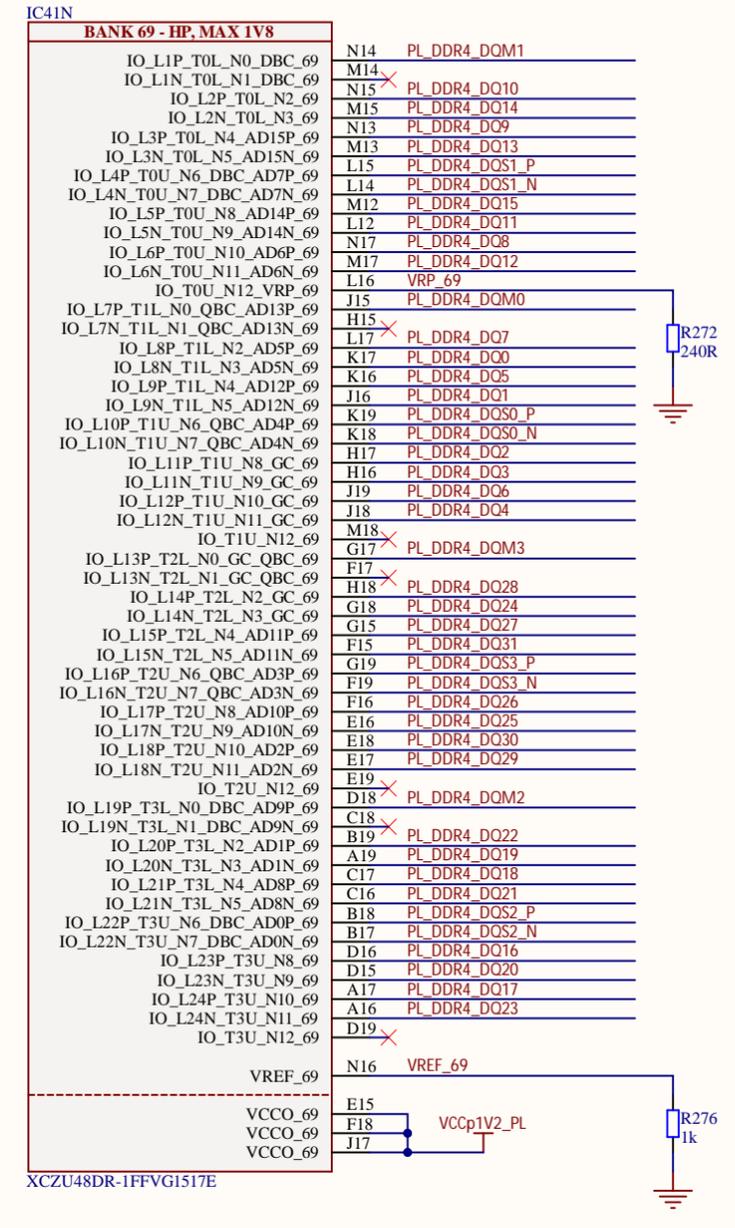
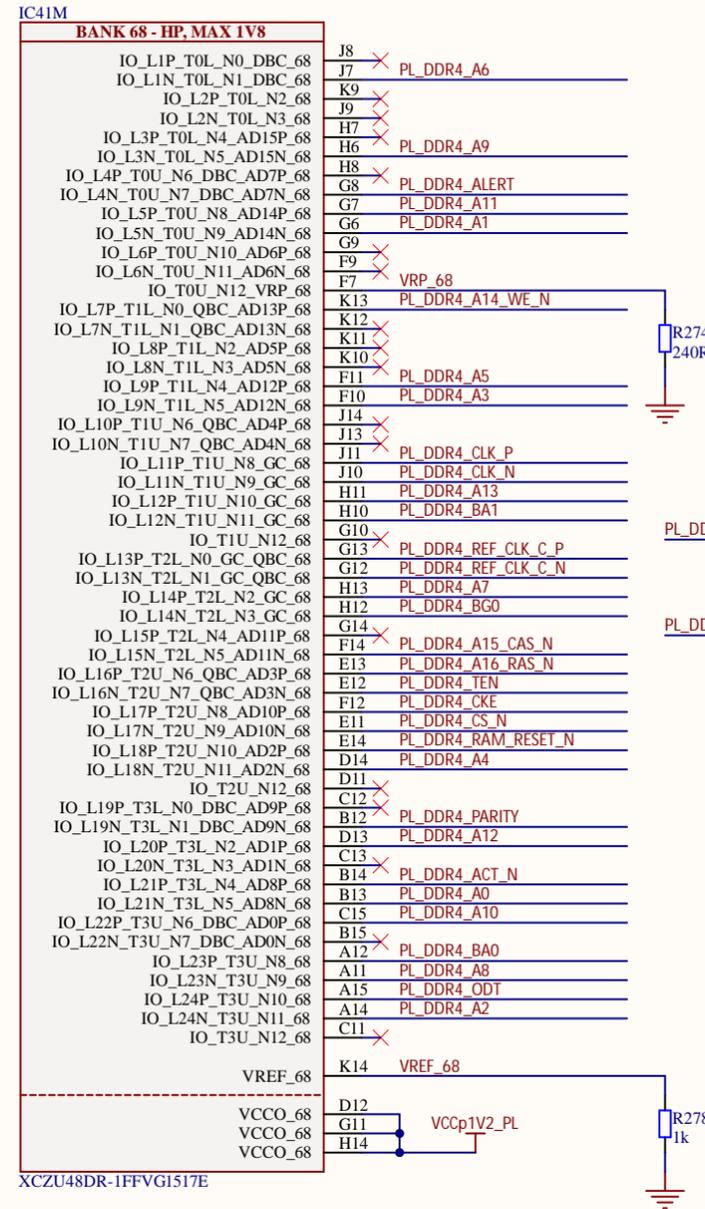
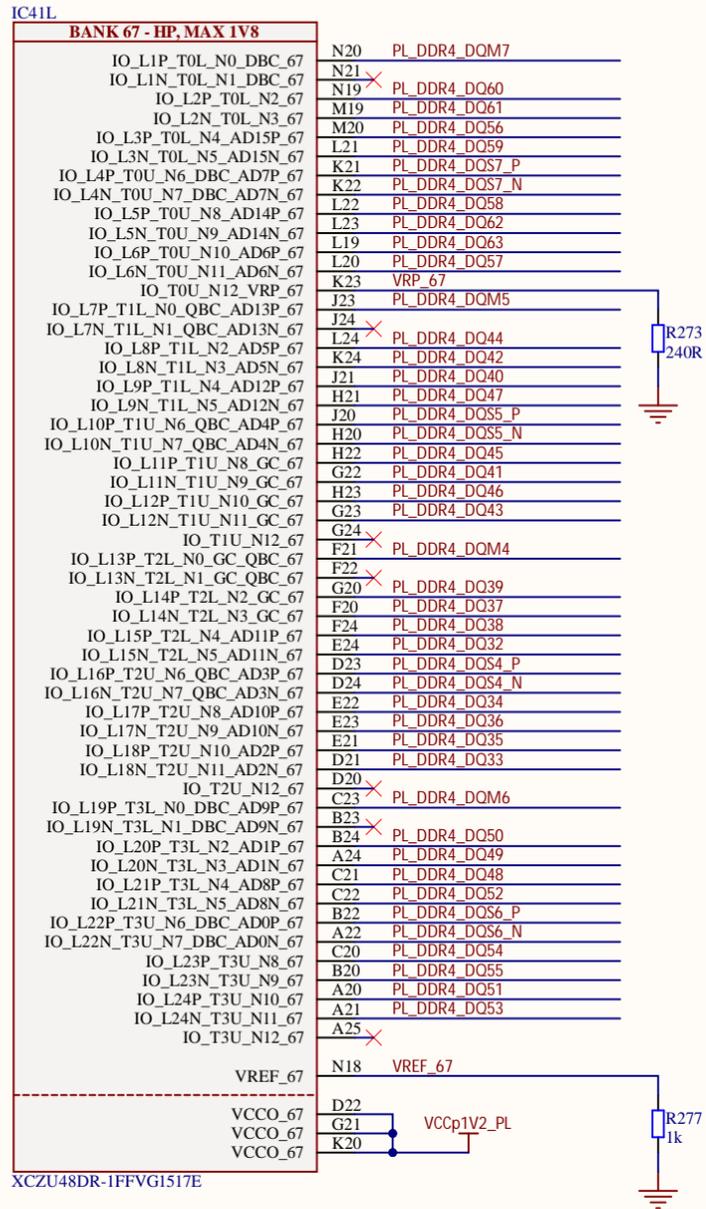
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PL: BANKS 64-66



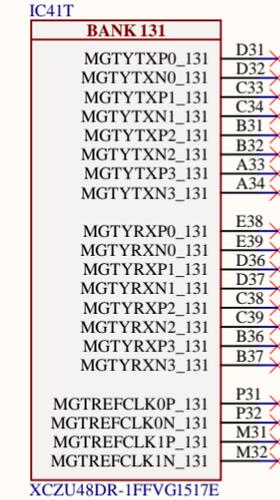
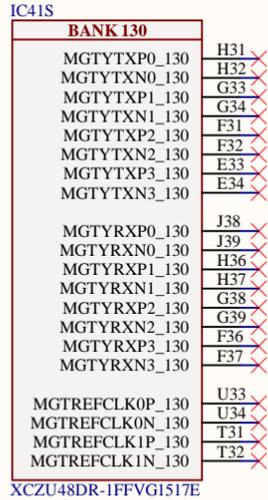
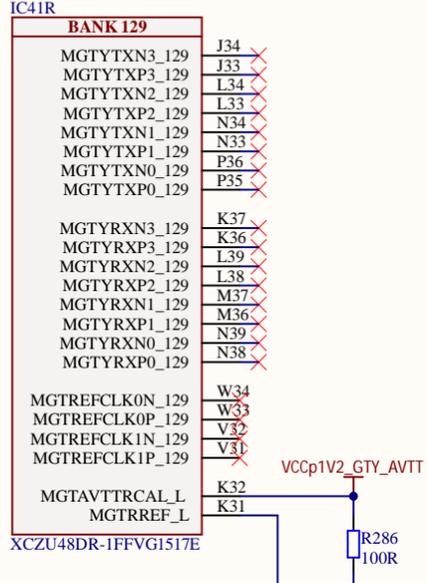
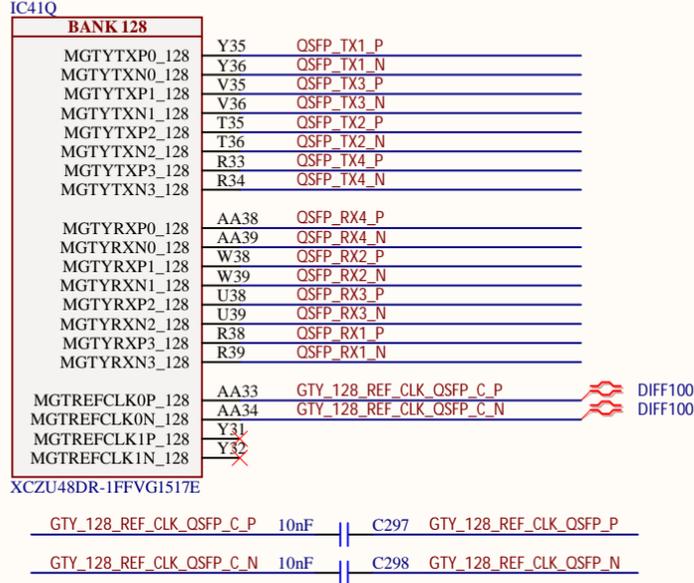
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PL: BANKS 67-69



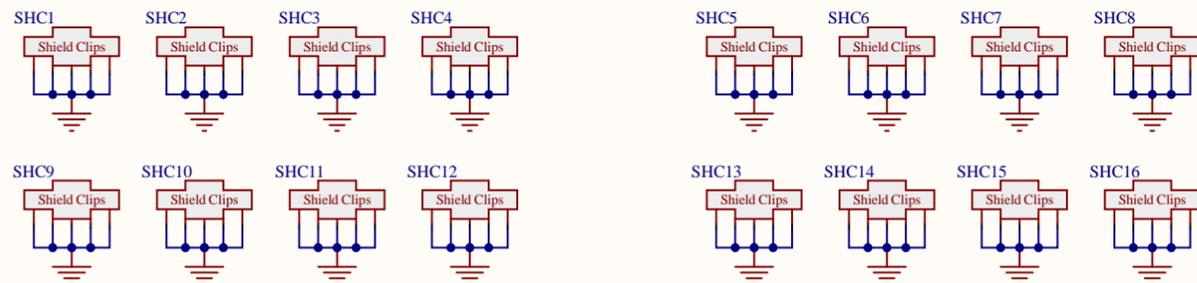
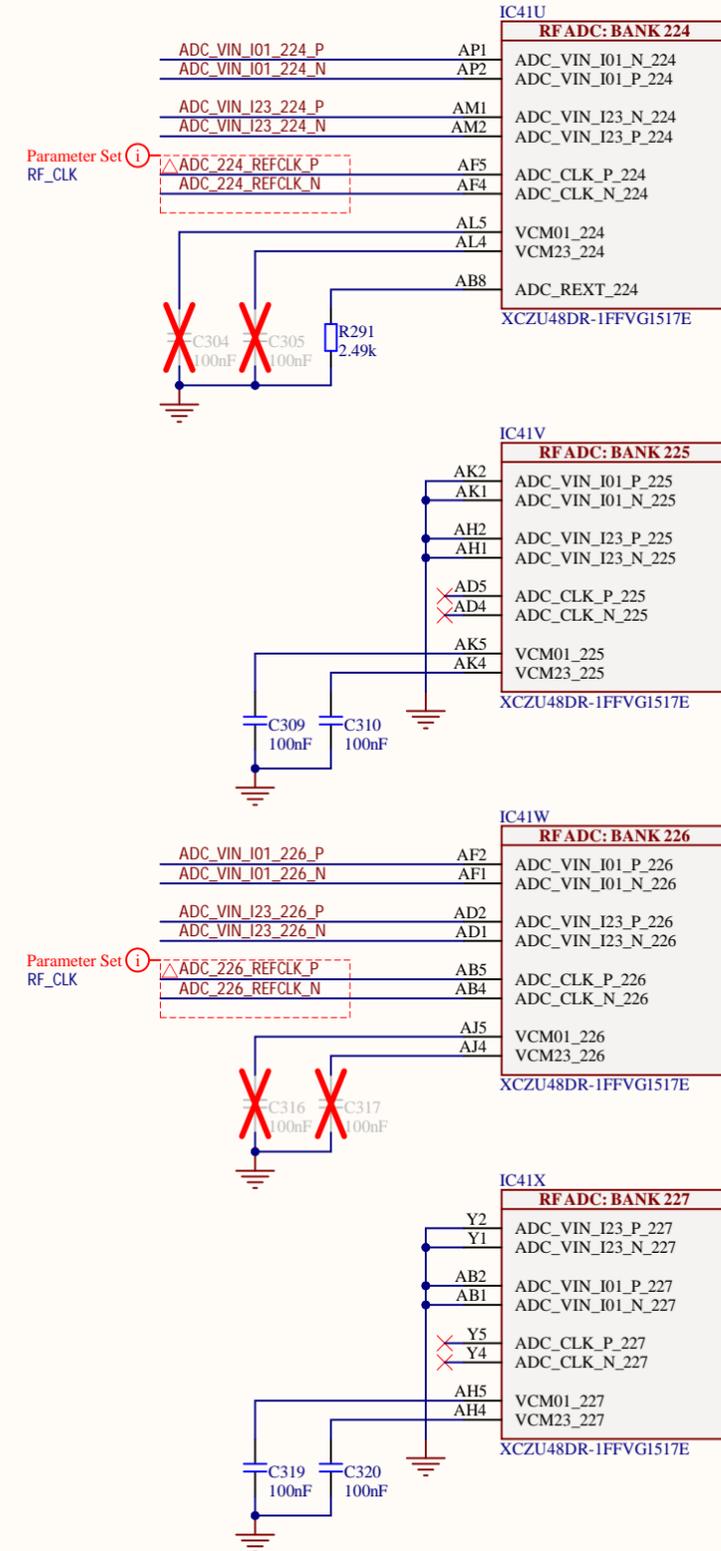
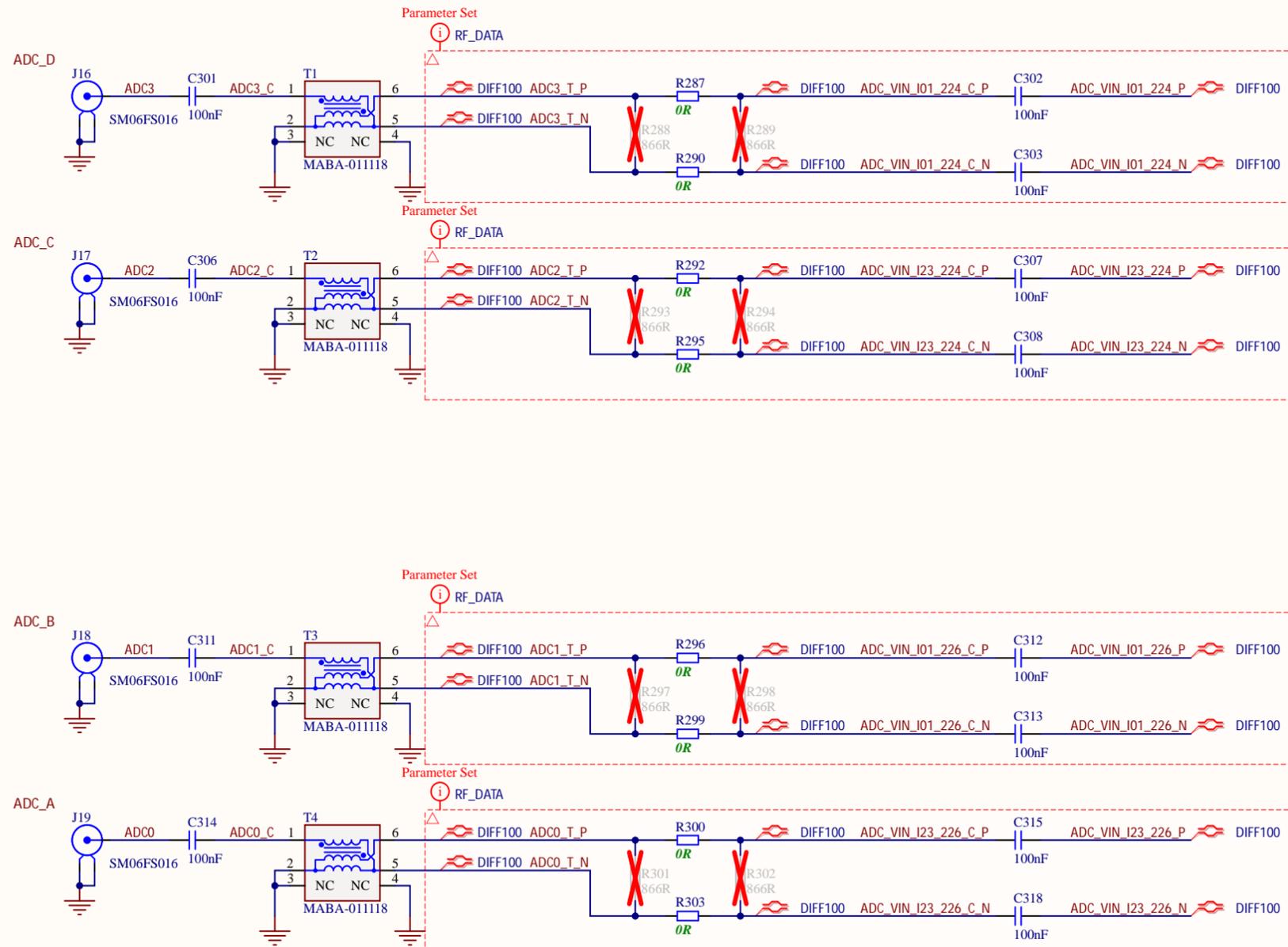
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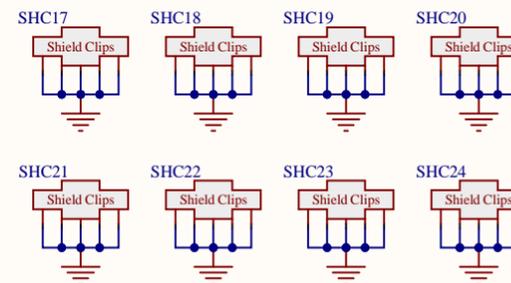
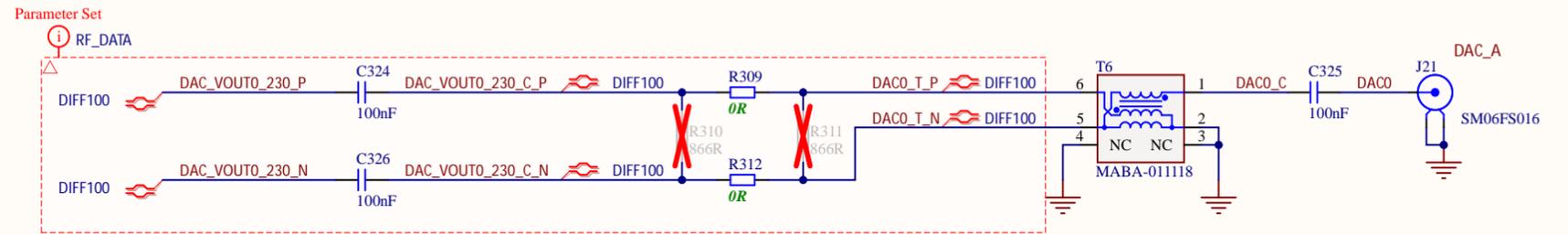
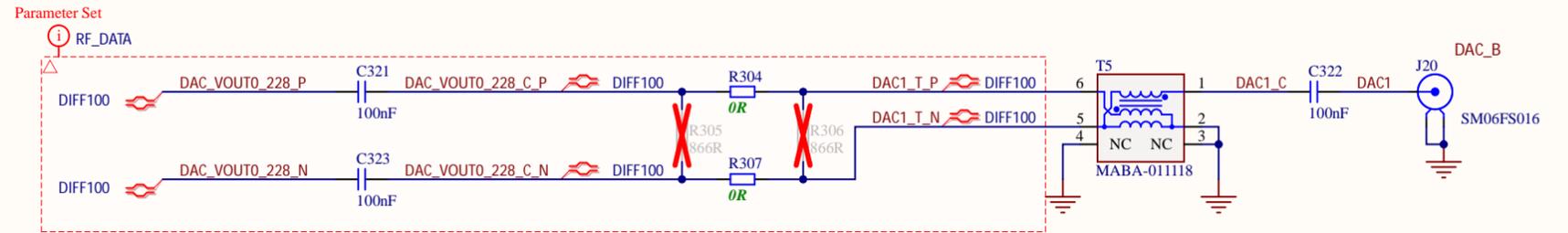
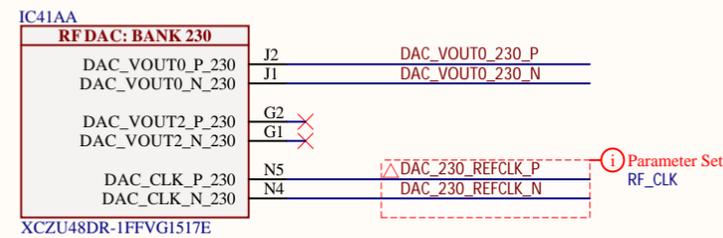
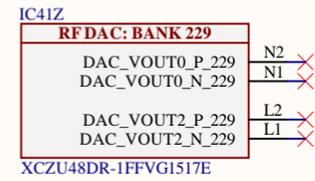
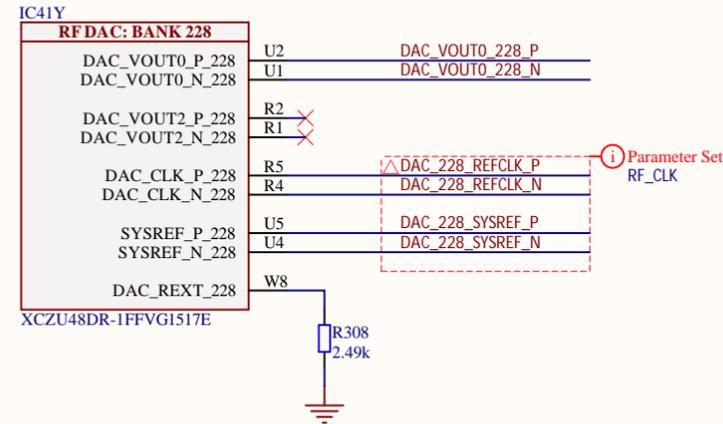
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RF ADC



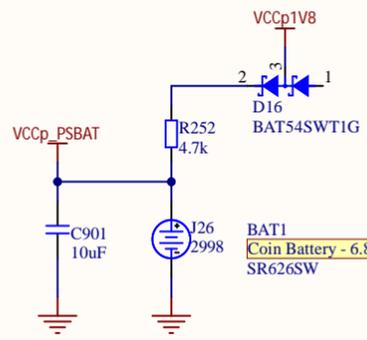
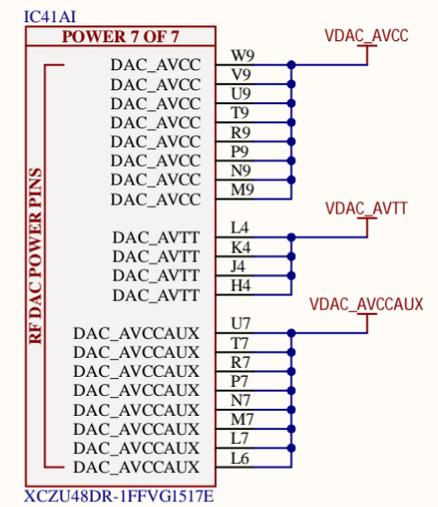
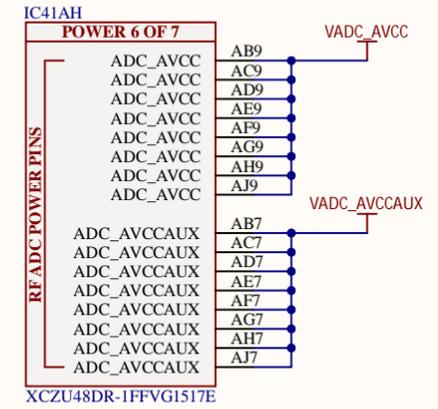
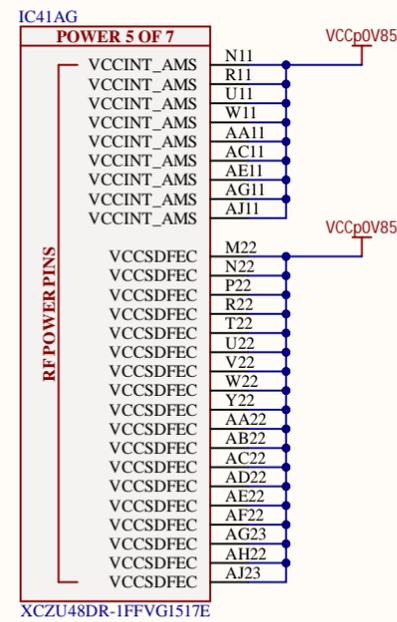
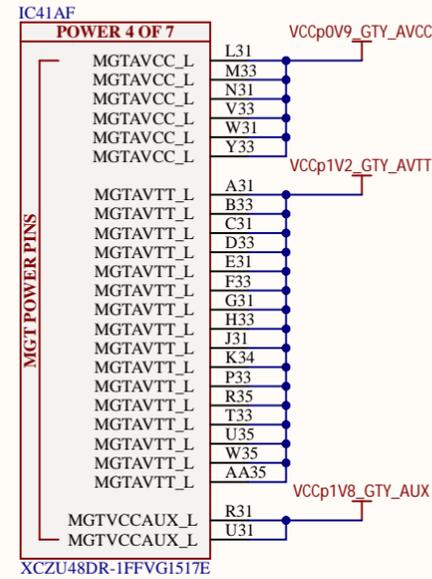
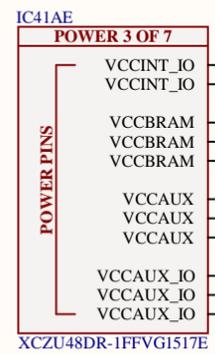
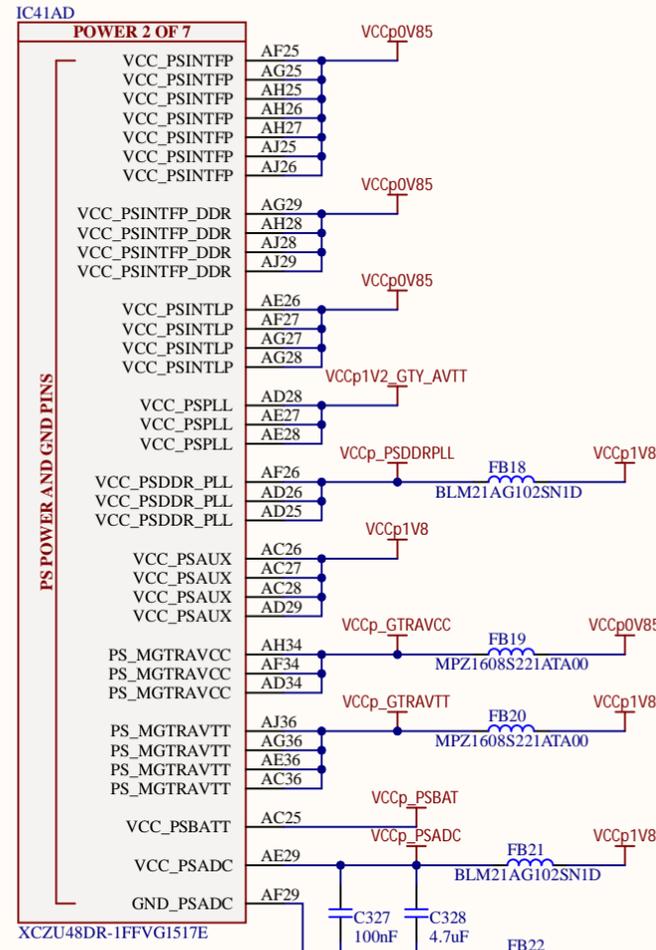
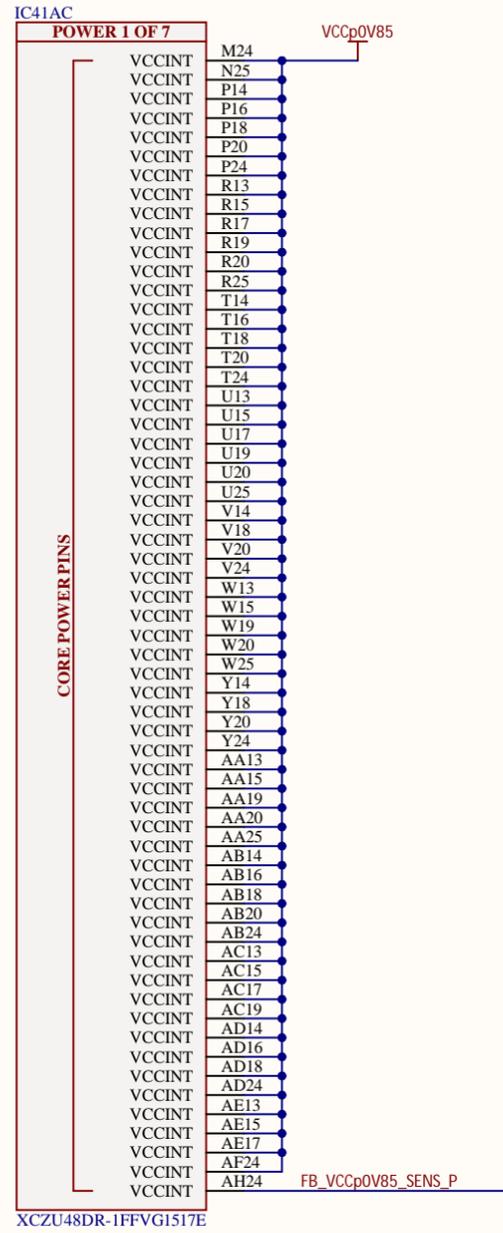
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RF DAC



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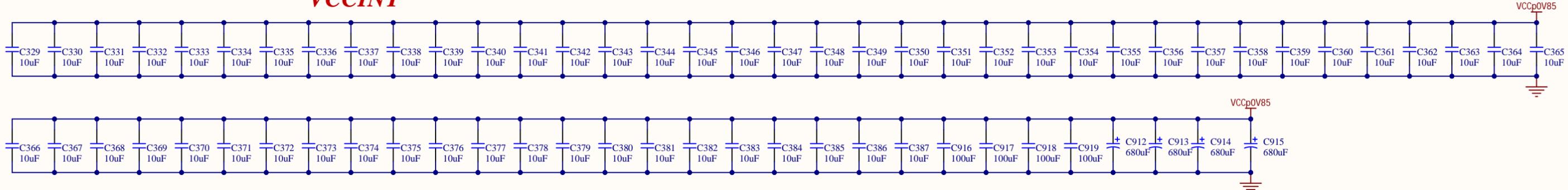
RFSoc POWER Pins



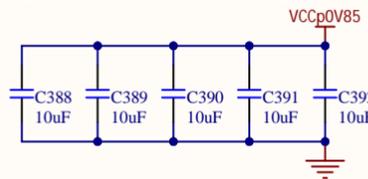
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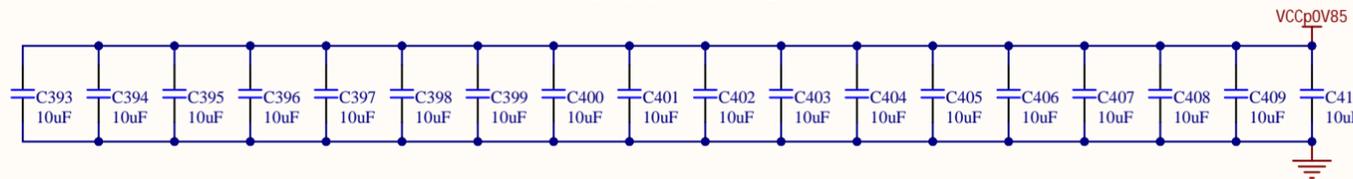
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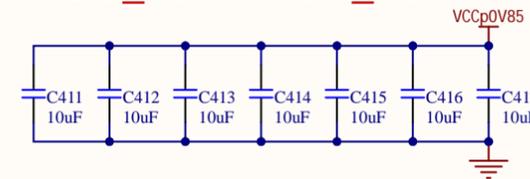
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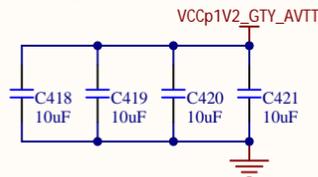
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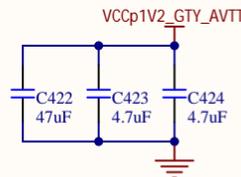
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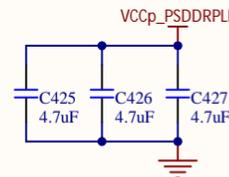
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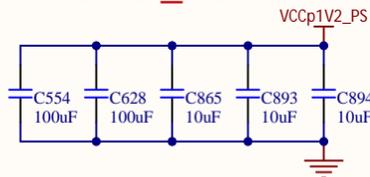
PSPLL



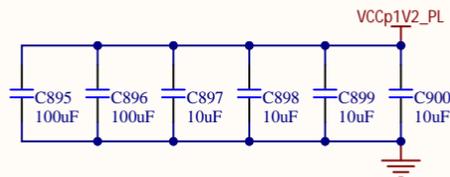
PS DDRPLL



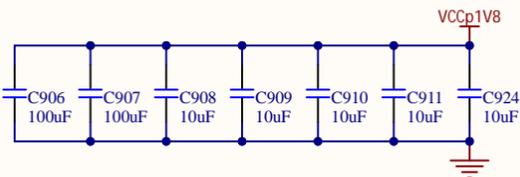
VCCO_PSDDR



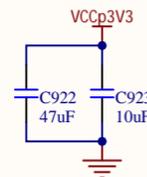
VCCO PLDDR



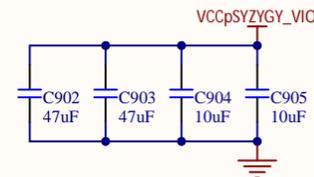
VCCO 1V8



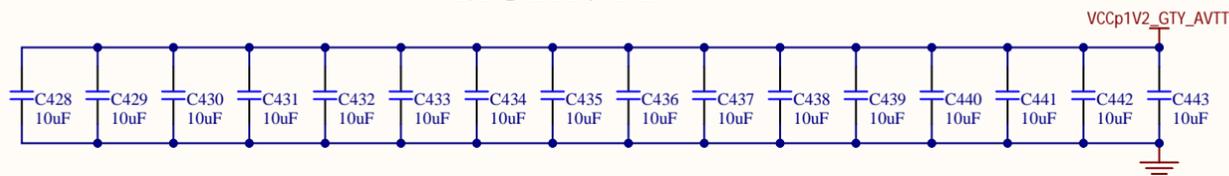
VCCO 3V3



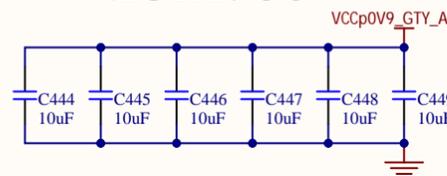
VCCO SYZYGY



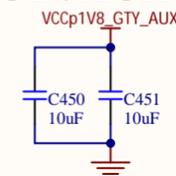
MGTAVTT



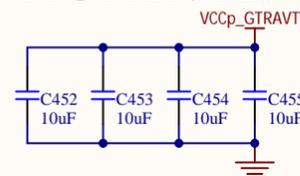
MGTAVCC



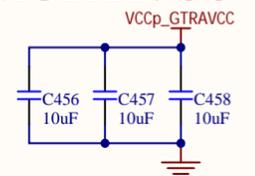
MGTVAUX



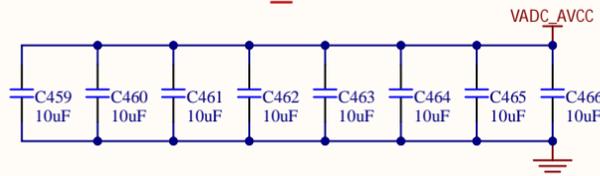
MGTRAVTT



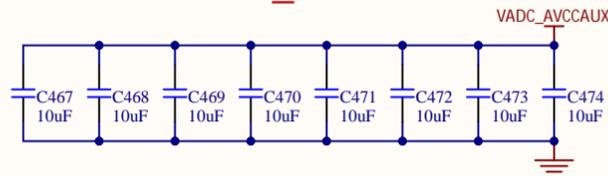
MGTRAVCC



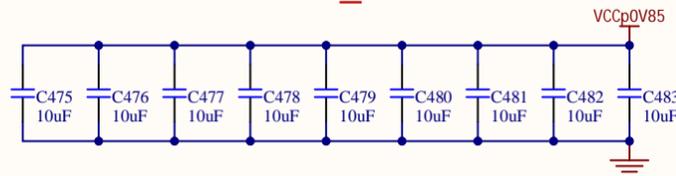
VADC_AVCC



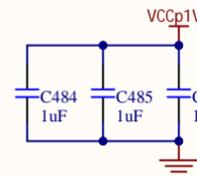
VADC_AVCCAUX



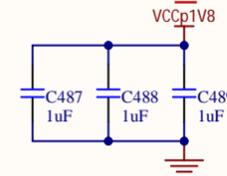
VCCINT_AMS



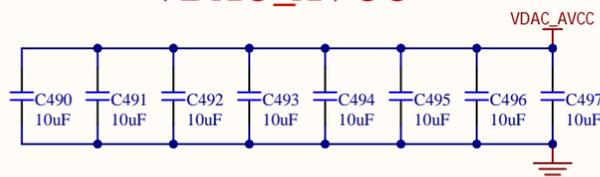
VCCAUX



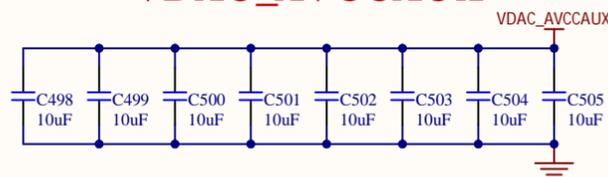
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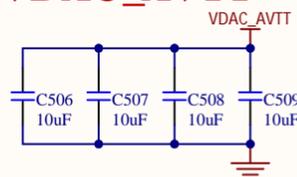
VDAC_AVCC



VDAC_AVCCAUX

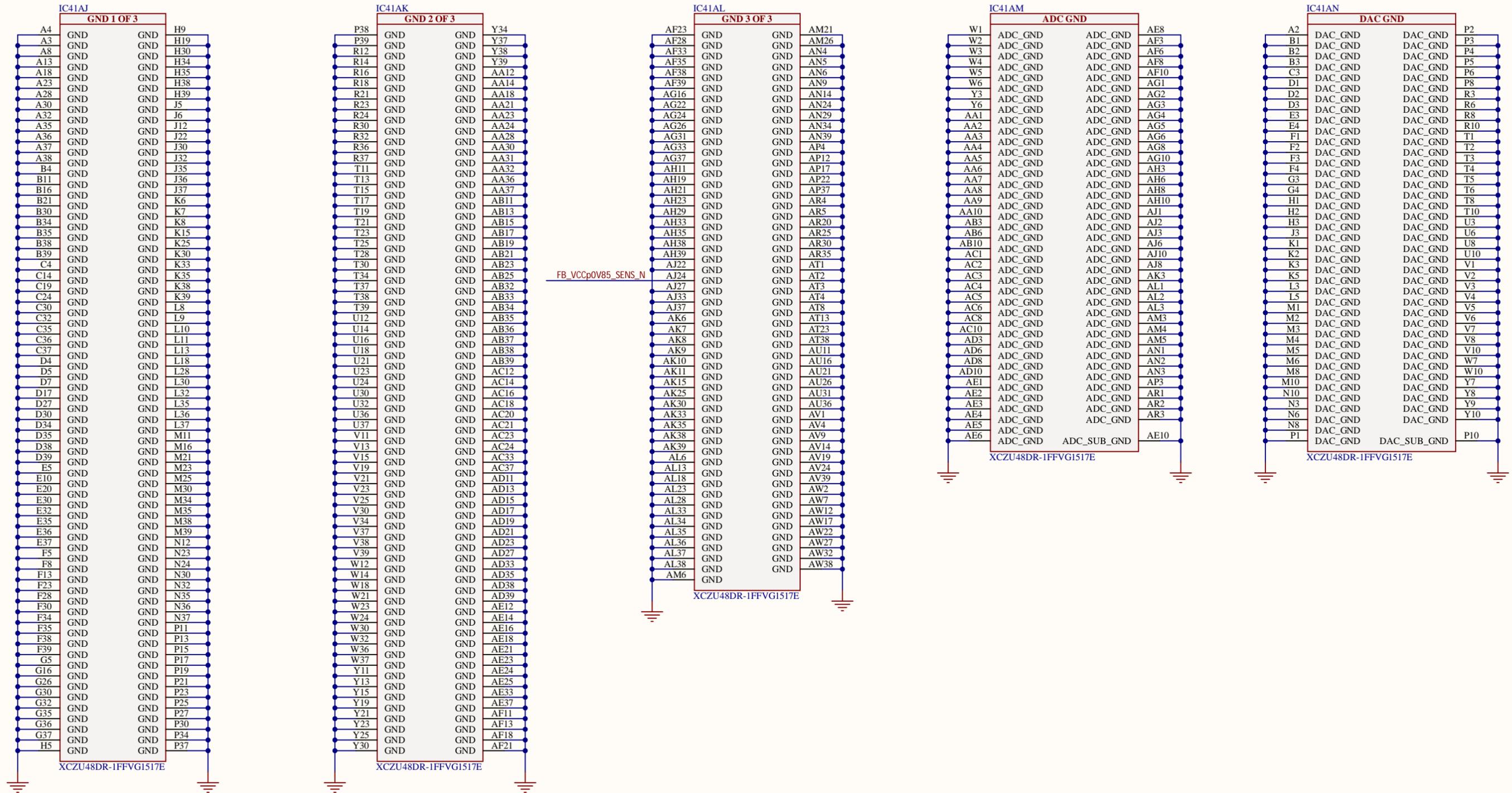


VDAC_AVTT



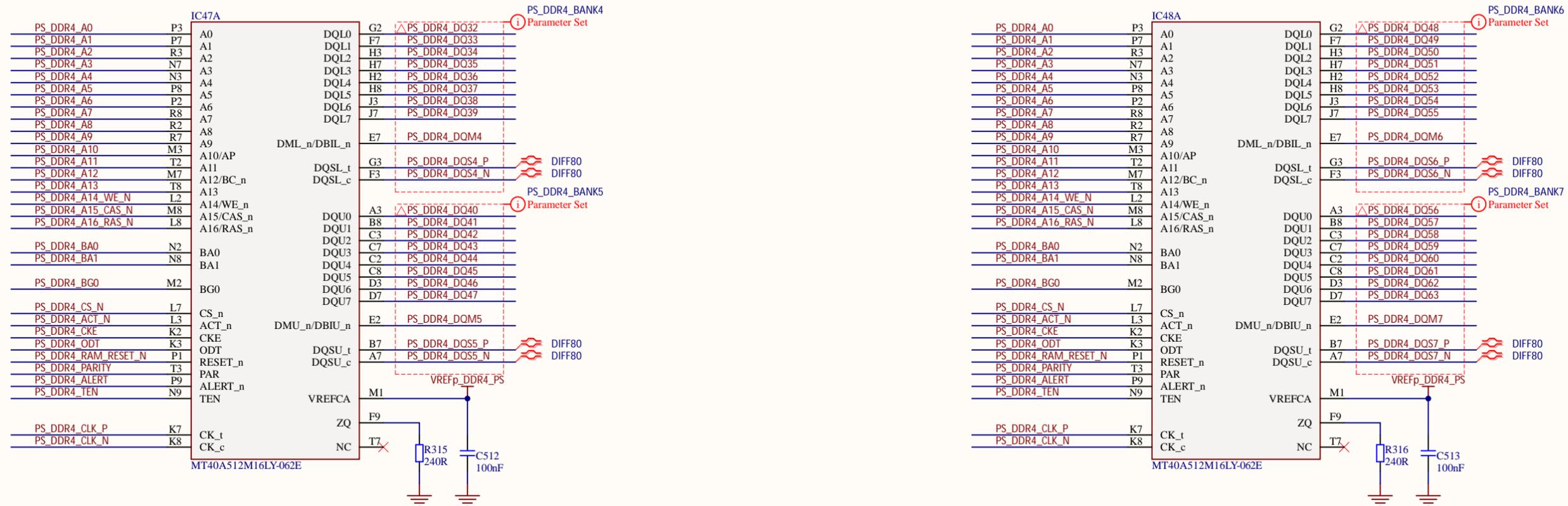
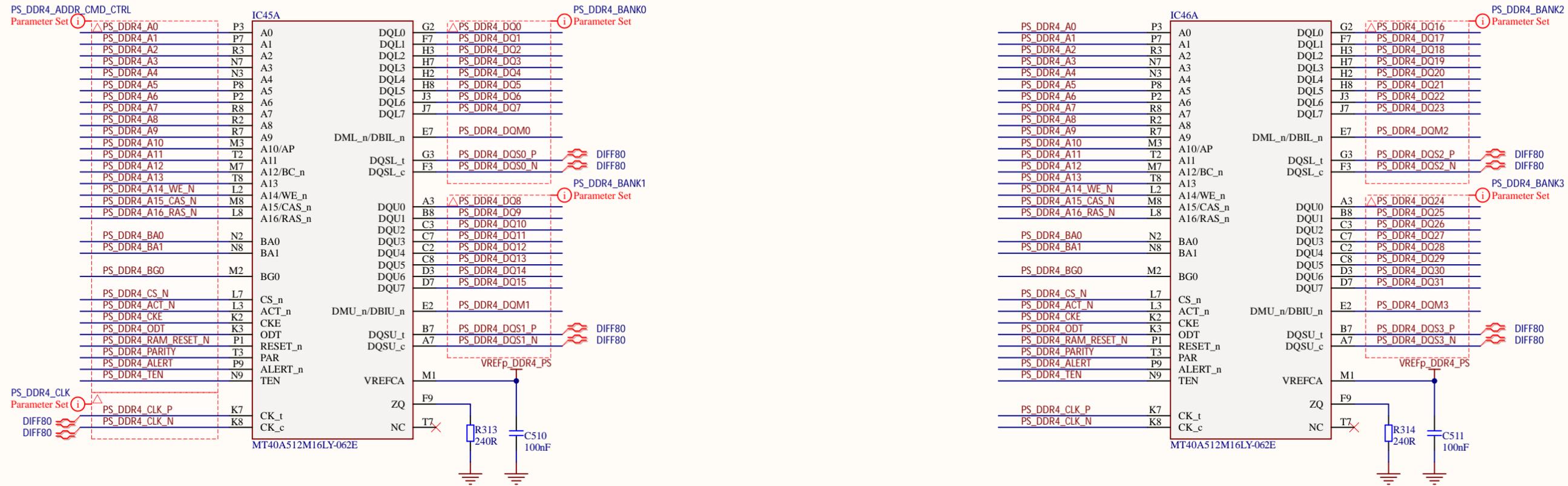
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [30] - RFSoc DECOUPLING.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 30 of 46 | |

RFSoc GND Pins



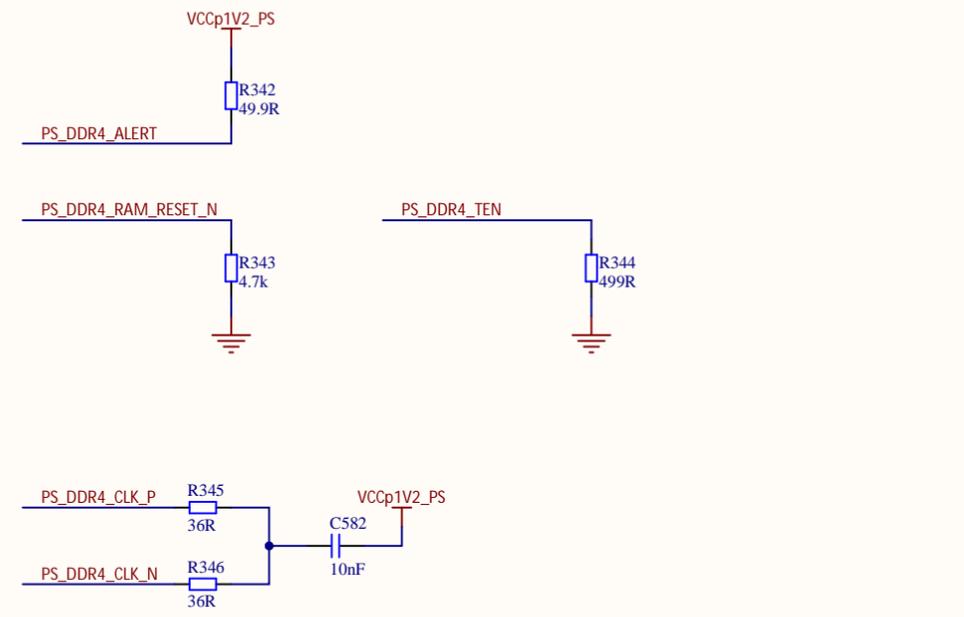
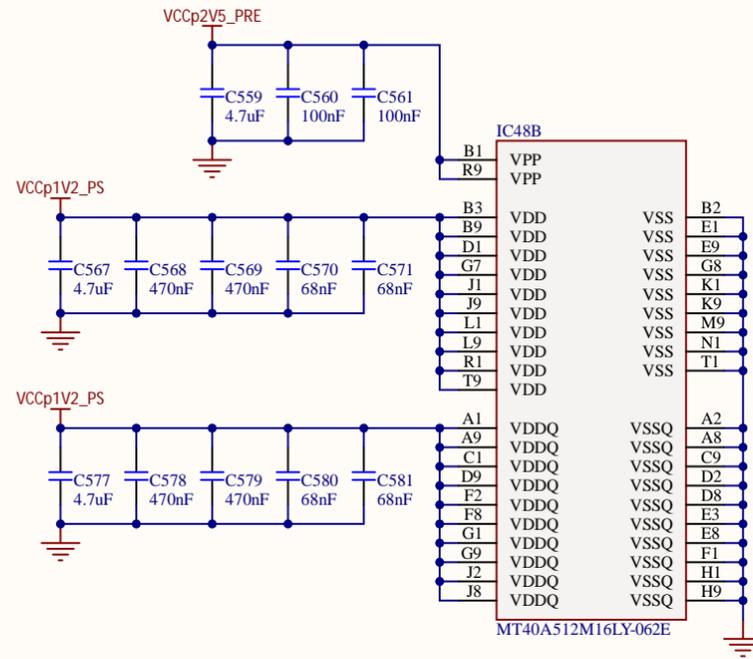
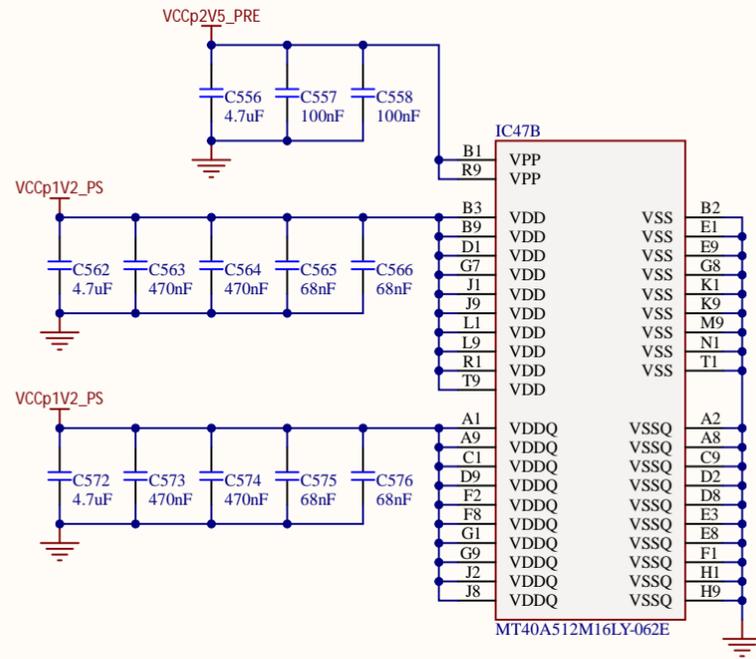
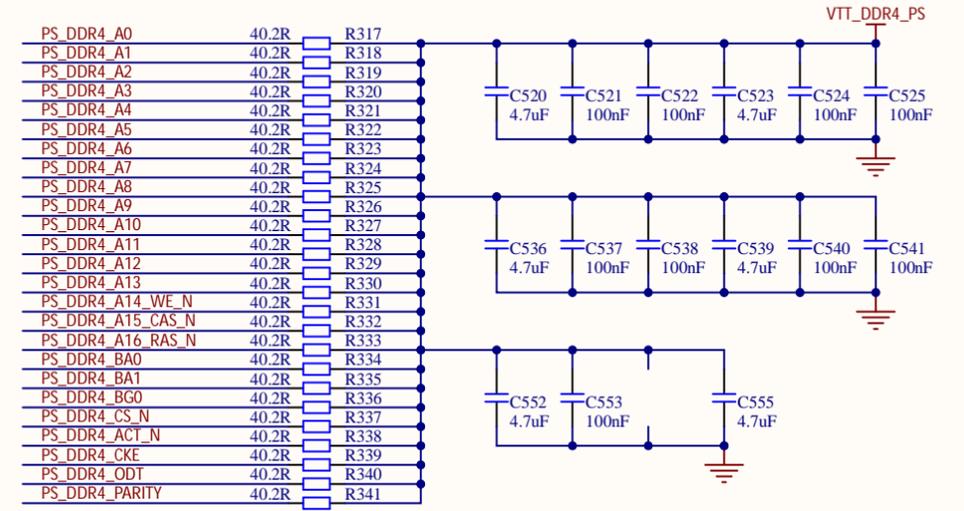
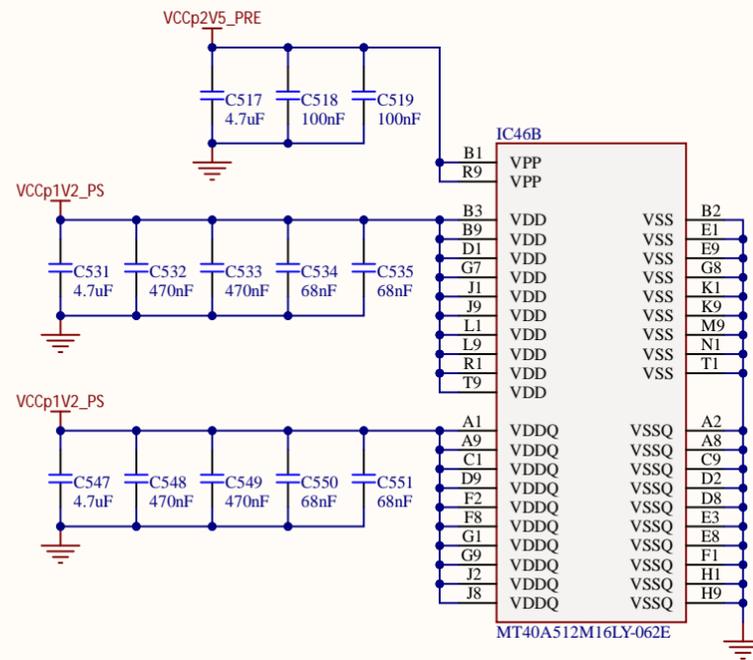
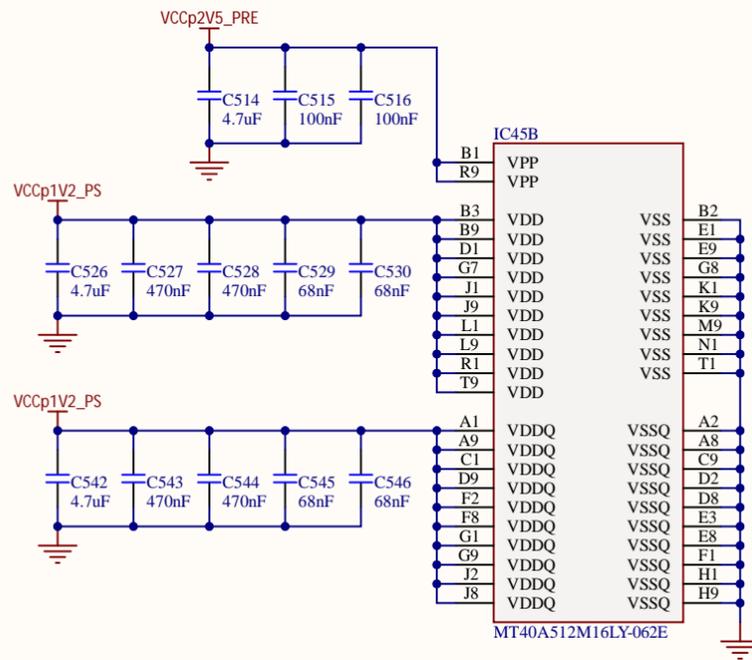
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [31] - RFSoc GND Pins.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 31 of 46 | |

DDR4 MEMORY PS I



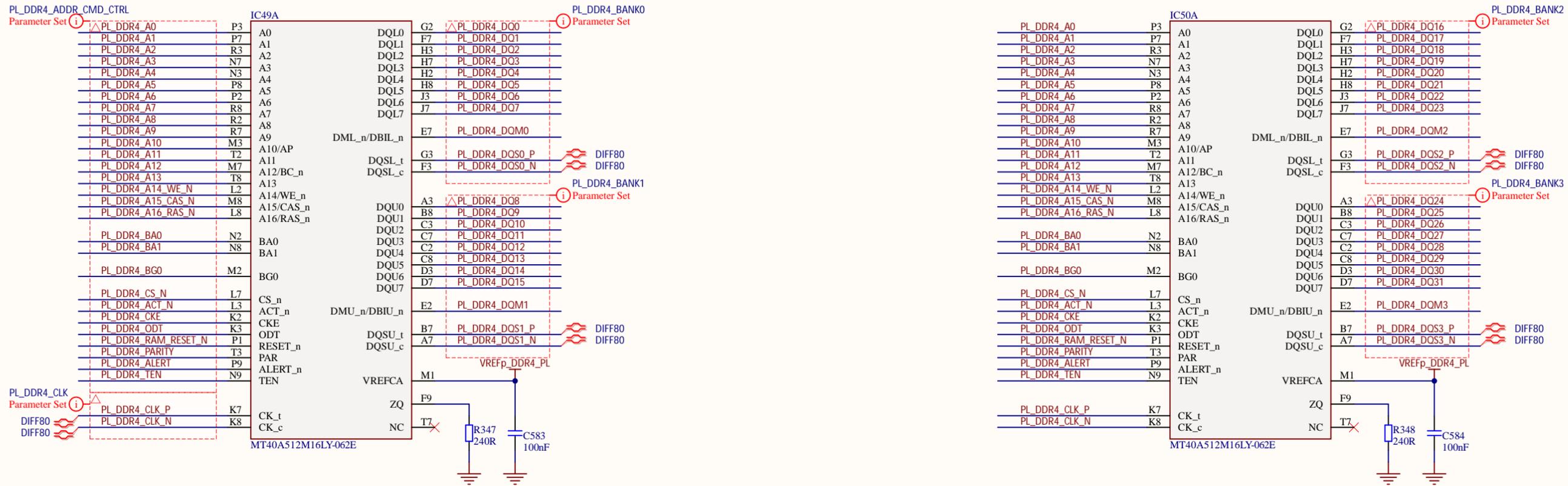
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| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [32] - DDR4 MEMORY PS I.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 32 of 46 | |

DDR4 MEMORY PS II

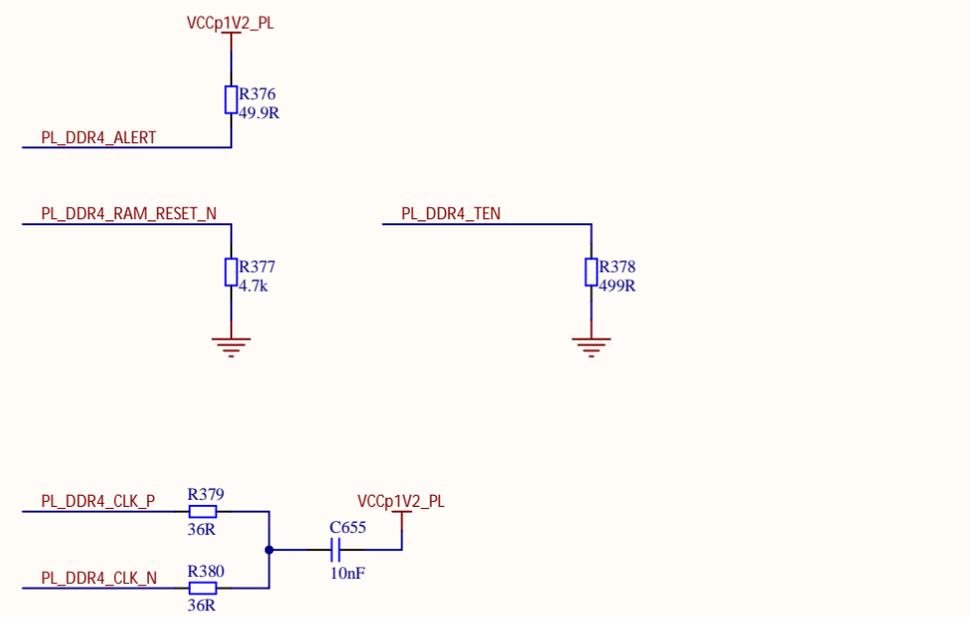
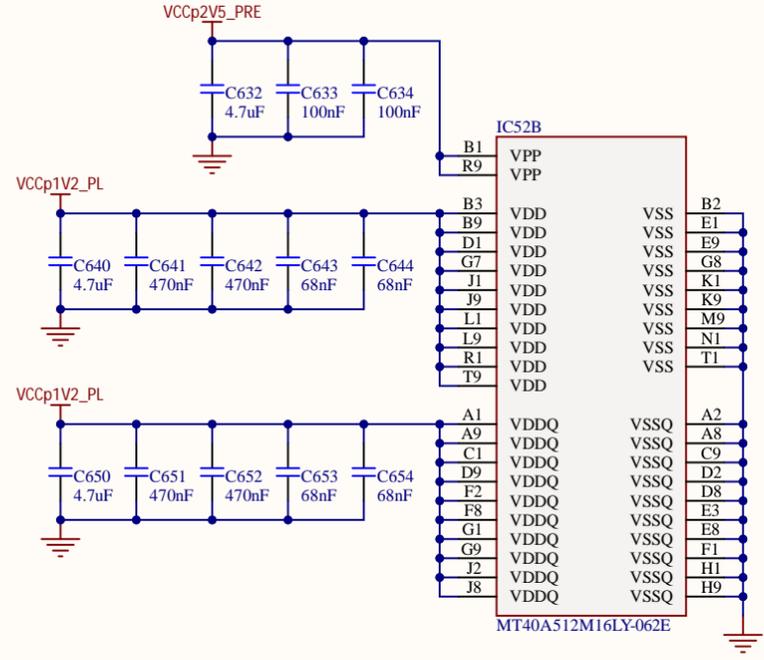
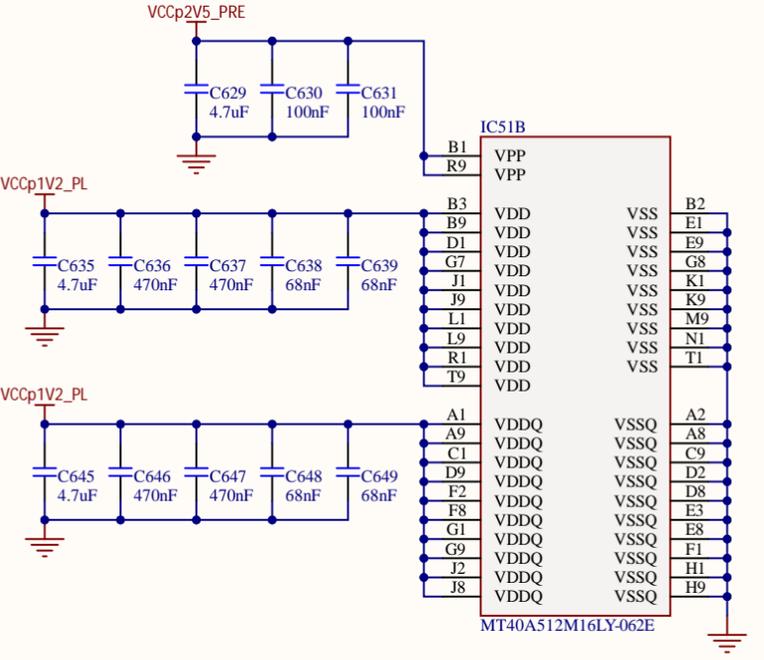
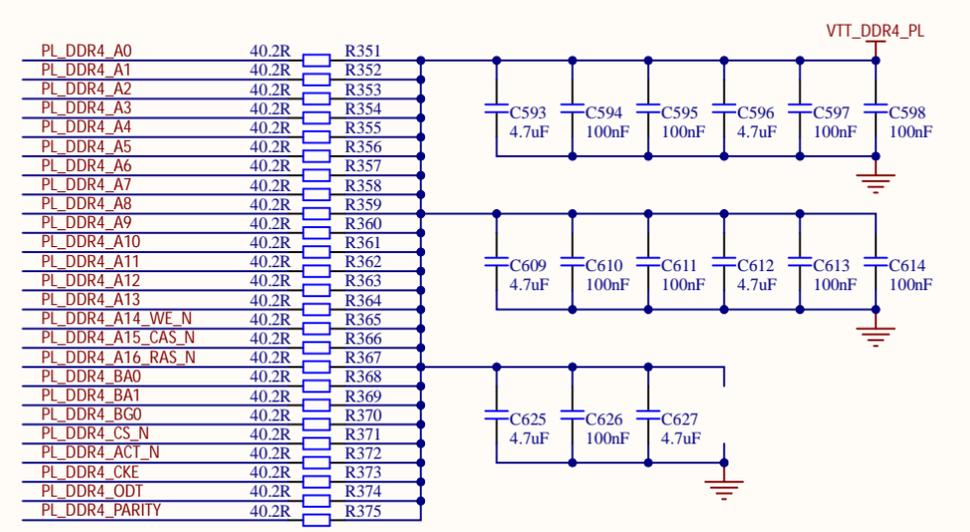
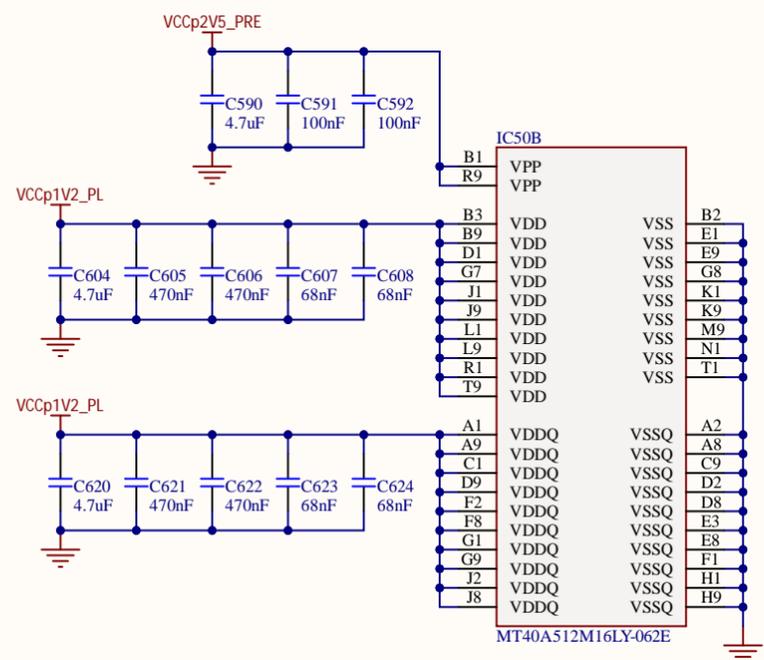
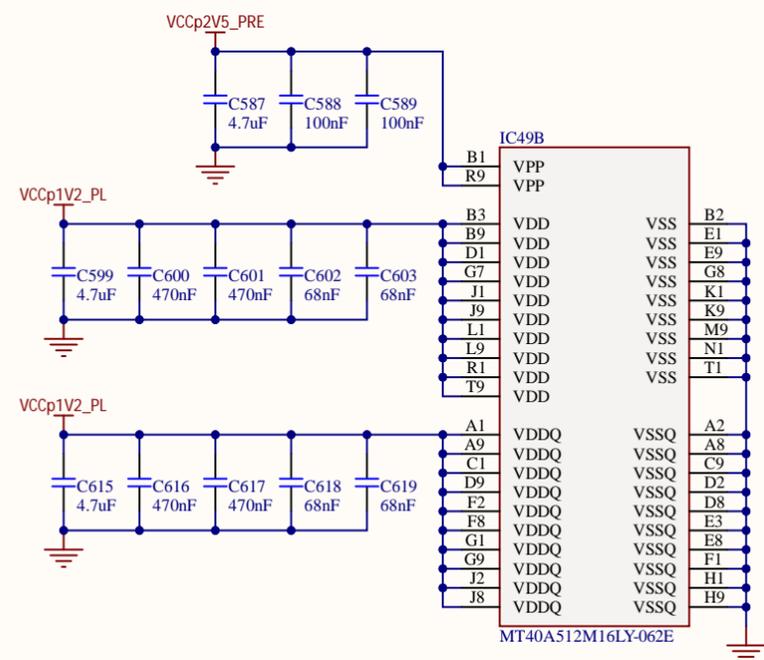


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| REAL DIGITAL | | © Xilinx 2021 | |
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| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3II | |
| Date: 5/23/2024 | Checked by: * | Sheet 33 of 46 | |

DDR4 MEMORY PL I



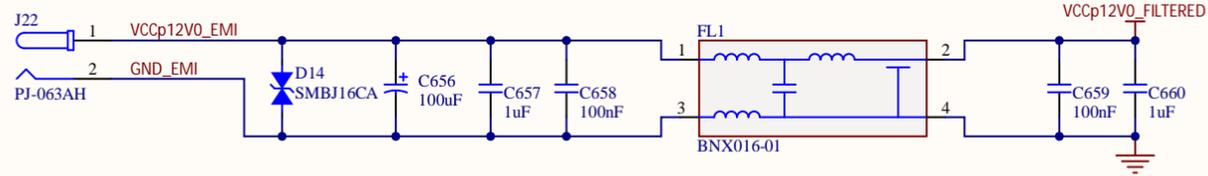
DDR4 MEMORY PL II



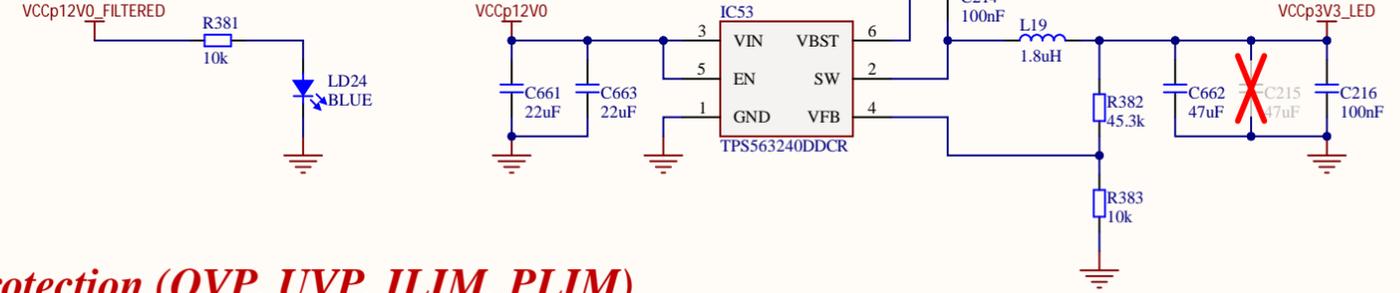
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [35] - DDR4 MEMORY PL II.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3II | |
| Date: 5/23/2024 | Checked by: * | Sheet 35 of 46 | |

POWER INPUT AND FAN CONTROLLER

EMI Filter

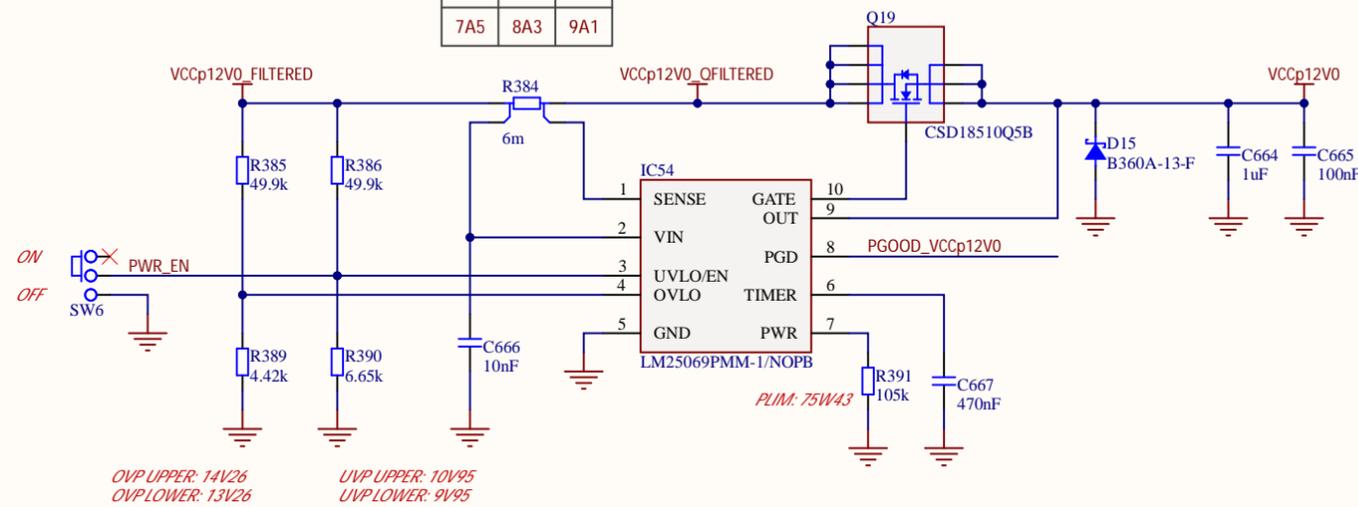


12V0 LED

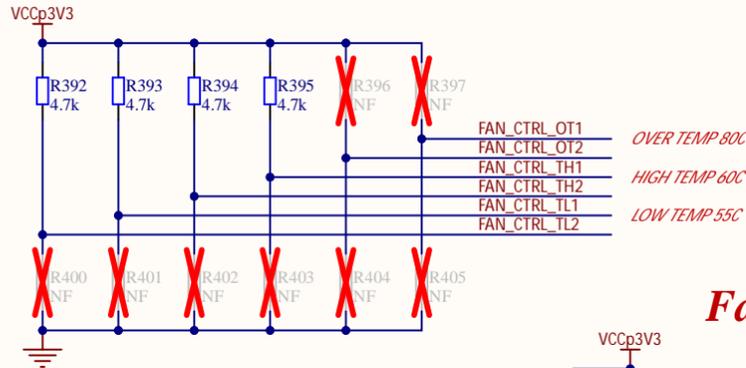


Input Protection (OVP, UVP, ILIM, PLIM)

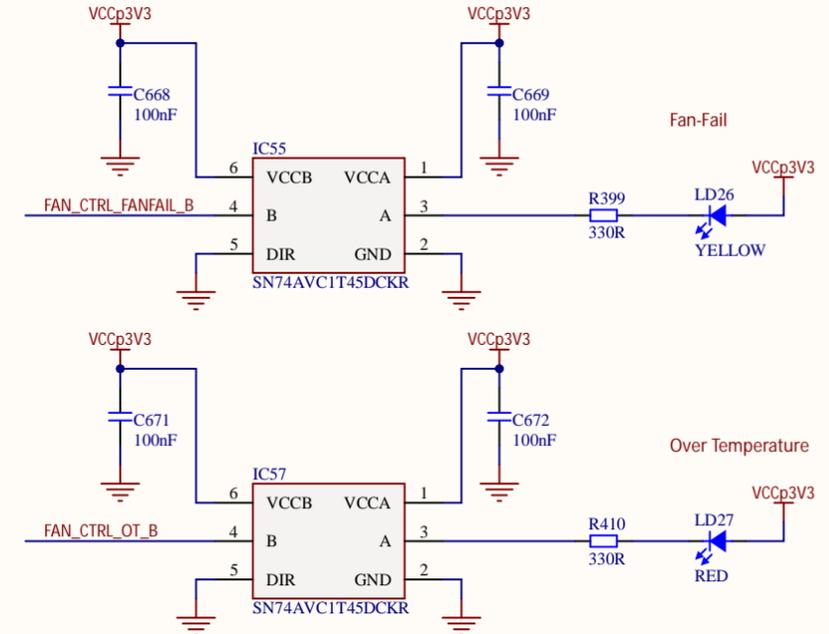
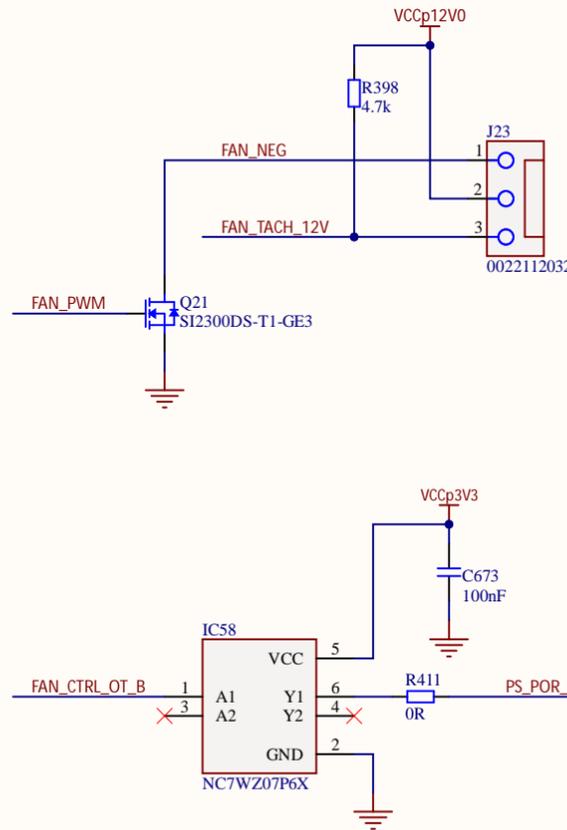
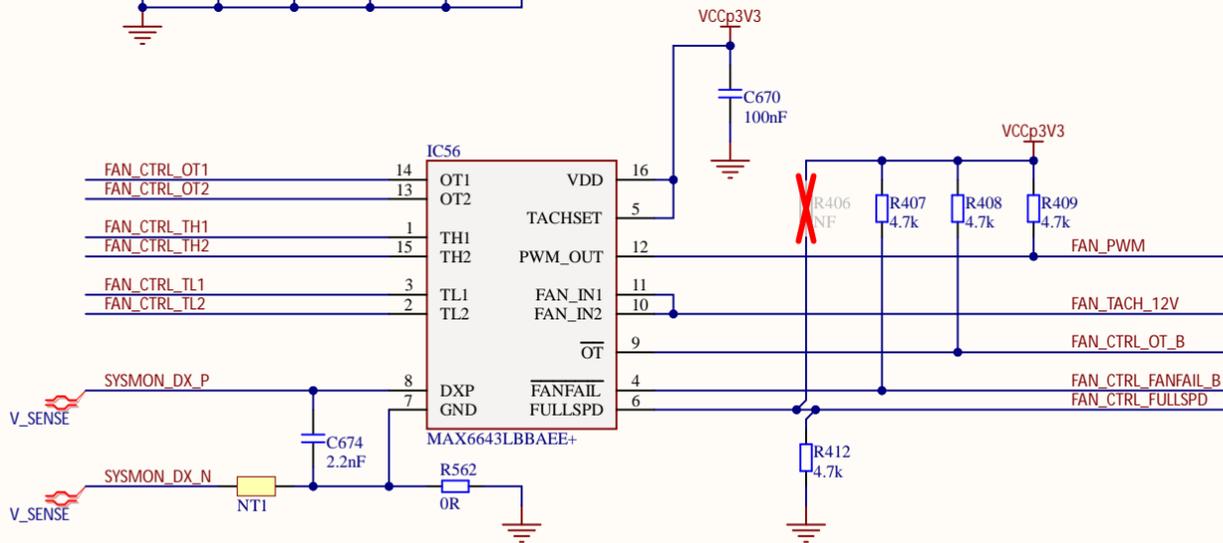
| Current Limit | | |
|---------------|-----|-----|
| MIN | TYP | MAX |
| 7A5 | 8A3 | 9A1 |



HS1
Heatsink+Fan
FA+K30B+T725

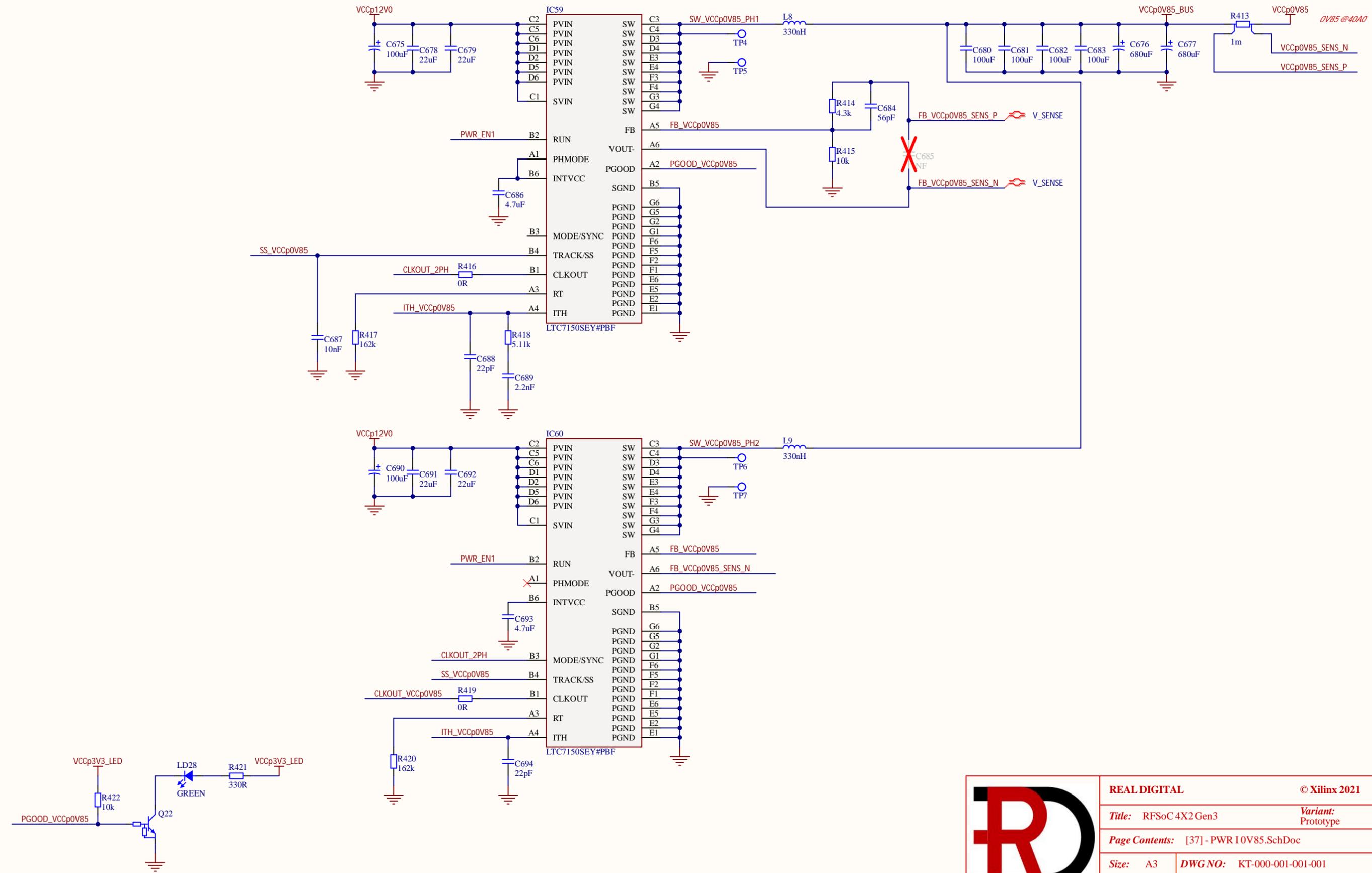


Fan Controller



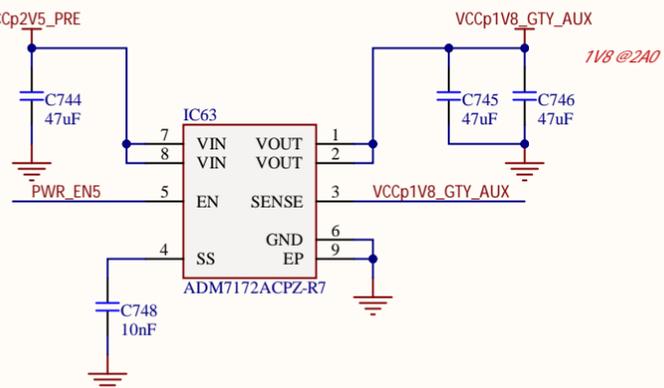
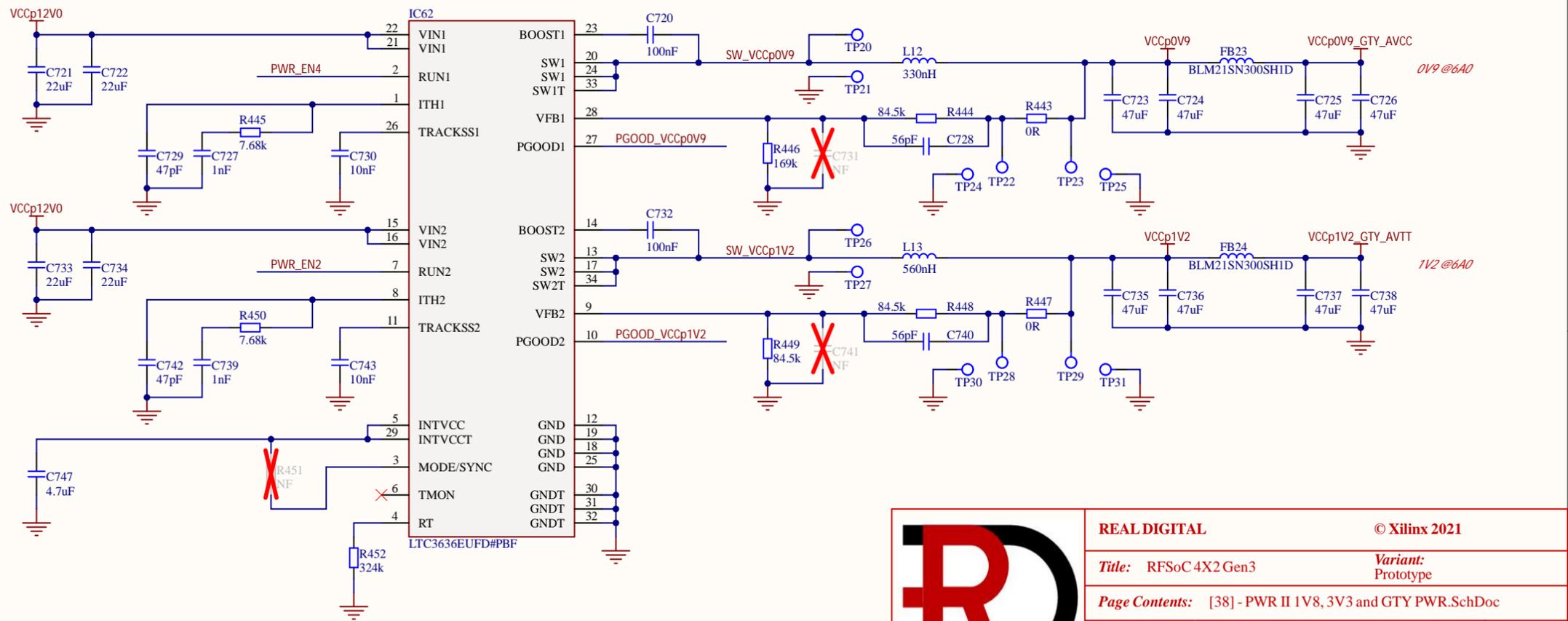
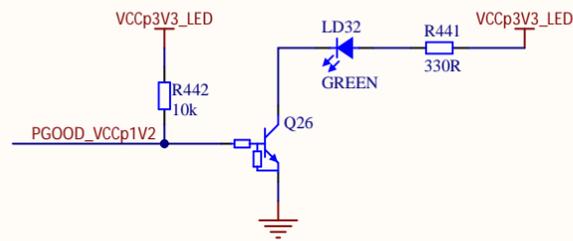
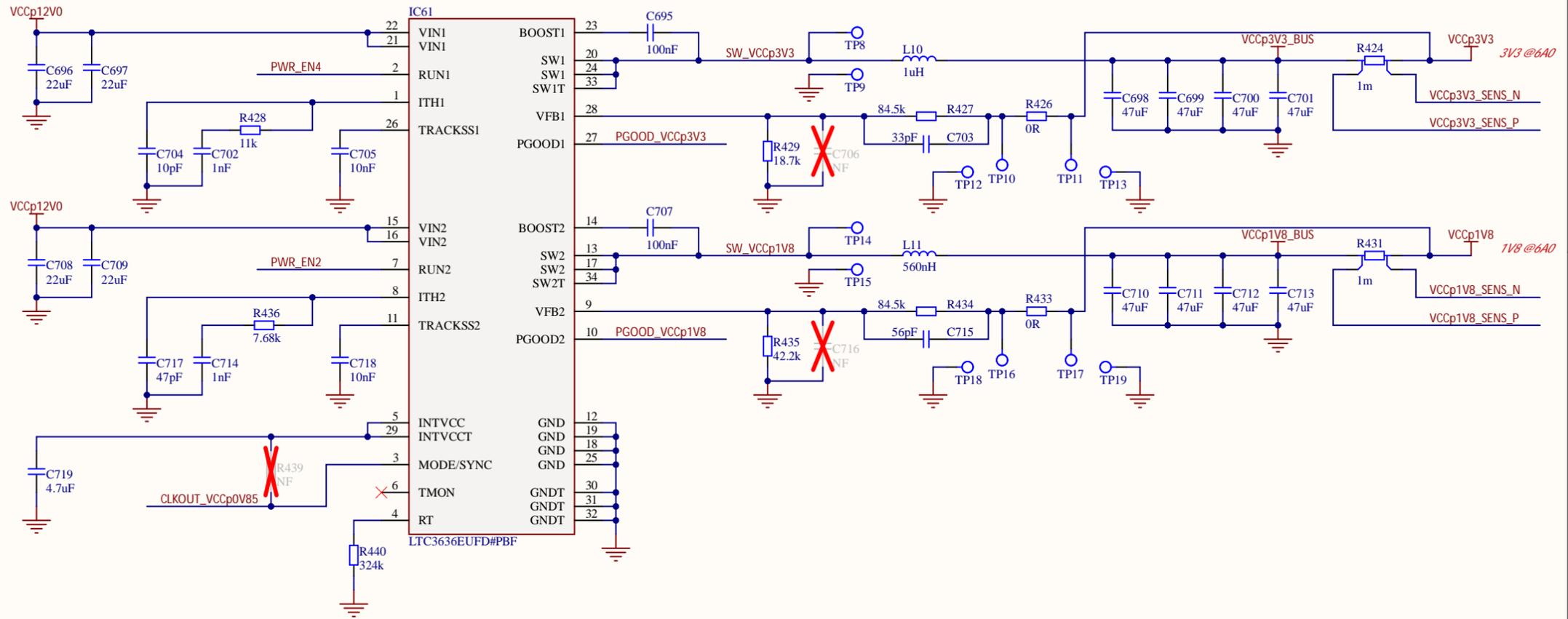
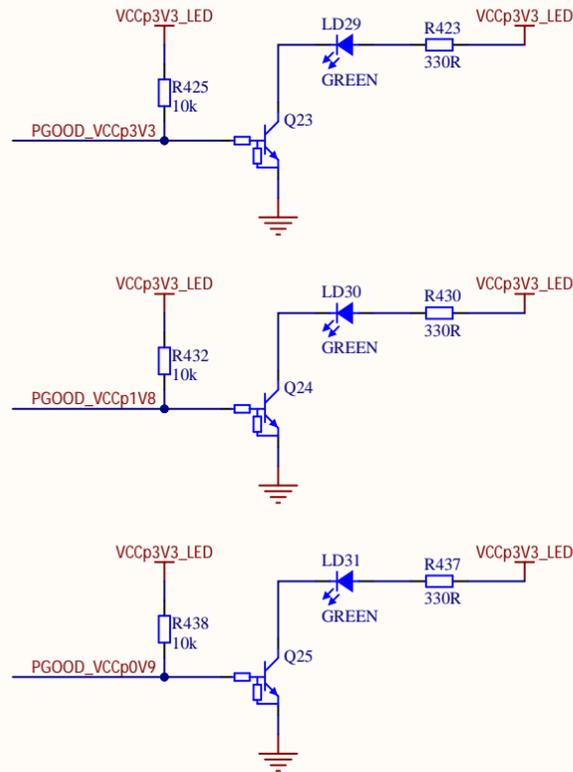
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [36] - PWR INPUT AND FAN CONTROLLER.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 36 of 46 | |

POWER I: VCCp0V85



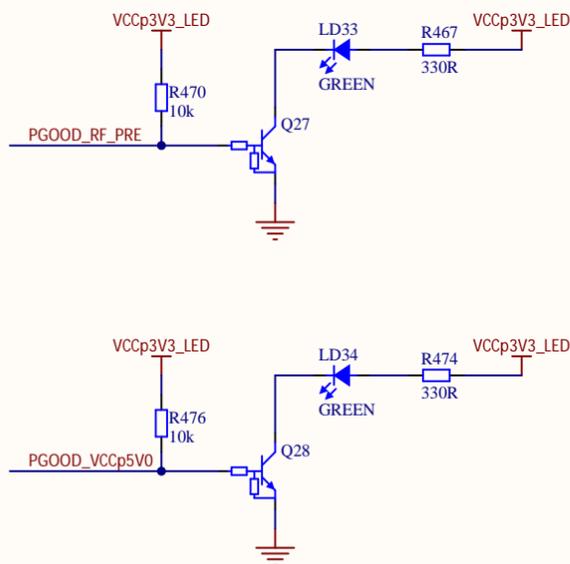
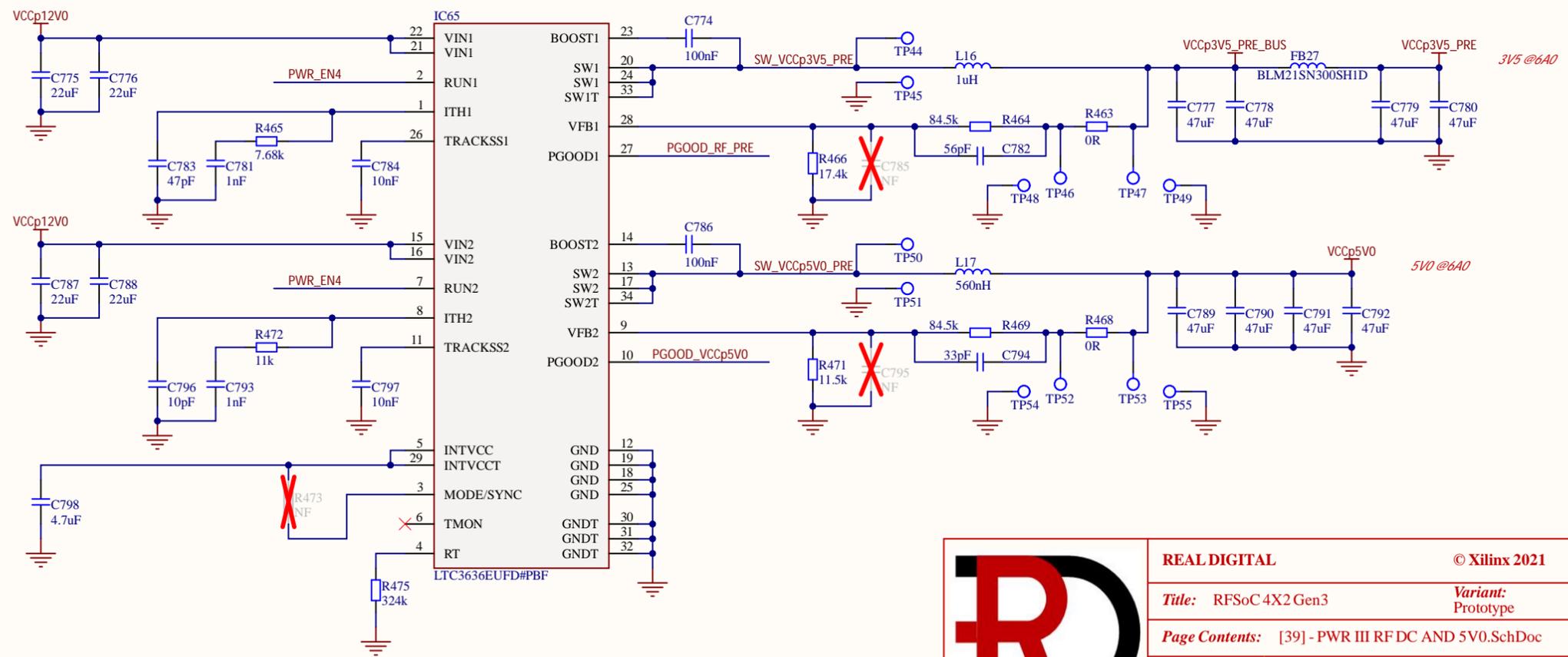
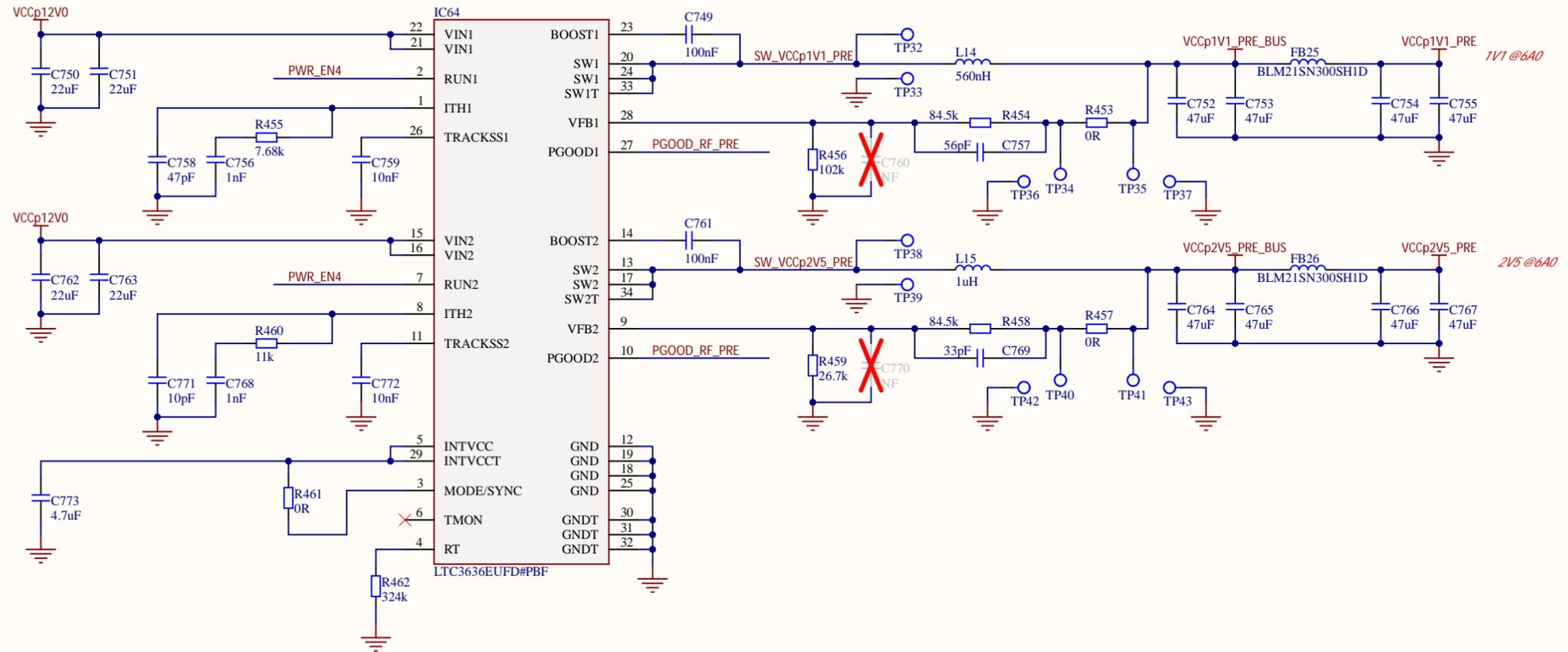
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| REAL DIGITAL | | © Xilinx 2021 | |
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| Page Contents: [37] - PWR I 0V85.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 37 of 46 | |

POWER II: VCCp1V8, VCCp3V3 and GTY PWR



| | | | |
|--|----------------------------|--------------------|--|
| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [38] - PWR II 1V8, 3V3 and GTY PWR.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3II | |
| Date: 5/23/2024 | Checked by: * | Sheet 38 of 46 | |

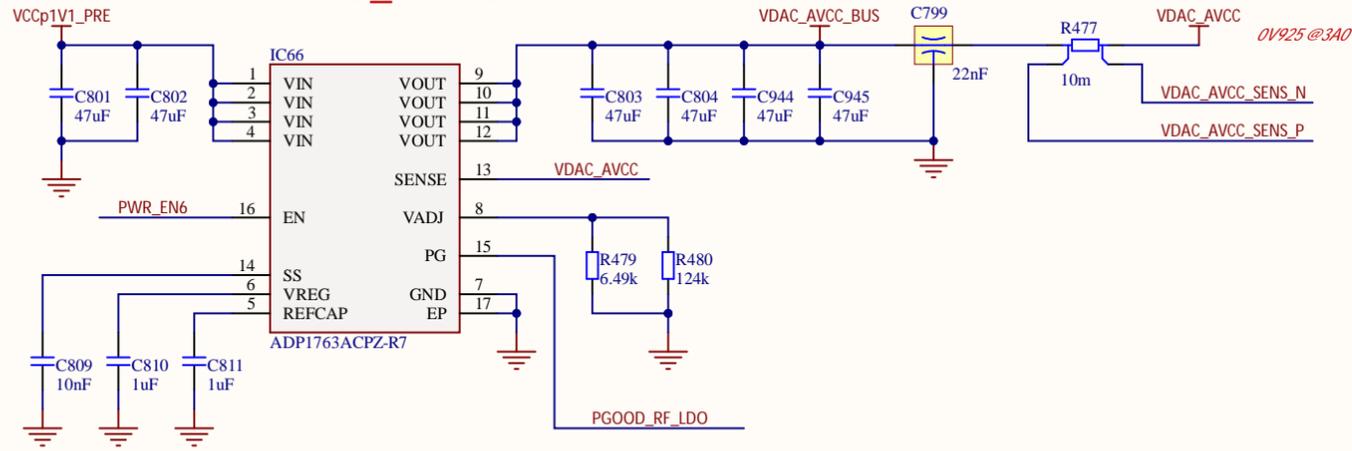
POWER III: RF DC/DC AND 5V0



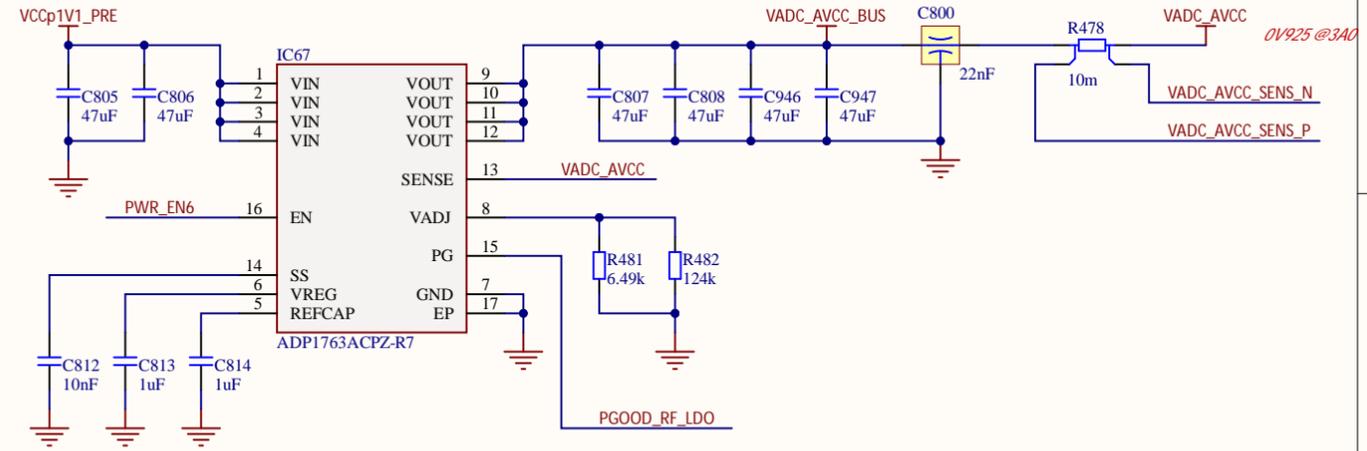
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoC 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [39] - PWR III RF DC AND 5V0.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 39 of 46 | |

POWER IV: RF LDO

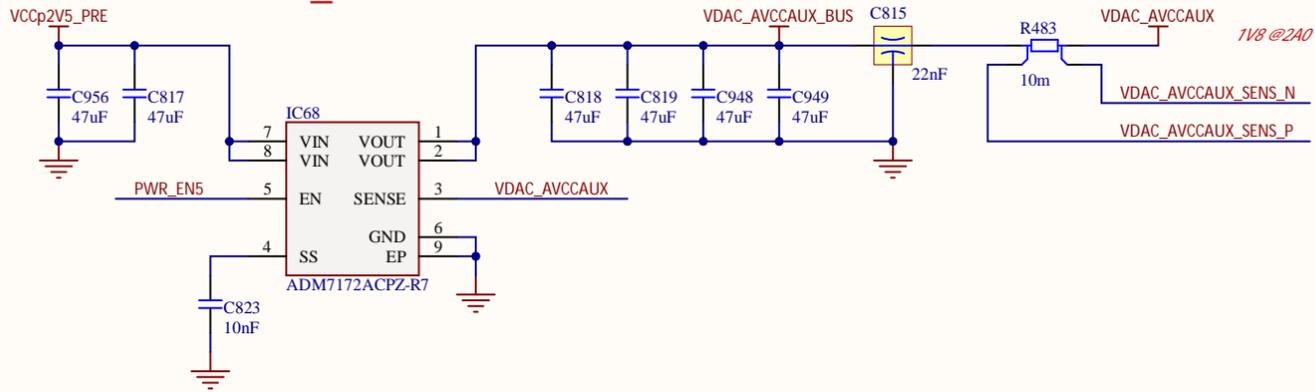
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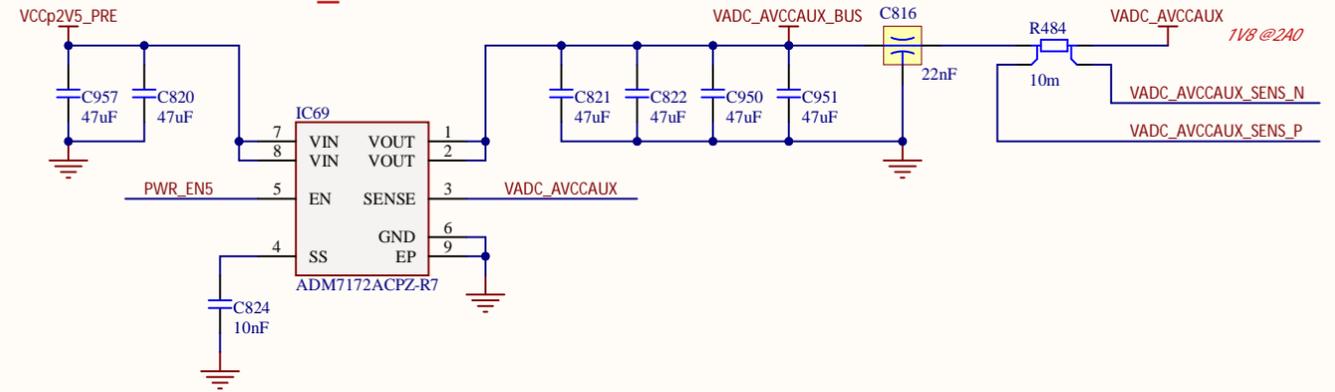
VADC_AVCC



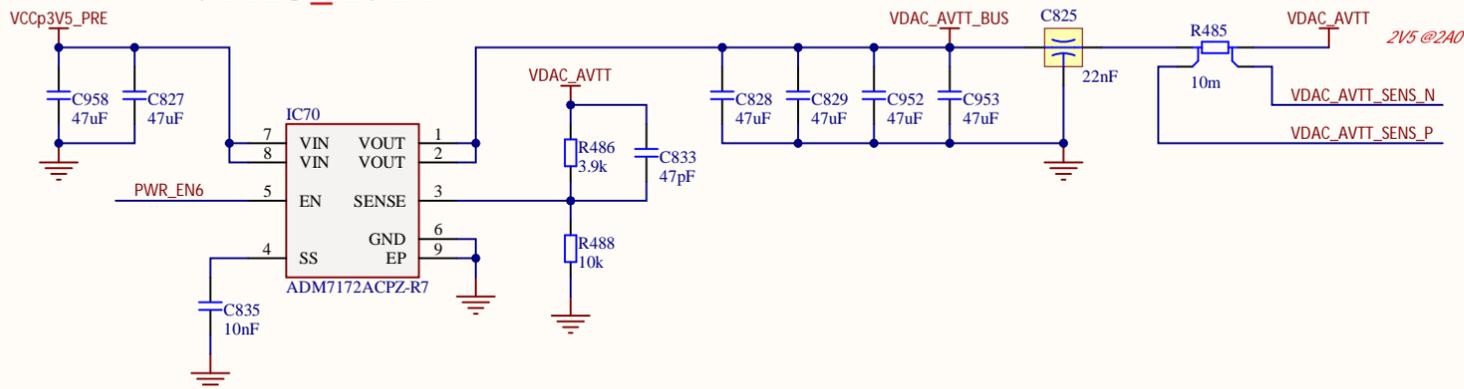
VDAC_AVCCAUX



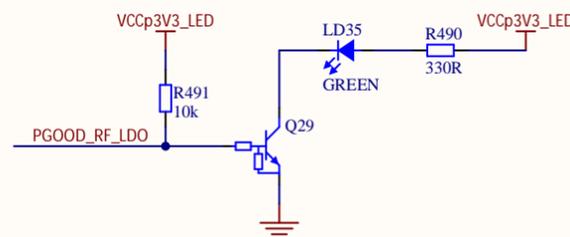
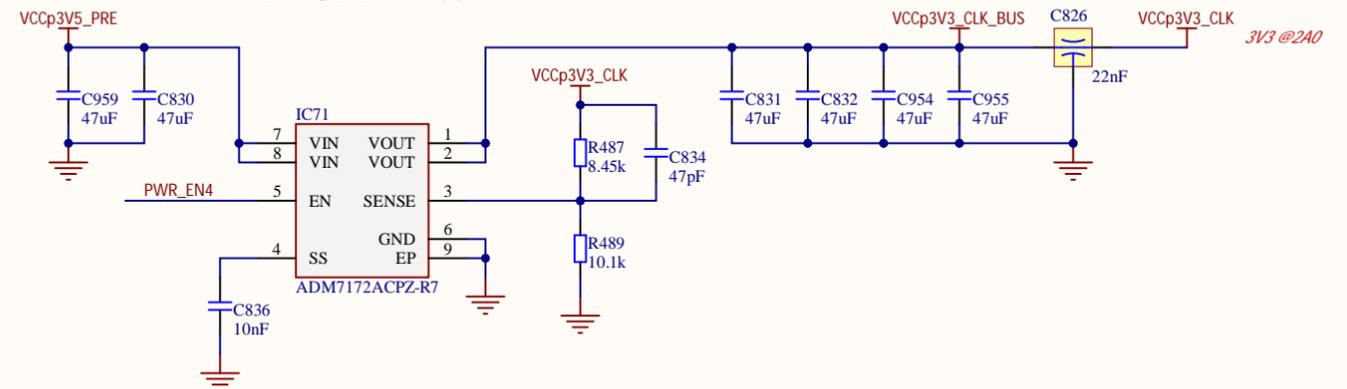
VADC_AVCCAUX



VDAC_AVTT

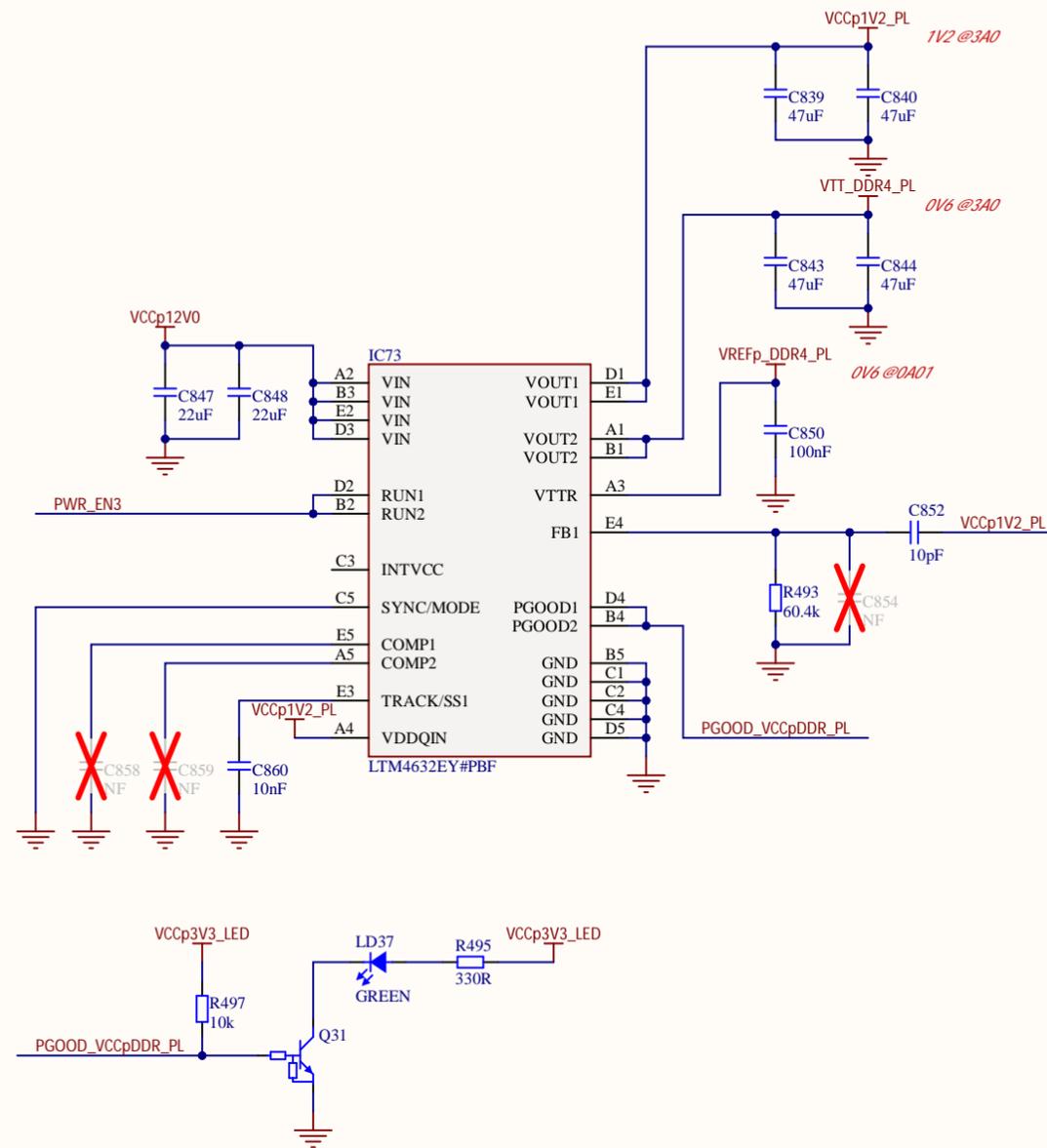
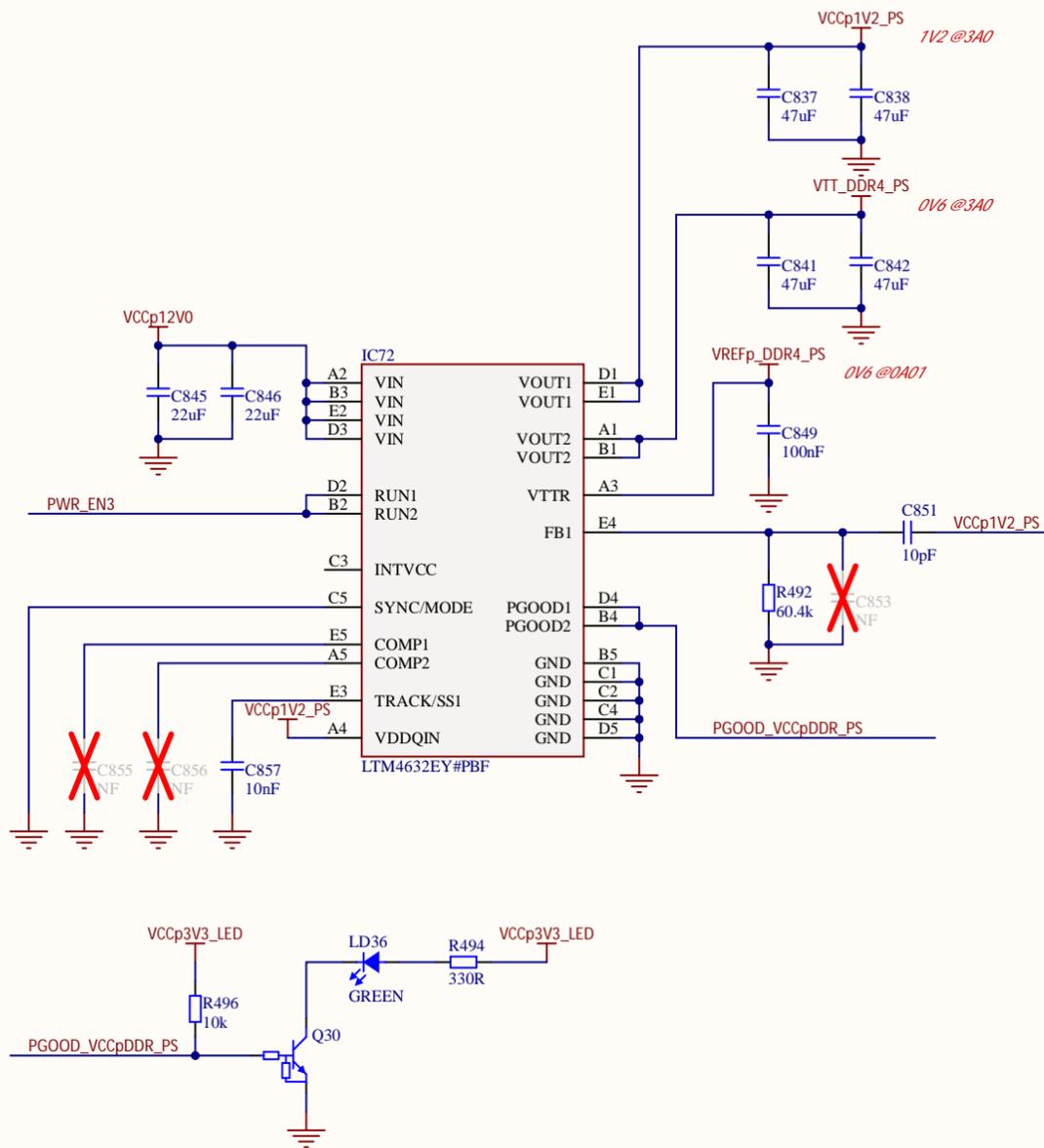


RF CLK PWR



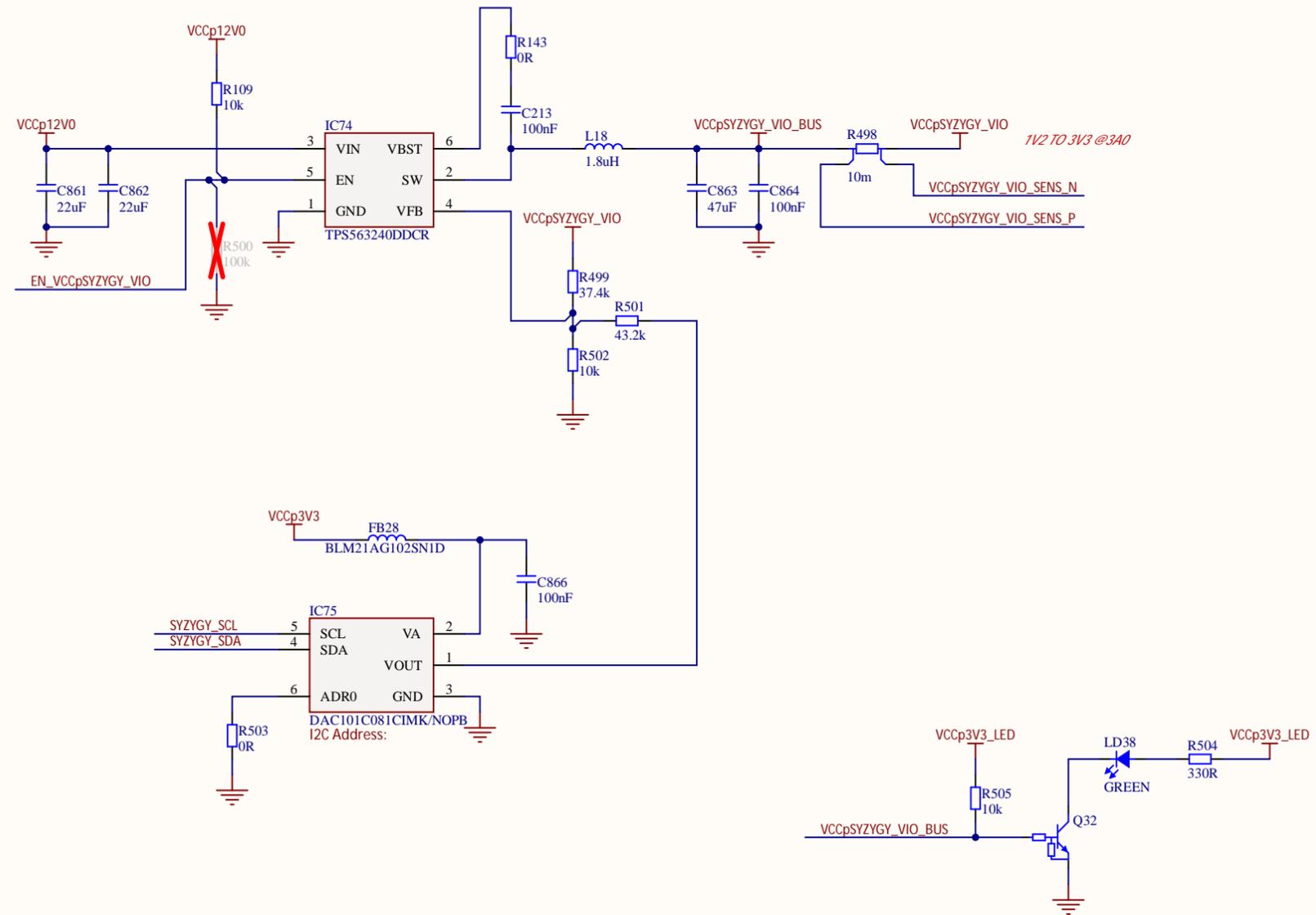
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| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [40] - PWR IV RF LDO.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 40 of 46 | |

POWER V: DDR4



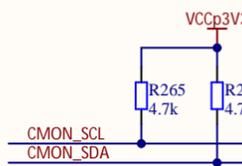
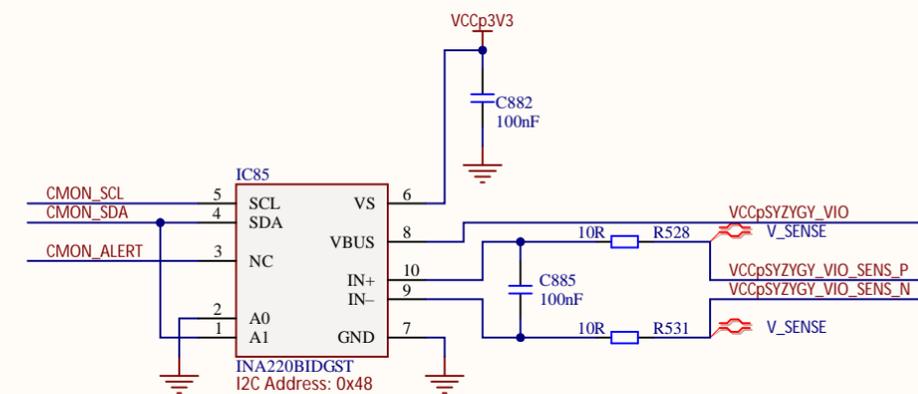
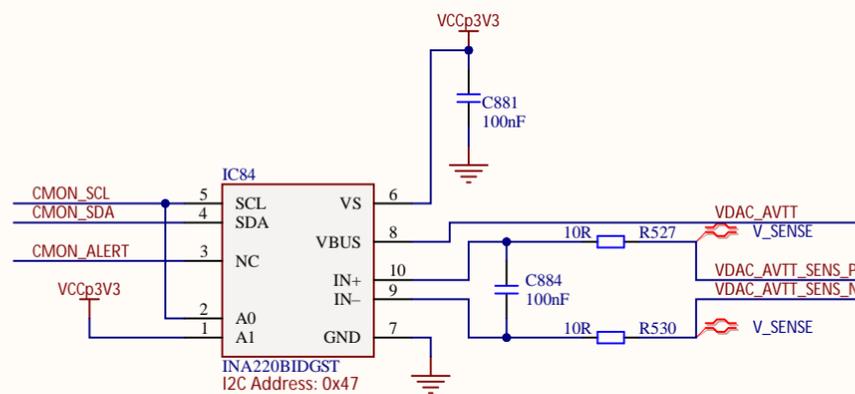
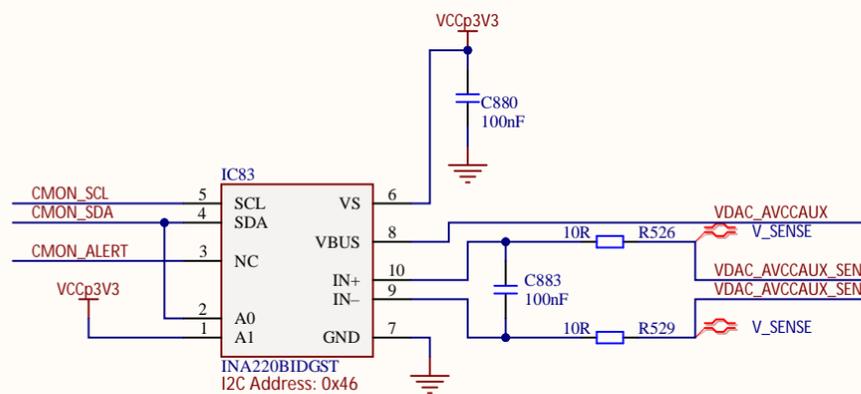
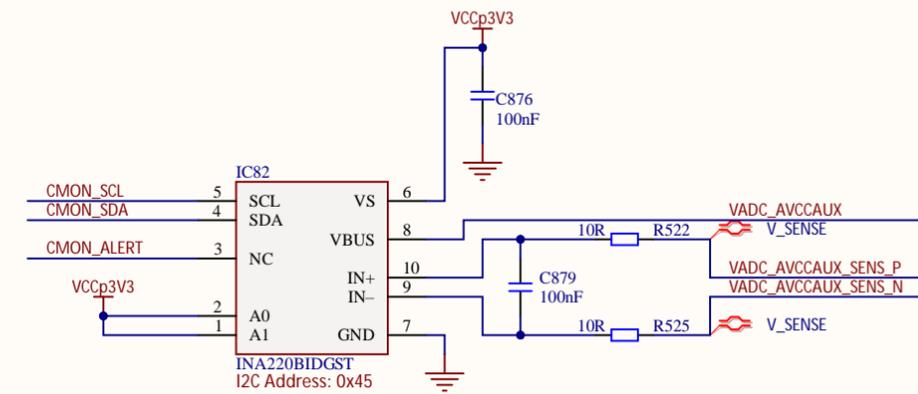
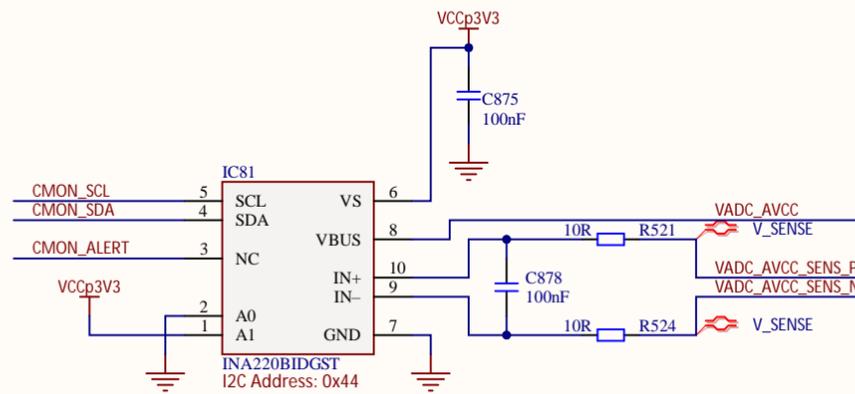
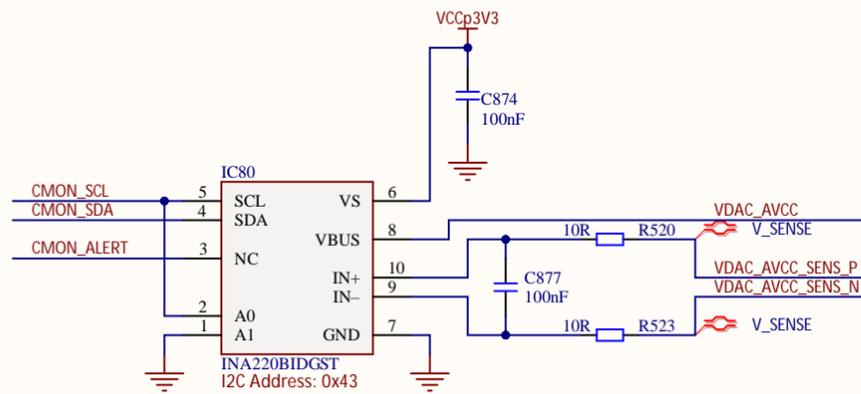
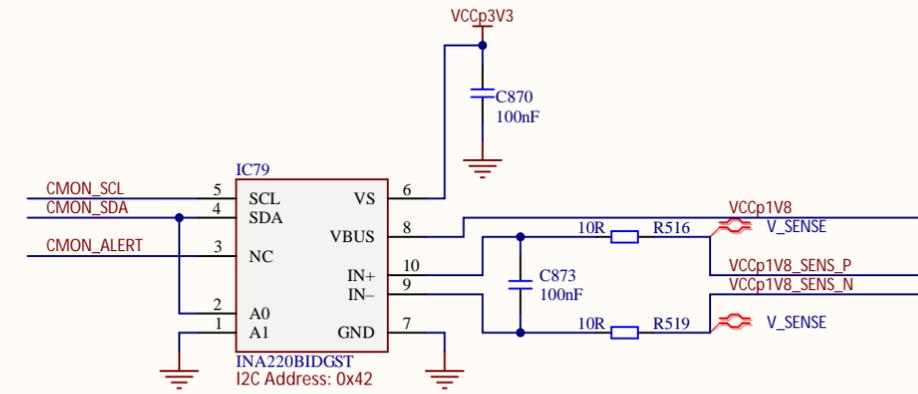
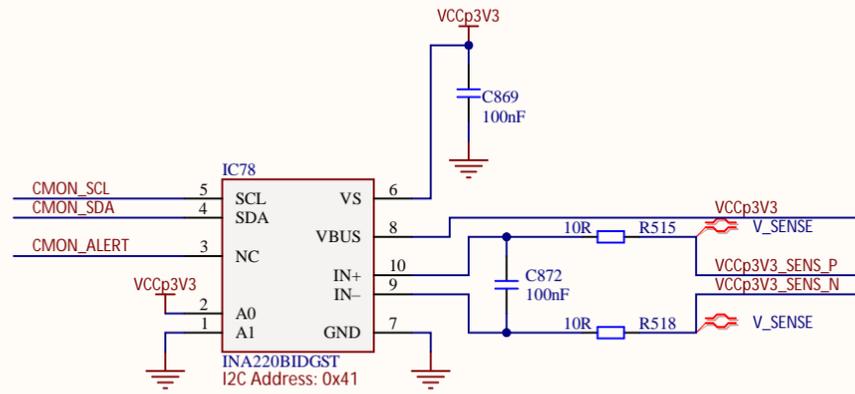
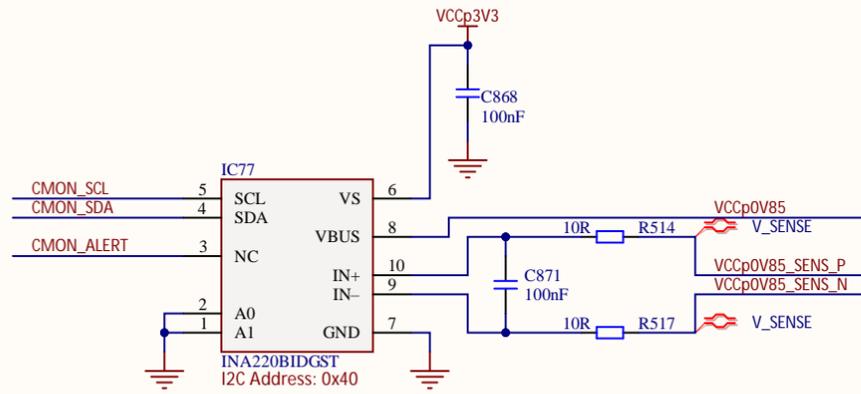
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|---|----------------------------|--------------------|--|
| REAL DIGITAL | | © Xilinx 2021 | |
| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [41] - PWR V DDR4.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 41 of 46 | |

POWER VI: SYZYGY



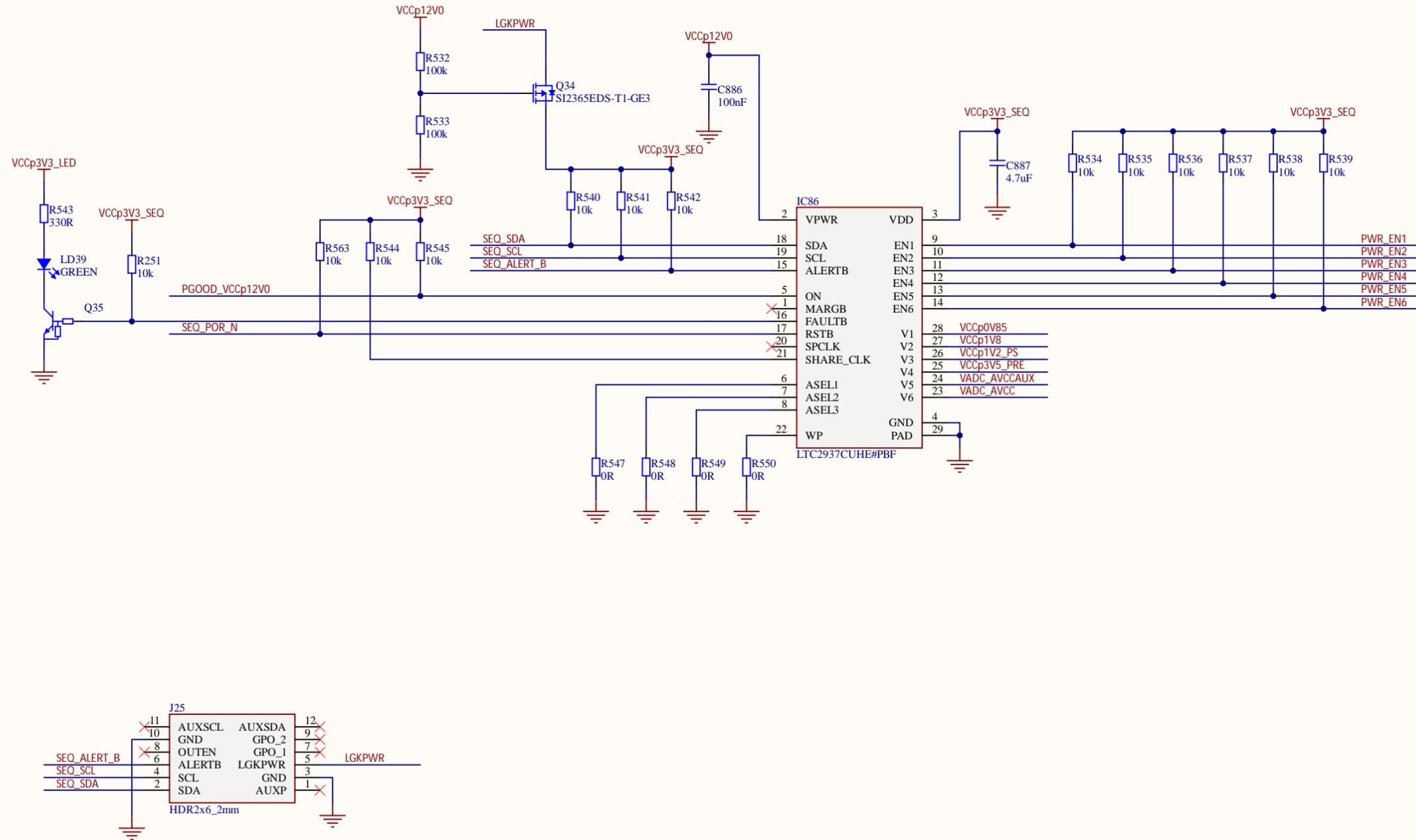
| | | | |
|---|----------------------------|--------------------|--|
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| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [42] - PWR VII SYZYGY.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 42 of 46 | |

CURRENT MONITOR



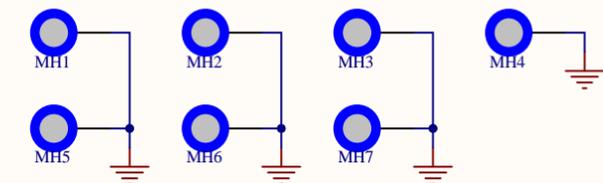
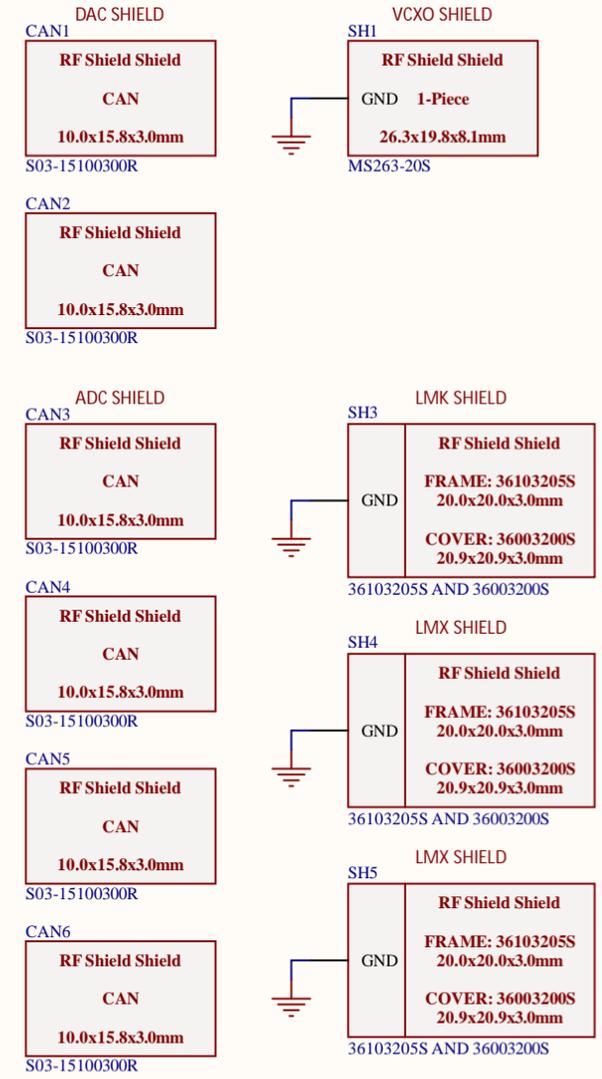
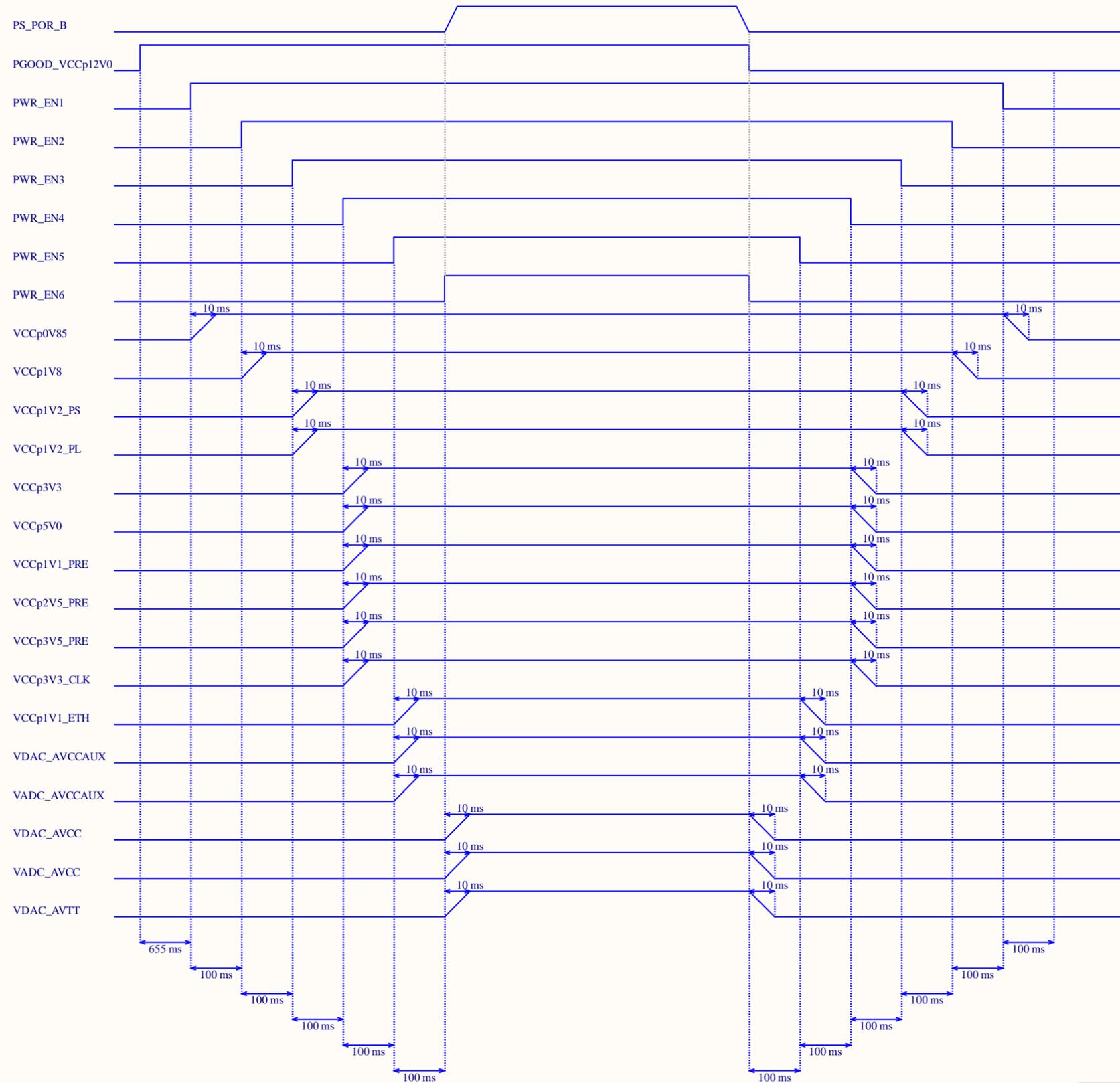
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|--|----------------------------|--------------------|--|
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| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [43] - CURRENT MONITOR.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 43 of 46 | |

SEQUENCER



| | | | |
|--|----------------------------|--------------------|--|
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| Title: RFSoc 4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [44] - SEQUENCER.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 44 of 46 | |

MECHANICAL AND POWER SEQUENCING



| | | | | | | |
|---|---|---|---|---|---|---|
| SC5 Screw, Phillips, M3, 6mm M3, 6mm STDF5 Standoff, M3, L:5.0mm 970050351 | SC6 Screw, Phillips, M3, 6mm M3, 6mm STDF6 Standoff, M3, L:5.0mm 970050351 | SC7 Screw, Phillips, M3, 6mm M3, 6mm STDF7 Standoff, M3, L:5.0mm 970050351 | SC8 Screw, Phillips, M3, 6mm M3, 6mm STDF8 Standoff, M3, L:5.0mm 970050351 | SC9 Screw, Phillips, M3, 6mm M3, 6mm STDF9 Standoff, M3, L:5.0mm 970050351 | SC10 Screw, Phillips, M3, 6mm M3, 6mm STDF10 Standoff, M3, L:5.0mm 970050351 | SC11 Screw, Phillips, M3, 6mm M3, 6mm STDF11 Standoff, M3, L:5.0mm 970050351 |
|---|---|---|---|---|---|---|

| |
|--------------|
| Real Digital |
| LG1 |
| AMD Xilinx |
| LG2 |
| PYNQ |
| LG3 |



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|--|----------------------------|--------------------|--|
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| Title: RFSoc4X2 Gen3 | | Variant: Prototype | |
| Page Contents: [45] - MECH AND PWR SEQUENCING.SchDoc | | | |
| Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V3I1 | |
| Date: 5/23/2024 | Checked by: * | Sheet 45 of 46 | |

DOC: REVISION HISTORY

Schematic:

V211

1. Update Title Block: "CONFIDENTIAL Do not distribute" and "CR 2021 REAL DIGITAL" from all schematic pages
2. Update Cover Page (Sheet 1)
3. Update Block Diagram (Sheet 2)
4. Update Power Diagram (Sheet 3)
5. Remove design notes (Sheet 4, Sheet 18, and Sheet 28)
6. Update POWER SEQUENCING diagram (Sheet 45)

Schematic and PCB

V211

1. Swap MIO33_UA1_RXD and MIO32_UA1_TXD (Sheet 20)
2. Change Sheet 12 name from "SD CARD" to "SD CARD AND EEPROM". Add the EEPROM memory AT24MAC402-MAHM-T connected to the Syzygy I2C bus.
3. Change the status for the resistors connected to SPI_CLK/SMCLK (38) and SPI_DO/SMDAT (39) to "No Load" (Sheet 9, USB5742/2G).
4. Change the status for the capacitors connected to VCM01_224 (AL5), VCM23_224 (AL4), VCM01_226 (AJ5), and VCM23_226 (AJ4) to "NoLoad" (Sheet 27).
5. Rename the net between the power supply sequencer IC86.17 and the OLED display DISP1.8 to be SEQ_POR_N and add a pull-up resistor (10k) to Vccp3v3_SEQ on SEQ_POR_N (Sheet 44).
6. Connect SEQ_POR_N to NVT2008BQ level shifter pin B6 and connect PS_POR_N to NVT2008BQ level shifter pin A6 (Sheet 14).
7. Change the status for the pull-up resistor connected to PS_POR_N to "Load" (Sheet 19).
8. Change DDR4 memory part number from "MT40A512M16JY-083E" to "MT40A512M16LY-062E".
10. Add the AC decoupling capacitors for the RF clocks.
11. Remove the 3dB attenuator for the external input reference clock.
12. Increase the output capacitance for the LDOs (Sheet 40).
13. Silkscreen changes:
 - Remove the QR Code;
 - Change the Xilinx logo to be AMD_Xilinx;
 - Add PYNQ logo;
 - Change "USD DEVICE" to "USB DEVICE";
 - Add labels for the programming headers: JTAG, SI5395 PROG, SEQ PROG, CLK PROG
 - Change DAC0, DAC1, ADC0, ADC1, etc. to DAC_A, DAC_B, ADC_A, ADC_B, etc.
14. Add 200k pull-up resistors connected for the NVT2008BQ "EN" pin, update "VREFB" connection, and add pull-ups on the B side of the level translators. (Sheet 05 - 3 ICs, Sheet 10 - 1 IC, Sheet 14 - 1 IC)
15. Increase the input capacitance for the ADM7172ACPZ-R7 LDOs (Sheet 40).
16. Update the USB3.0 Slave connector schematic symbol and footprint (Sheet 8).
17. Increased the value of the resistors to reduce the brightness of the white and RGB user LEDs
 - Change R2, R3, R4, and R5 resistors values from 330R to 1k
 - Change R16, R20, R24, and R26 resistors values from 86R6 to 270R
 - Change R16, R20, R24, and R26 resistors values from 150R to 470R

V212

1. Add a pull-up resistor connected to the enable pin of the Syzygy power supply (IC74) - add R109 (10k) and change R500 to NF.

V311

1. Update Sheet 9 USB 3.0 HOST.

| | | | |
|---|--|-----------------------------------|---------------------------|
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| | Page Contents: [46] - DOC REVISION HISTORY.SchDoc | | |
| | Size: A3 | DWG NO: KT-000-001-001-001 | Revision: V311 |
| Date: 5/23/2024 | Checked by: * | Sheet 46 of 46 | |