Digital Logic Problem Set #2

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1. (20 points) Complete the truth tables below.

A	B	F

AND

A	B	F

OR

A	B	F

XOR

A	F

INV

2. (8 points) Sketch non-minimized SOP and POS circuits for the truth table below.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

3. (20 points) Complete the truth tables and provide minterm equations.

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

$$F = \overline{A} \cdot B + C$$

F <= ∑ ( )

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

$$F = A \cdot B \cdot \overline{C} + B \cdot C$$

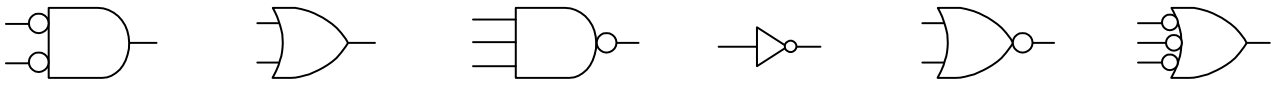
F <= ∑ ( )

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

$$F = B \cdot \overline{C} + \overline{B} \cdot C$$

F <= ∑ ( )

4. (12 points) Write the number of transistors required for each logic gate below inside the gate symbol, and then write the logic gate name below the symbol.



5. (10 points) Complete the following truth table based on the Verilog assignment statement below, and write minterm and maxterm equations for F.

assign F = (A & ~ B) | (~A & ~C) | (A & B & C);

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

6. (12 points) Sketch circuits and write Verilog assignment statements for the following logic equations.

$$F = \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot C$$

$$F = \overline{\overline{A} \cdot B \cdot \overline{C}} + \overline{A + B}$$

$F = (A + \bar{B}) \cdot \overline{\overline{B + C} \cdot \bar{A}}$

F = ∑m(1, 2, 6)

F = ∏M(0, 7)

7. (20 points) In a logic function with n inputs, there are 2^n unique combinations of inputs and 2^{2^n} possible logic functions. The table below has four rows that show the four possible combinations of two inputs ($2^2 = 4$), and 16 output columns that show all possible two-input logic function ($2^{2^2} = 16$). Six of these output columns are associated with ***common logic functions of two variables***. Circle the six columns, and label them with the appropriate **logic gate name**. Draw the circuit symbols for the functions represented.

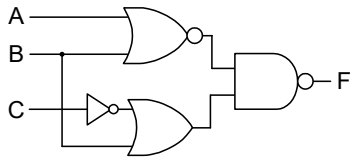
INPUTS		ALL POSSIBLE FUNCTIONS															
A	B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

A table like the one above for 3 inputs would need _____ rows and _____ columns.

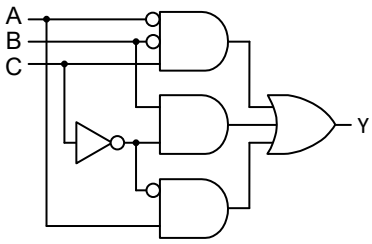
A table like the one above for 4 inputs would need _____ rows and _____ columns.

A table like the one above for 5 inputs would need _____ rows and _____ columns.

8. (12 points) Complete truth tables for the circuits shown below.

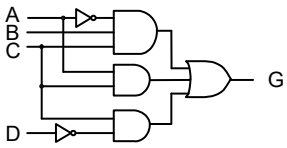


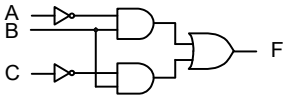
A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

9. (18 points) Show the total transistor count and gate/input number for the circuits below. Then sketch equivalent circuits using NAND gates that use fewer transistors (do not minimize the circuits).





10. (10 points) Simplify the following using Boolean algebra

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assign Y = (A & B & ~C & D) | (A & C) | (~C & ~D) | (A & ~B & ~C & D) | (~A & C)
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$$Y <= \overline{A \bullet B} + \overline{B + C} + \overline{B}$$

11. (12 points) Timing diagrams show circuit inputs and outputs as they change over time. In the figure below, the signals A and B come from pushbuttons that are pressed at different times (in the first time slice, neither A or B are pressed, in the second time slice, B is pressed but A is not, etc.). Complete the timing diagrams to show how the various logic gates respond to their inputs.