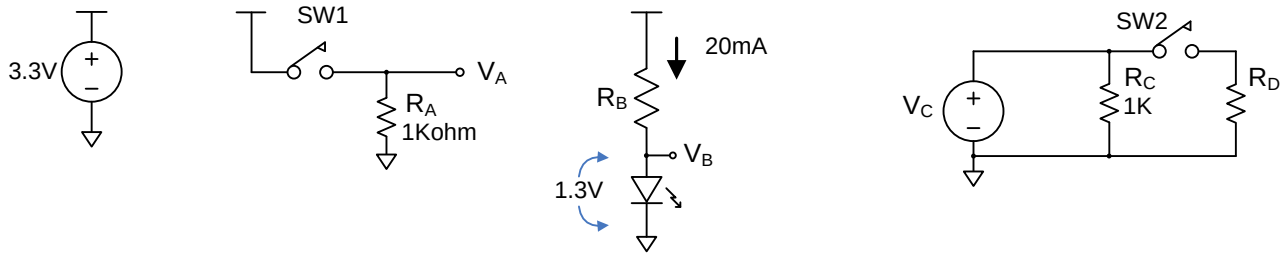
Problem Set #1

Revision: 2/3/19

RealDigital

1. (15 points) Below are some circuit elements from a simple digital system.

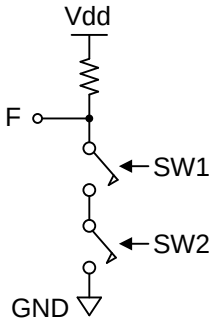


When the pushbutton SW1 is not pressed, what is the voltage at V_A?	(1pt)	
When the SW1 is pressed, what is the voltage at V_A?	(1pt)	
When the SW1 is pressed, what current flows in the 1K resistor R_A?	(1pt)	
When SW1 is pressed, what power is dissipated in R_A?	(2pt)	
In the LED circuit, 1.3V is required at V_B to forward-bias the LED and cause current to flow. Given there is a 1.3V drop across the LED, what resistance R_B is required for 20mA to flow through the LED?	(2pt)	
What power is dissipated in the LED?	(1pt)	
In the circuit on the far right, if R_C dissipates 25mW, what is V_C?	(2pt)	
Using the V_C voltage you calculated, if R_C is changed to 100Ohms, how much power would it dissipate?	(2pt)	
Using the V_C voltage you calculated and a 1K R_C, if pressing SW2 causes the total circuit power to increase to 75mW, what value must R_D be?	(3pt)	

2. (22 points) The example circuit below asserts its output as a logic 0 when both switches are closed. Based on your reasoning for how this example circuit works, sketch a different circuit that asserts logic 1 when both switches are closed. Label the switches 1 and 2, and complete the truth table for your circuit. Then circle the correct term (high or low, and open or closed) to complete the following sentences describing the AND and OR relationships for your circuit:

AND Relationship:
The output F is [high / low] when SW1 is [open / closed], ***and*** SW2 is [open / closed].

OR Relationship:
The output F is [high / low] when SW1 is [open / closed], ***or*** SW2 is [open / closed].

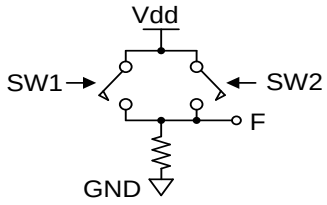


SW1	SW2	F

The example circuit below asserts its output as a logic 1 when either switch is closed. Sketch a new circuit that asserts logic 0 whenever one or both switches are closed. Label the switches 1 and 2, and complete the truth table below. Circle the correct term (high or low, and open or closed) to complete the following sentences describing the AND and OR relationships for your circuit:

AND Relationship:
The output F is [high / low] when SW1 is [open / closed], ***and*** SW2 is [open / closed].

OR Relationship:
The output F is [high / low] when SW1 is [open / closed], ***or*** SW2 is [open / closed].

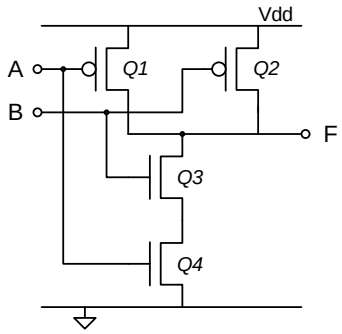


SW1	SW2	F

3. (4 points) Complete the following.

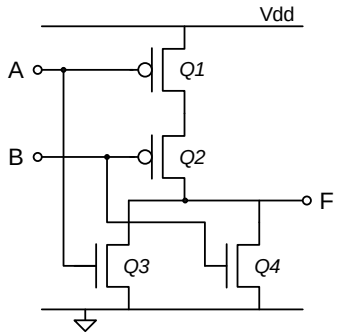
A pFET turns [ON / OFF] with LLV and conducts [LHV / LLV] well (circle one in each bracket).
An nFET turns [ON / OFF] with LLV and conducts [LHV / LLV] well (circle one in each bracket).

4. (20 points) Complete the truth tables below (enter “on” or “off” under each transistor entry, and “1” or “0” for output F), and enter the gate name and schematic shapes in the tables.



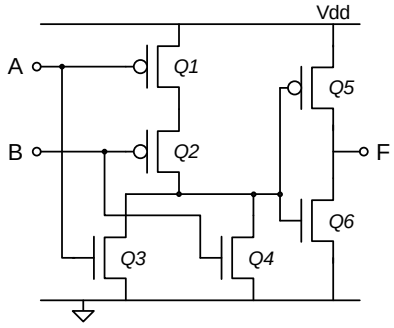
A	B	Q1	Q2	Q3	Q4	F
0	0					
0	1					
1	0					
1	1					

Gate Name	
AND shape	OR shape



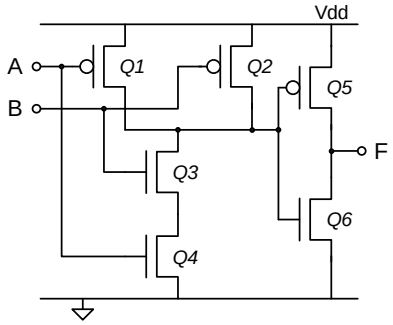
A	B	Q1	Q2	Q3	Q4	F
0	0					
0	1					
1	0					
1	1					

Gate Name	
AND shape	OR shape



A	B	Q1	Q2	Q3	Q4	F
0	0					
0	1					
1	0					
1	1					

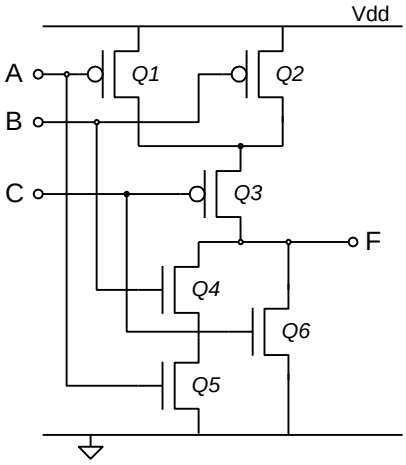
Gate Name	
AND shape	OR shape



A	B	Q1	Q2	Q3	Q4	F
0	0					
0	1					
1	0					
1	1					

Gate Name	
AND shape	OR shape

5. (10 points) Complete the truth table below (enter “on” or “off” under each transistor entry, and “1” or “0” for output F). Then, provide a logic equation for the circuit in the box below.



A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	F
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

F =

6. (12 points) Based on your knowledge of what a two-input NAND circuit and a two-input NOR circuit built from pFETs and nFETs look like, sketch a three-input NAND and four-input NOR circuit.

7. (8 points) The picture below shows a representation of a logic gate built from FETs as it might appear to a chip designer in a CAD/layout tool. The reddish polysilicon areas labeled A and B are conductive materials that form the circuit inputs, and the yellow and green areas are "diffusion" areas that have been implanted (or doped) with materials to make them more positive or more negative than the surrounding silicon. Based on your knowledge of CMOS gate structures, answer the following.

Which number points to the positive diffusion area?

Which number points to the negative diffusion area?

The dotted-line box pointed to by #3 represents what type of FET?

What number points to the circuit output?

What type of logic gate is this?