

PROJECT 6: CIRCUIT DELAYS AND GLITCHES

Digital Logic Project Submission Form

Revision: 2/3/19

I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Point Scale

- 4: Exemplary
- 3: Complete
- 2: Incomplete
- 1: Minor effort
- 0: Not submitted

 Print Name

 Sign Name

 Date

| # | Deliverable | Wt | Pts | Date | Asst. Signature |
|--|--------------------------------|----|-----|------|-----------------|
| Requirements | | | | | |
| 1: Simulate Circuit and Show Glitch | | | | | |
| | Program demo | 2 | | | |
| | Verbal questions answered well | 2 | | | |
| 2: Change OR Gate delay and simulate | | | | | |
| | Program demo | 3 | | | |
| | Verbal questions answered well | 3 | | | |
| 3: Change delay of all gates and simulate | | | | | |
| | Program demo | 3 | | | |
| | Verbal questions answered well | 3 | | | |
| Challenges | | | | | |
| 1: Delay in decoder | | | | | |
| | Program demo | 3 | | | |
| | Verbal questions answered well | 3 | | | |
| Extensions | | | | | |
| 1: Describe | | | | | |
| | Program demo | | | | |
| | Verbal questions answered well | | | | |
| Homework Problems | | | | | |
| 1 | Show SOP glitch | 8 | | | |
| 2 | Remove SOP glitch | 4 | | | |
| 3 | Show POS glitch | 8 | | | |
| 4 | Remove POS glitch | 4 | | | |
| 5 | Remove glitches from equations | 8 | | | |