Digital Logic Problem Set #4

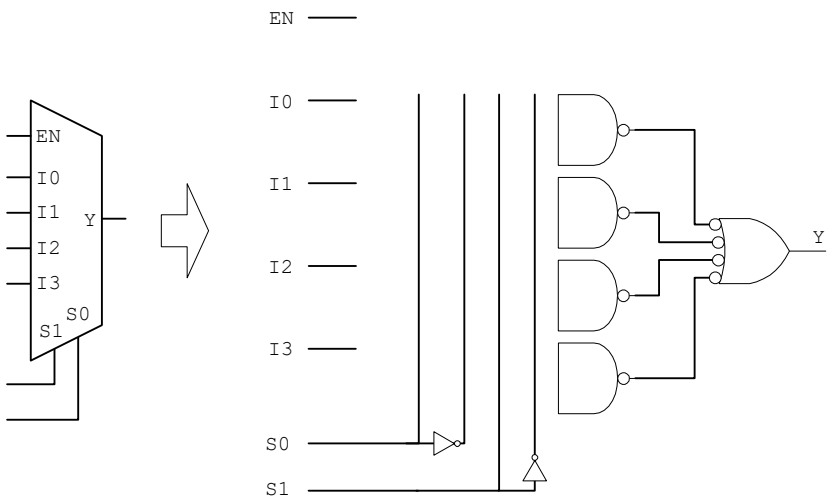
Revision: August 5, 2025

RealDigital
www.realdigital.org

1. (12 points) Complete the truth table and circuit sketch for a 4:1 mux. When completing the truth table, make use of don't care's to reduce the number of required rows.

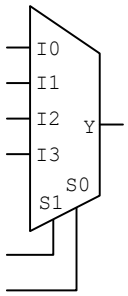
EN	S1	S0	Y

4:1 mux with enable truth table



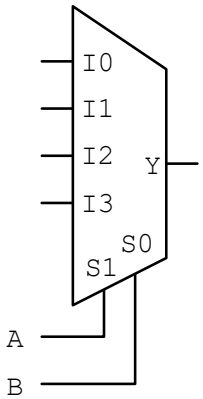
4:1 Mux with enable

2. (10 points) Compete a circuit sketch to show how F = Σm(0, 2, 4, 5, 6) can be implemented using the mux shown below. (Hint: prepare an entered-variable Kmap)



3. (10 points) Implement the logic function described in the K-map using a 4-to-1 Multiplexor. Show all your steps.

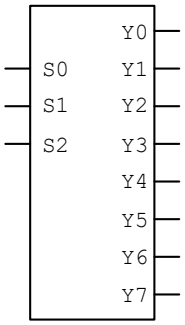
A B \ C D	00	01	11	10
00	1	0	0	1
01	1	1	1	1
11	1	1	0	0
10	1	0	0	1



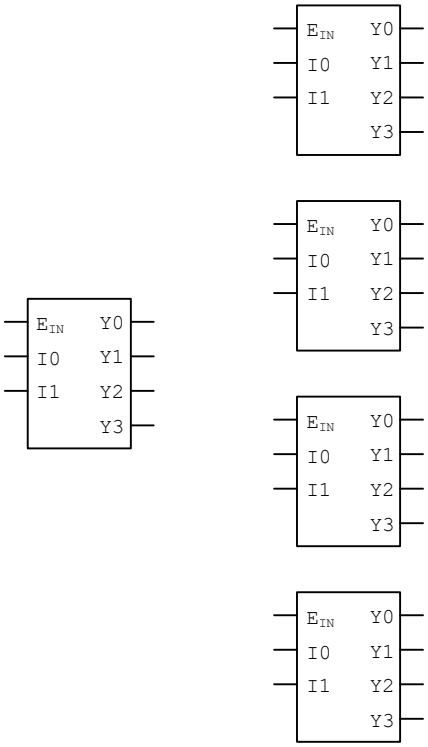
4. (6 points) Sketch an 8:1 mux using two 4:1 muxes and one 2:1 mux. Be sure to label all inputs and outputs.

5. (4 points) Sketch the circuit for a 3:8 decoder with enable.

6. (5 points) Sketch a circuit to implement $F = \Sigma m(1, 2, 4, 6)$ using the 3:8 decoder.

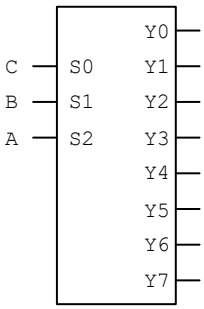


7. (5 points) Complete the 4:16 decoder built from 4 2:4 decoders below by sketching the missing wires. Label all inputs and outputs.



8. (5 points) Implement the logic function described in the K-map using a 3:8 Decoder.

A \ B C	00	01	11	10
0	1	0	0	1
1	1	1	0	1



9. (15 points) Sketch a circuit for a mux-demux circuit that has 8 data inputs and 8 data outputs. Label all inputs and outputs. (*Hint*: you should have four signals routed between the mux and demux).

10. (12 points) Complete the table below to show the numerical results from applying the indicated operation to the data shown. Opcodes are six-bit numbers defined as shown below. R = 1 for Rotate; D = 1 for Right; F is fill, and A2-A0 define the number of bits. Show all work to be eligible for partial credit.

R	D	F	A2	A1	A0

Input(Base10)	Input(Base2/8-bit)	Op Code	Output(Base10)	Output(Base2/8-bit))
47	00101111	000011	120	01111000
96		110111		
16		011001		
111		100011		
63		001111		
188		110001		