

RFSoc 4X2 Gen3
Variant: Prototype

12/17/2021
V2I1

RELEASED

Table with 8 columns: Page, Index, Page, Index, Page, Index, Page, Index. It lists the contents of the document, including Cover Page, Block Diagram, Power Diagram, User IO, LEDs, PMOD Headers, Syzygy Header, USB-JTAG, USB-UART, USB 3.0 Slave, USB 3.0 Host, 1PPS, Display Port, SD Card and EEPROM, Ethernet 1Gbit, QSFP, Clock I, Clock II, Clock III RF ADC Clock, Clock IV RF DAC Clock, RFSoc Config, PS 500-502, PS 504, PS MGT, PL Banks 64-66, PL Banks 67-69, PL Banks 84, 87, PL GTY, RF ADC, RF DAC, RFSoc Power Pins, RFSoc Decoupling, RFSoc GND Pins, DDR4 Memory PS I, DDR4 Memory PS II, DDR4 Memory PL I, DDR4 Memory PL II, PWR Input and Fan Ctrl, PWR I 0V85, PWR II 1V8, 3V3 and GTY PWR, PWR III RF DC and 5V0, PWR IV RF LDO, PWR V DDR4, PWR VI Syzygy, Current Monitor, Sequencer, Mech and PWR Sequencing, and Doc Revision History.

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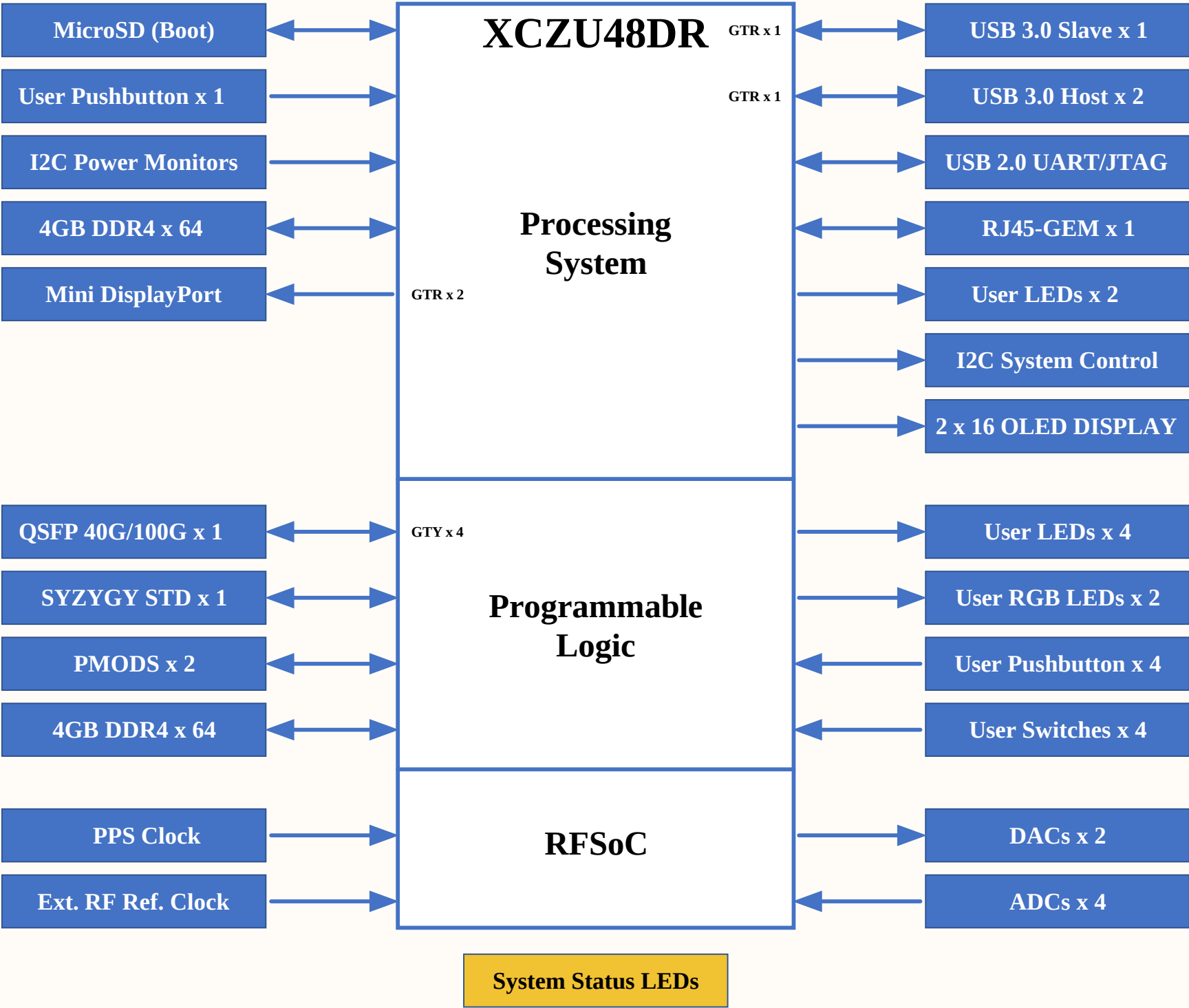
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Title: RFSoc 4X2 Gen3 Variant: Prototype
Page Contents: [01] - COVER PAGE.SchDoc
Size: A3 DWG NO: KT-000-001-001-001 Revision: V2I1
Date: 12/17/2021 Checked by: * Sheet 1 of 46

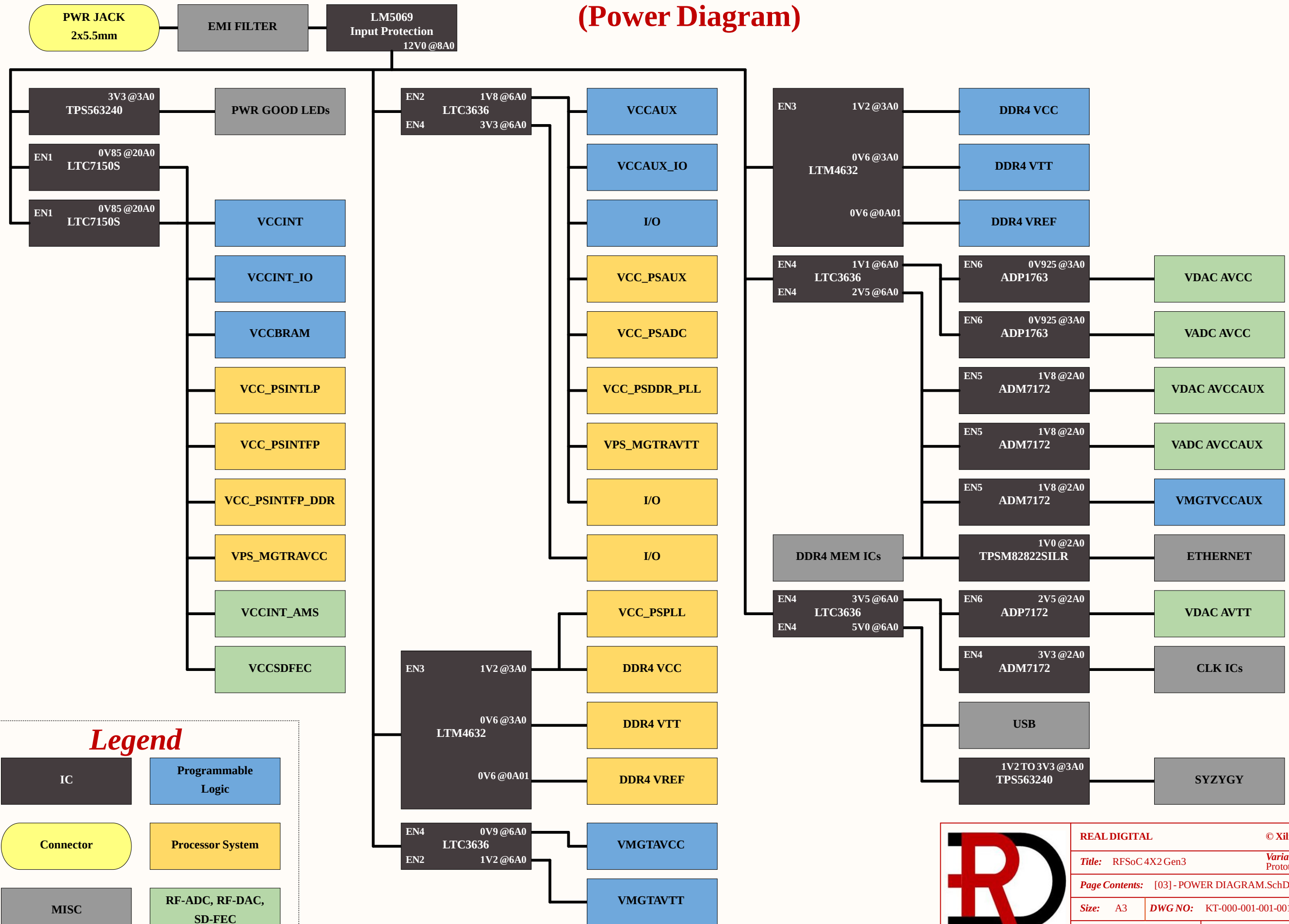
RFSoc 4X2 Gen3

(Block Diagram)



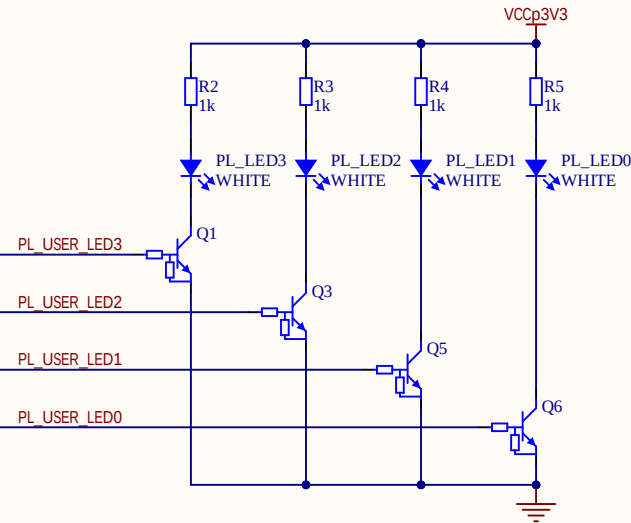
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	Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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RFSoC 4X2 Gen3 (Power Diagram)

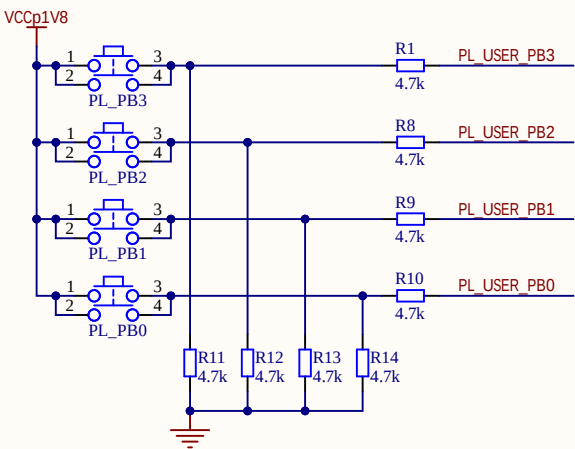


USER IO, LEDs

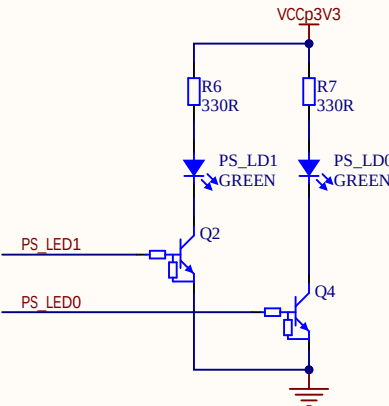
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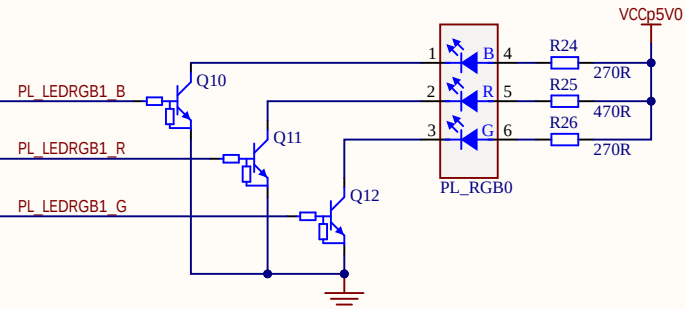
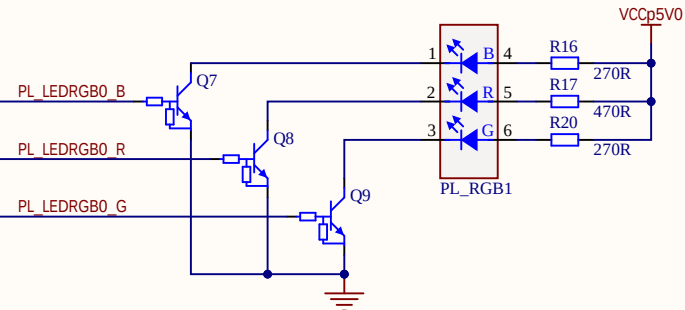
PL user-defined pushbuttons



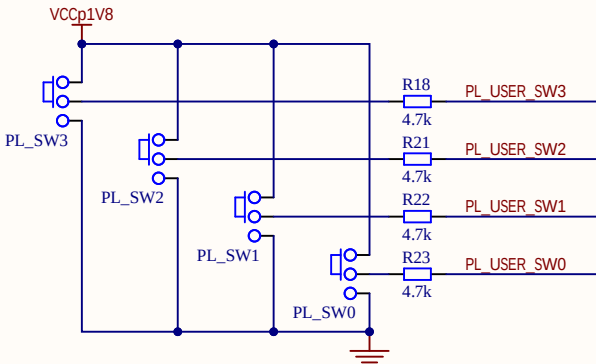
PS user-defined green LEDs



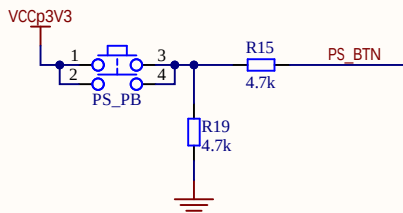
PL user-defined RGB LEDs



PL user-defined switches

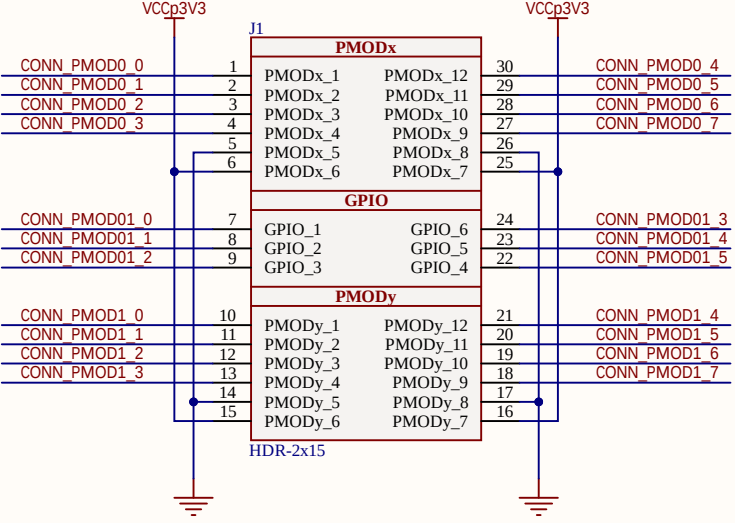
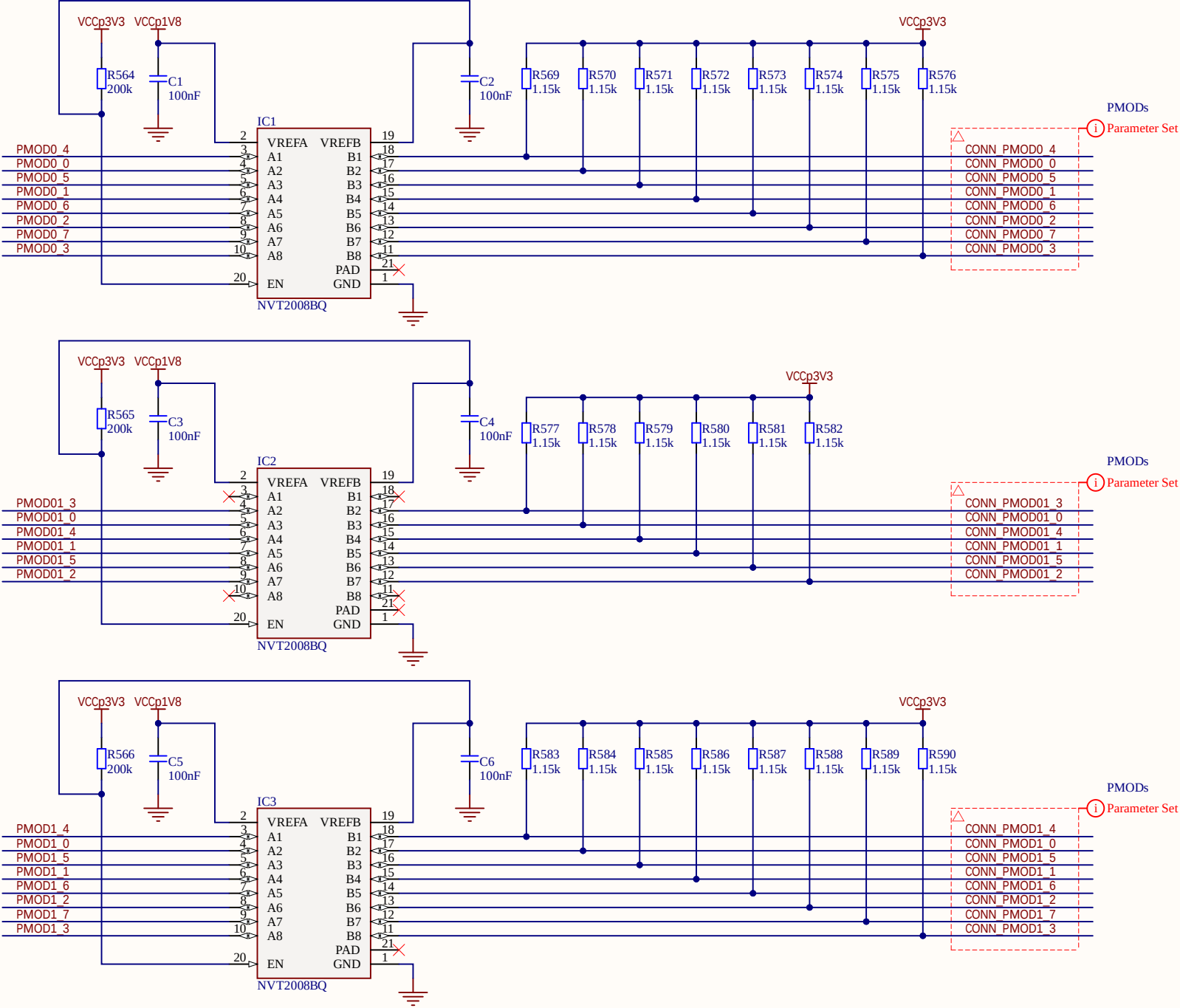


PS user-defined pushbutton



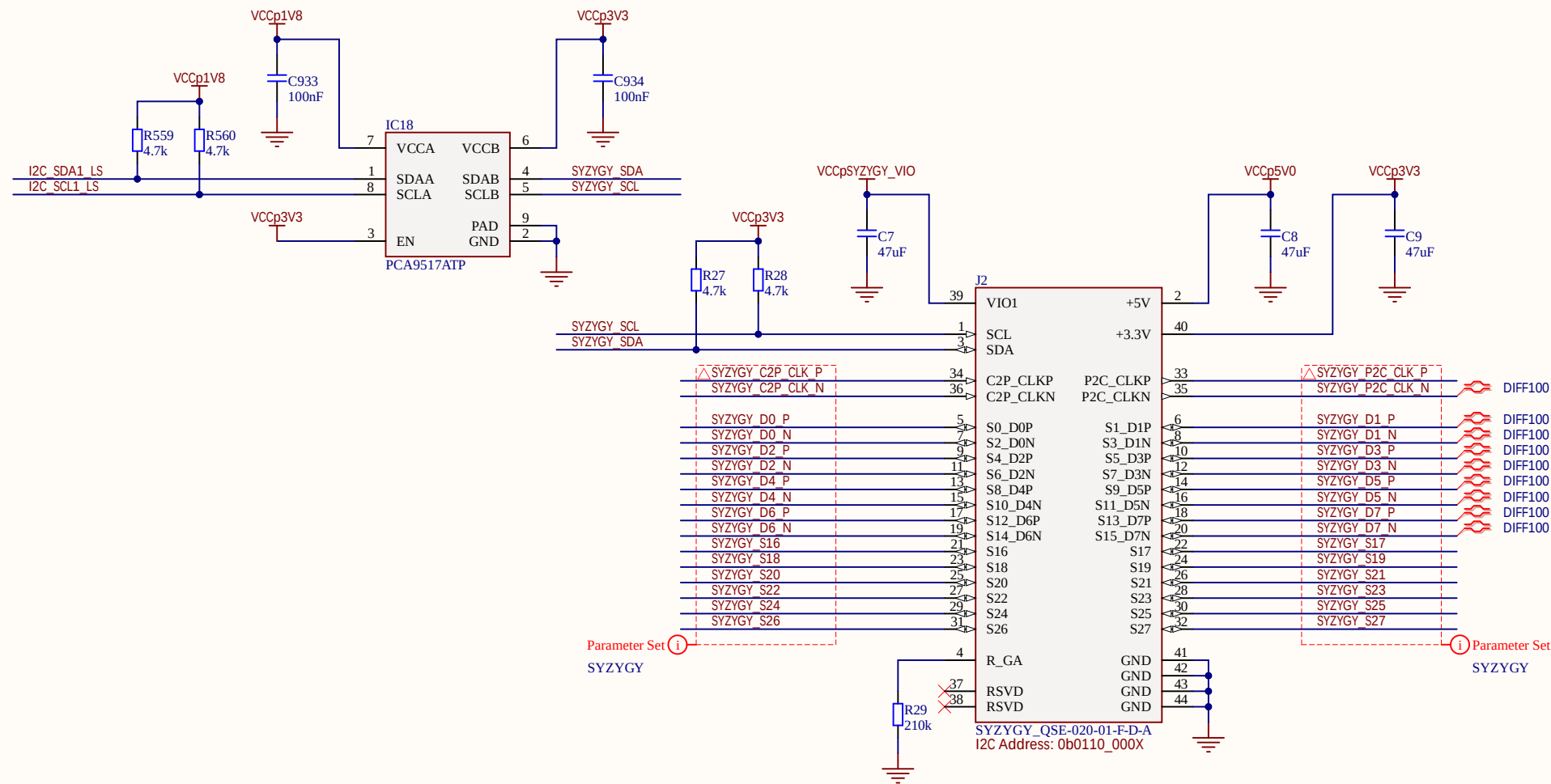
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Page Contents: [04] - USER IO, LEDs.SchDoc			
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PMOD HEADERS



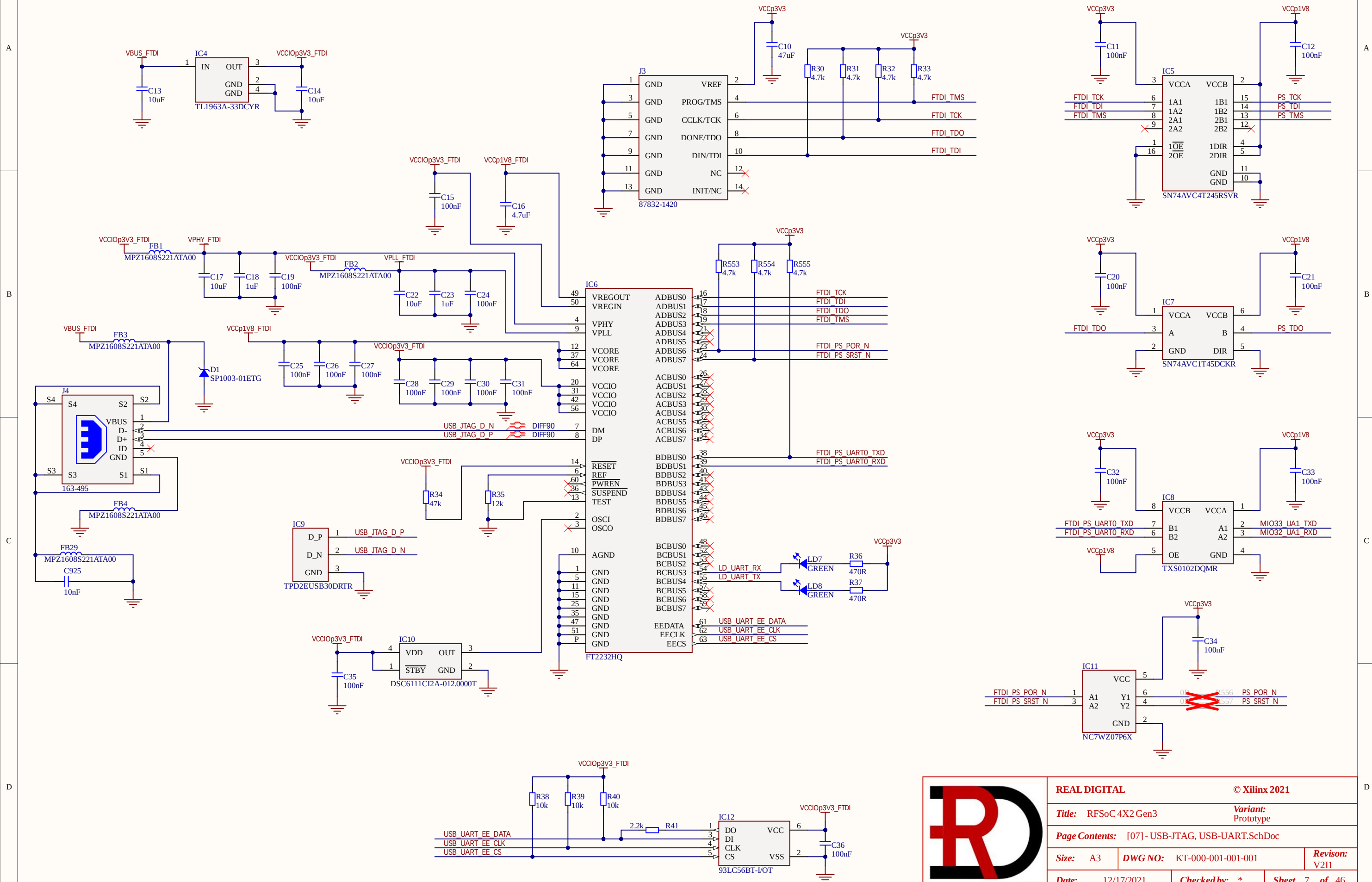
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SYZYGY HEADER

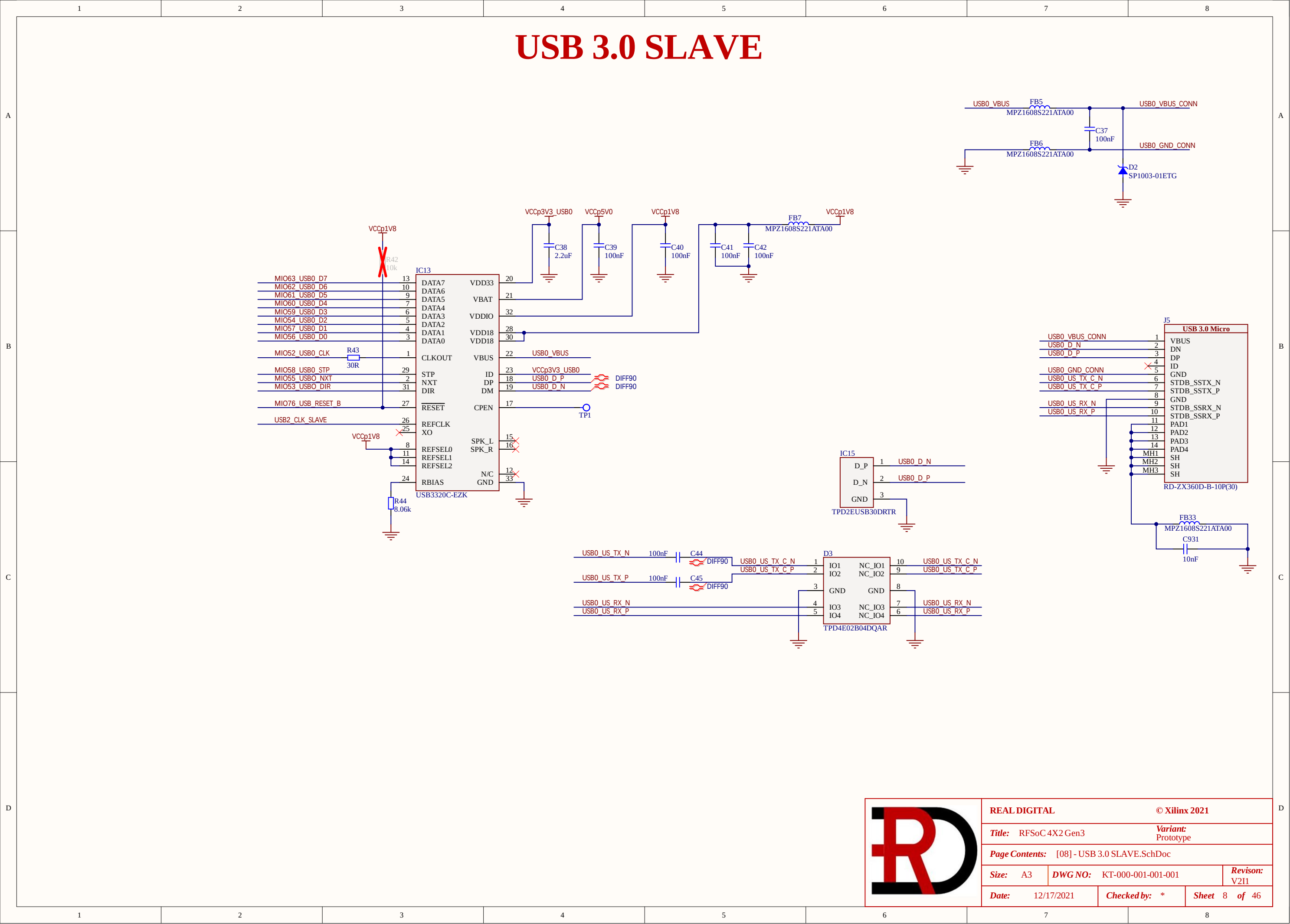
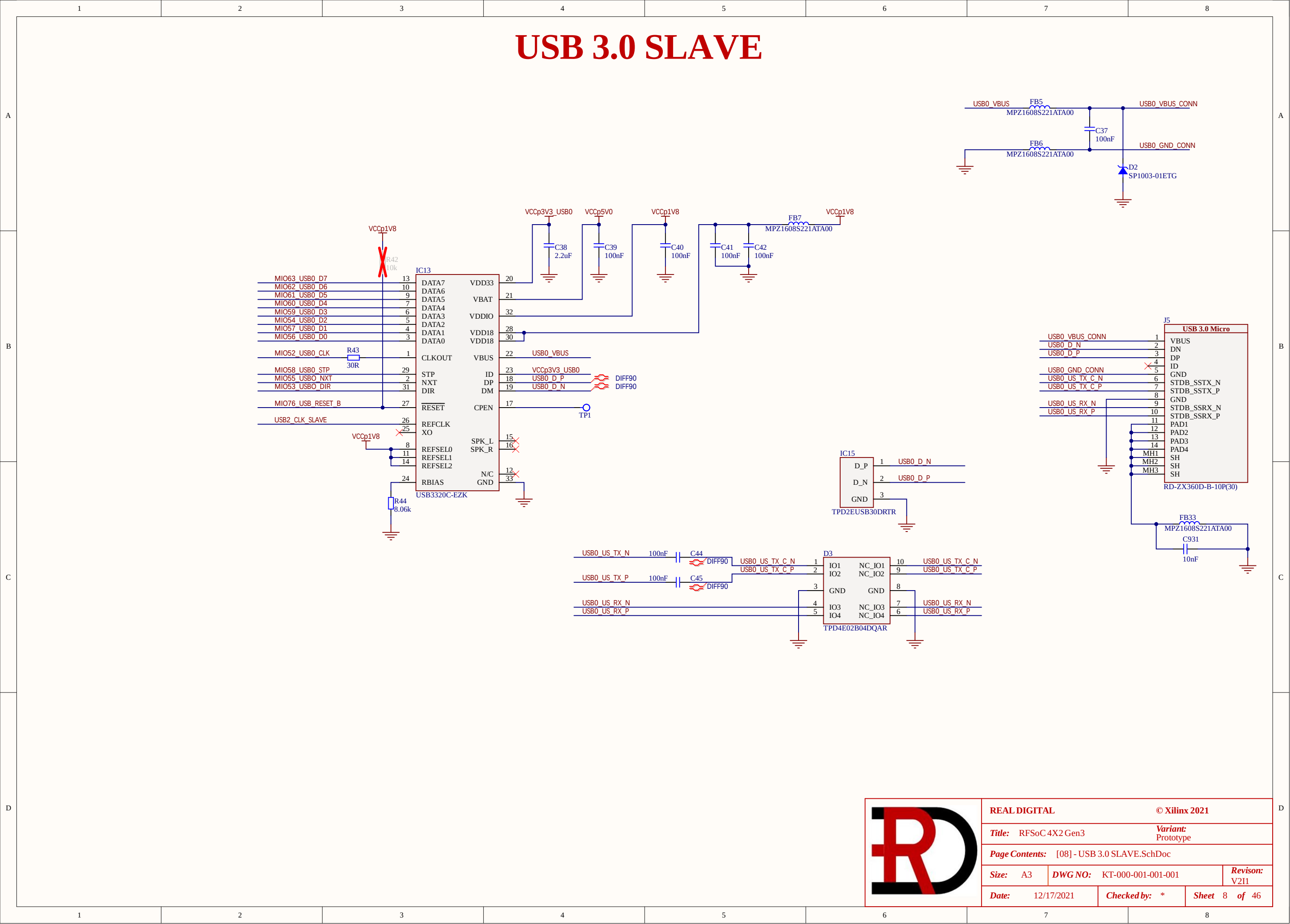
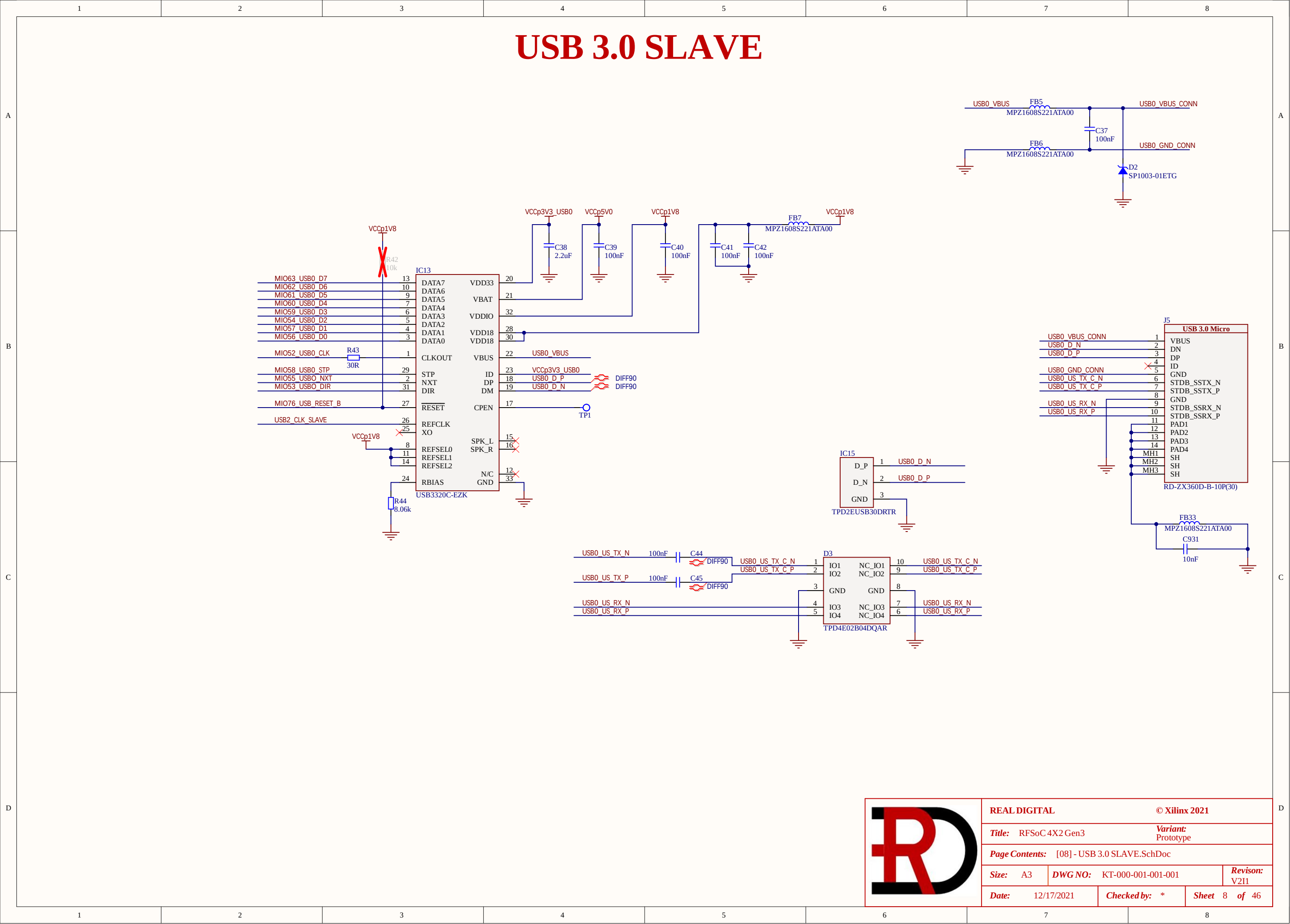
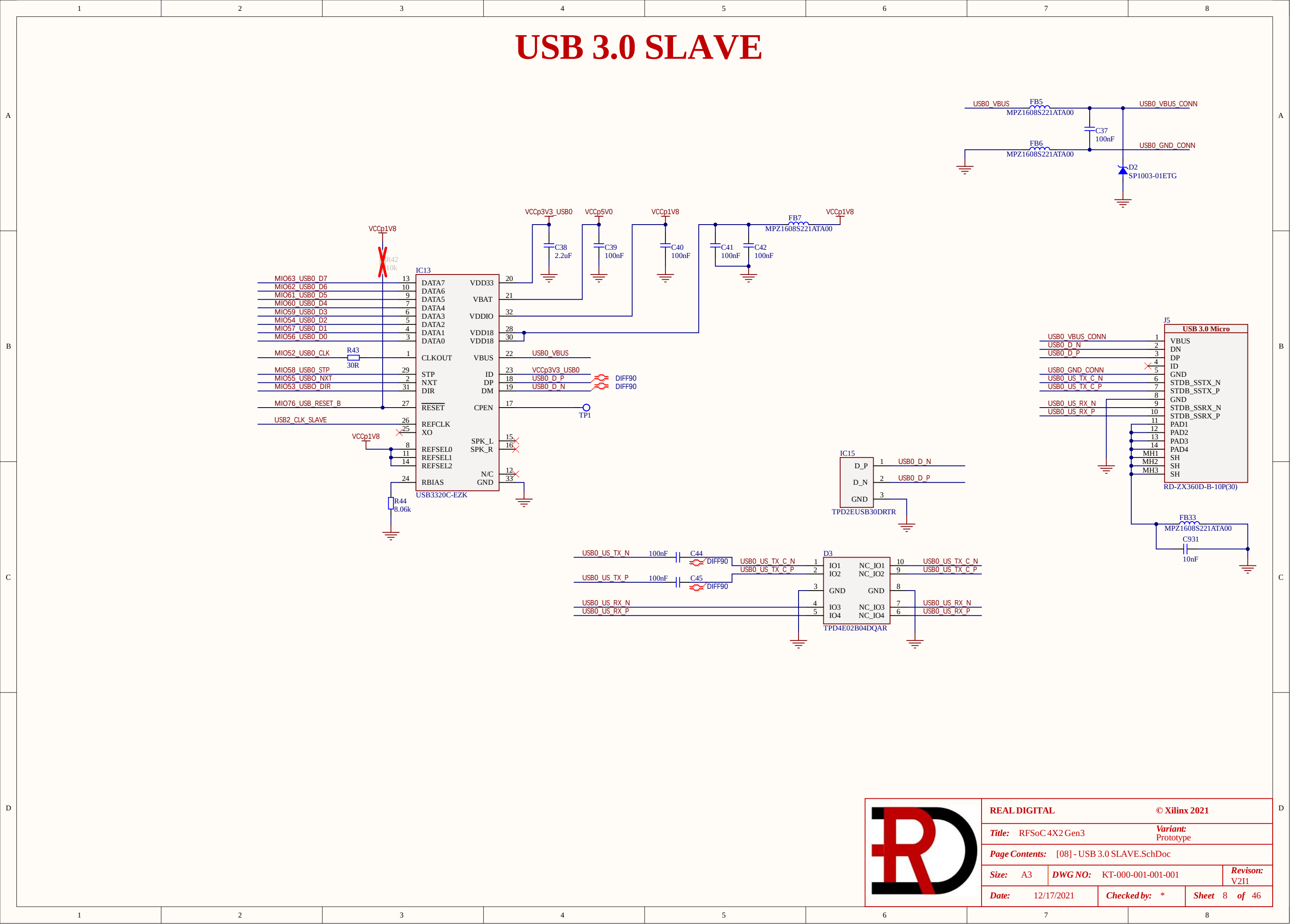
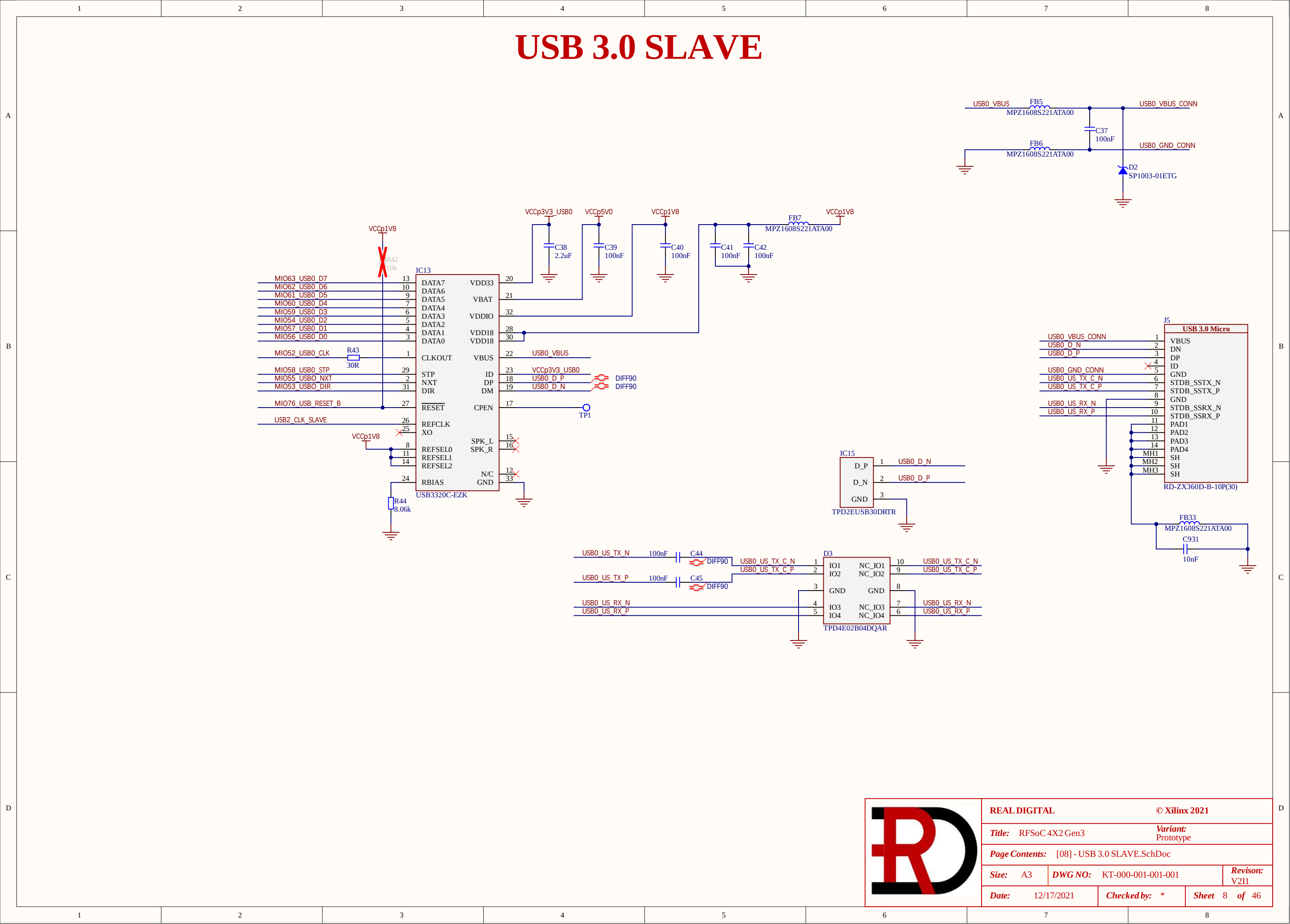


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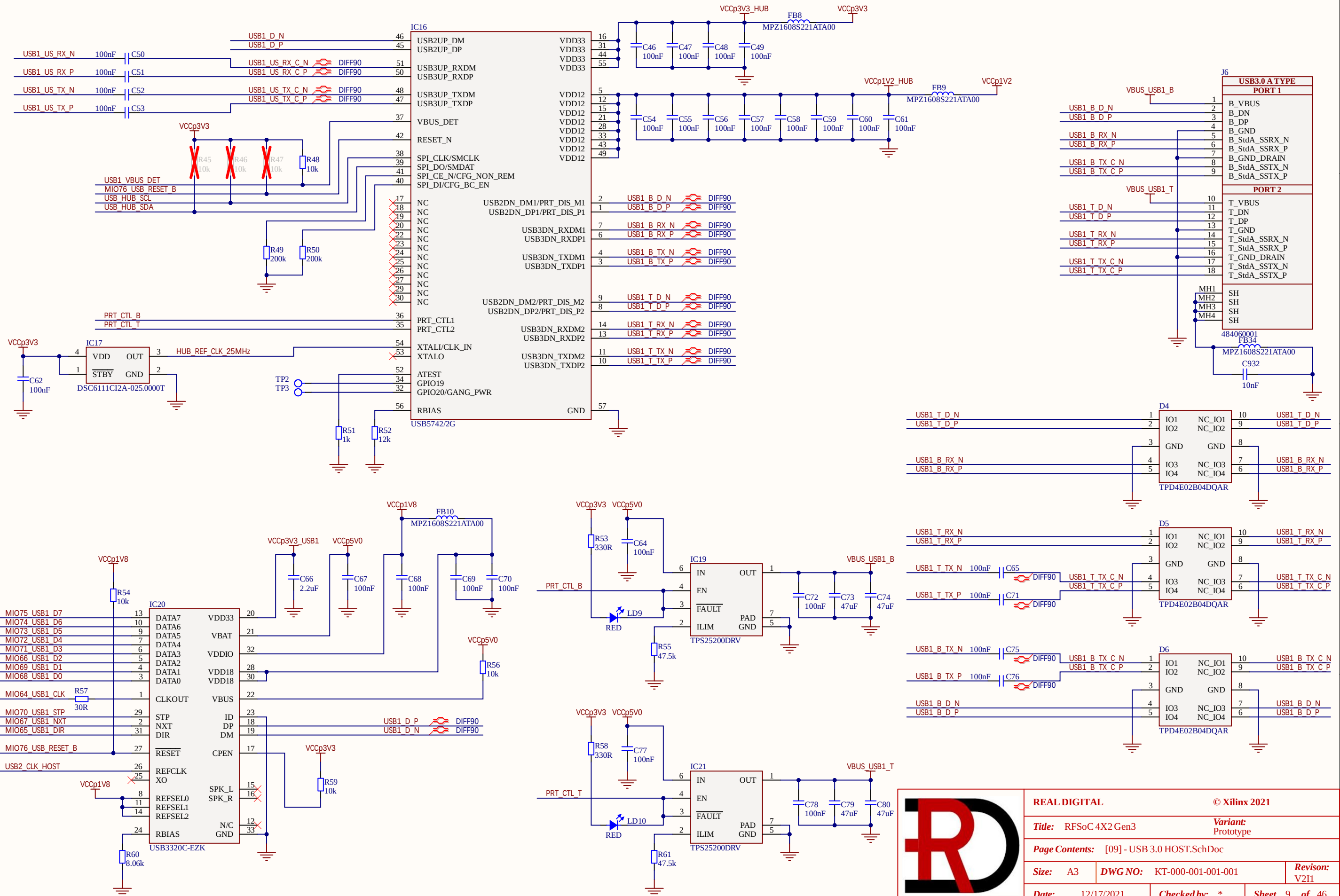
USB-JTAG, USB-UART



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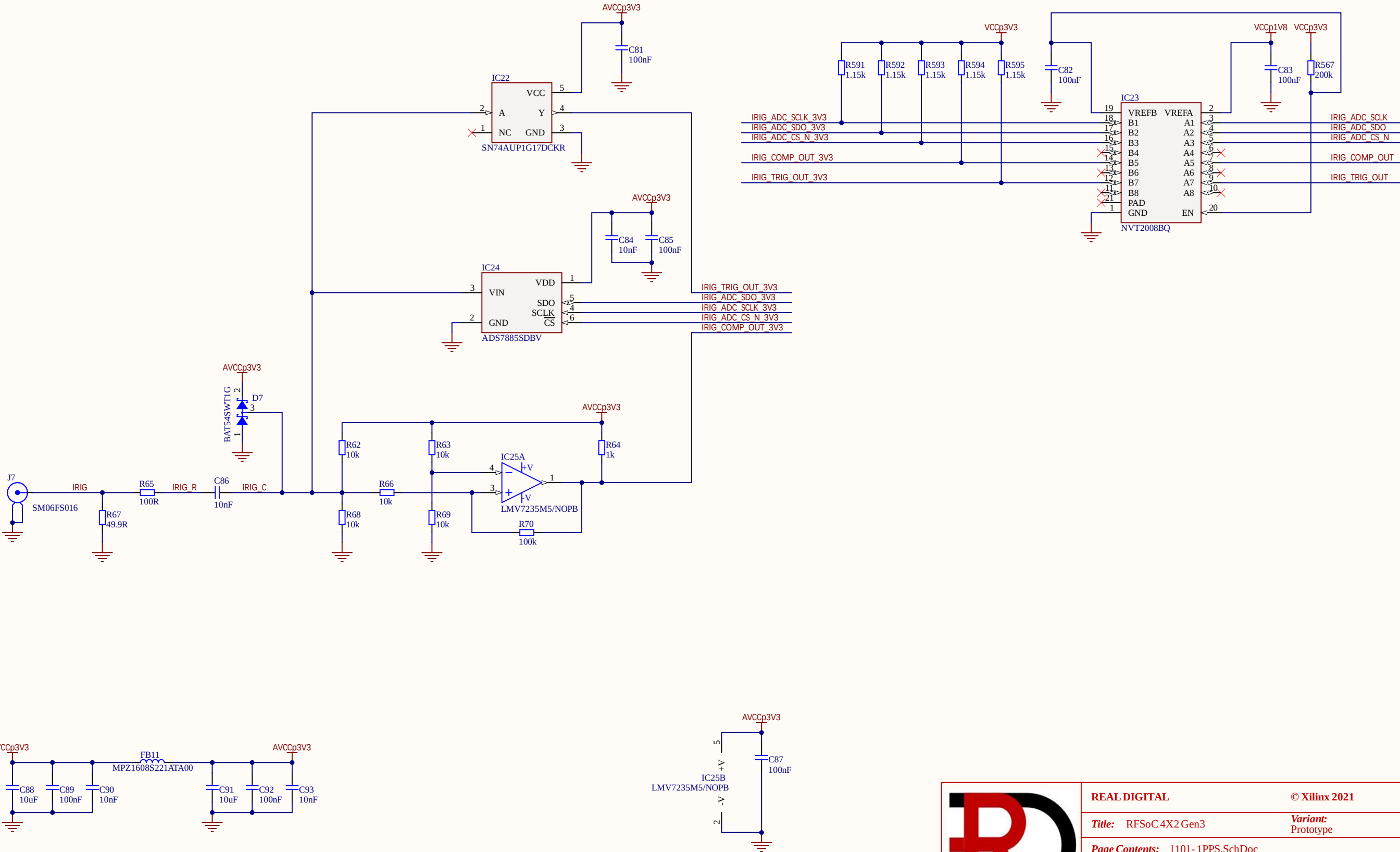
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USB 3.0 HOST



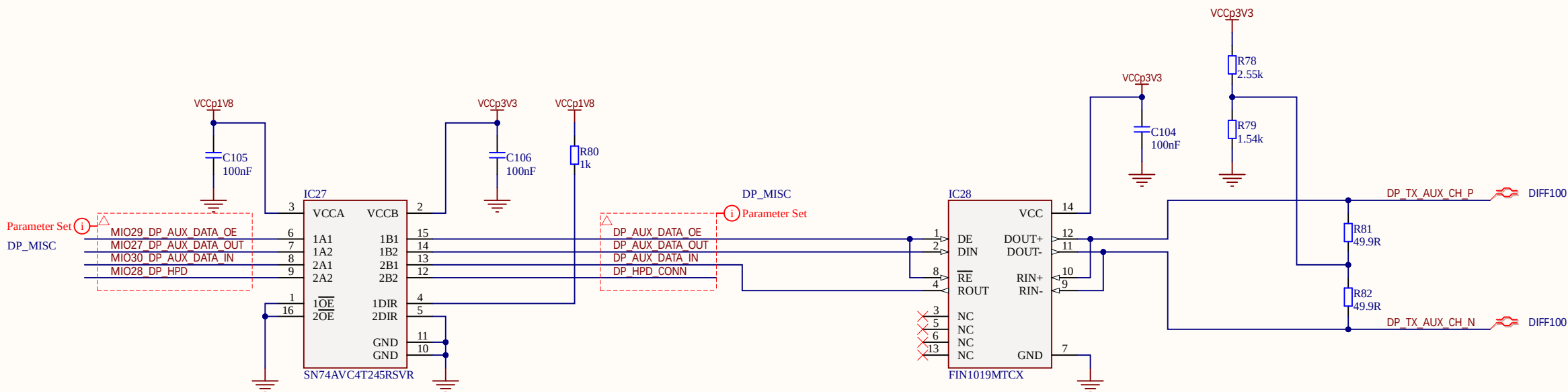
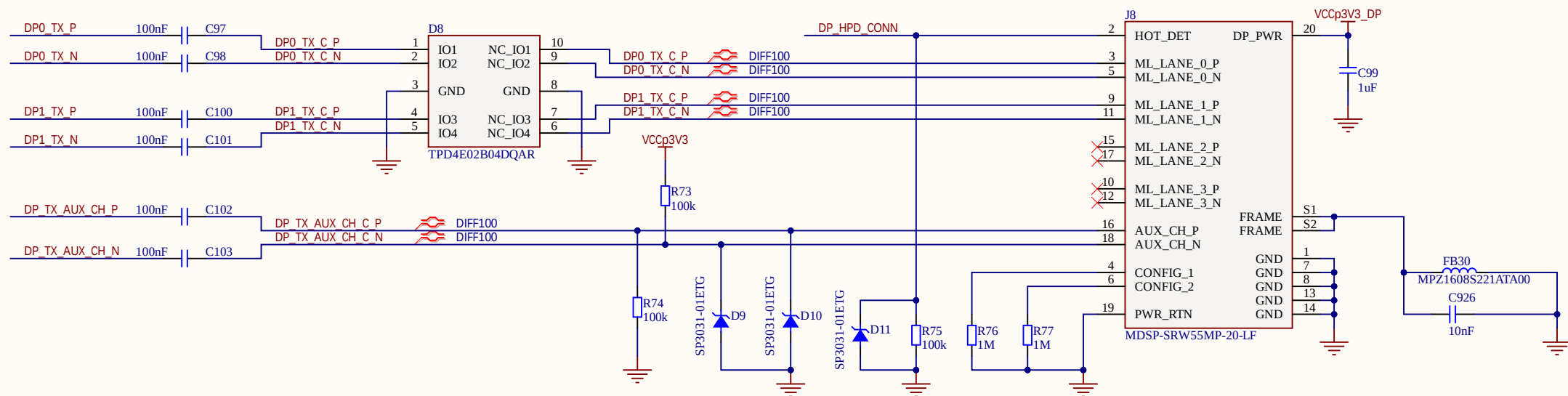
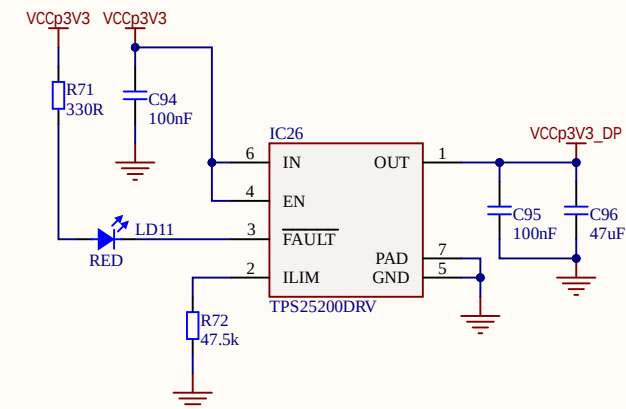
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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1PPS



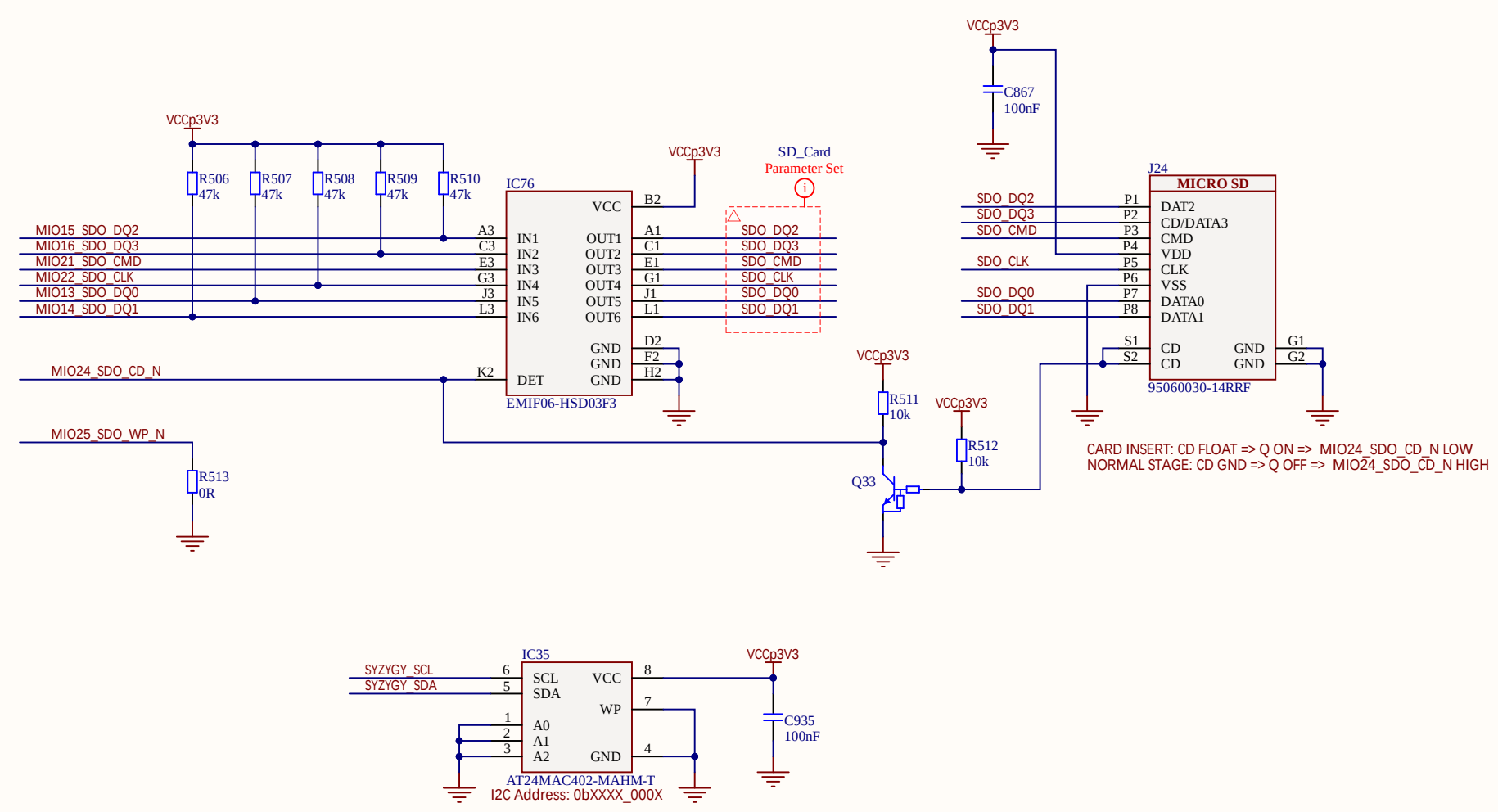
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DISPLAY PORT



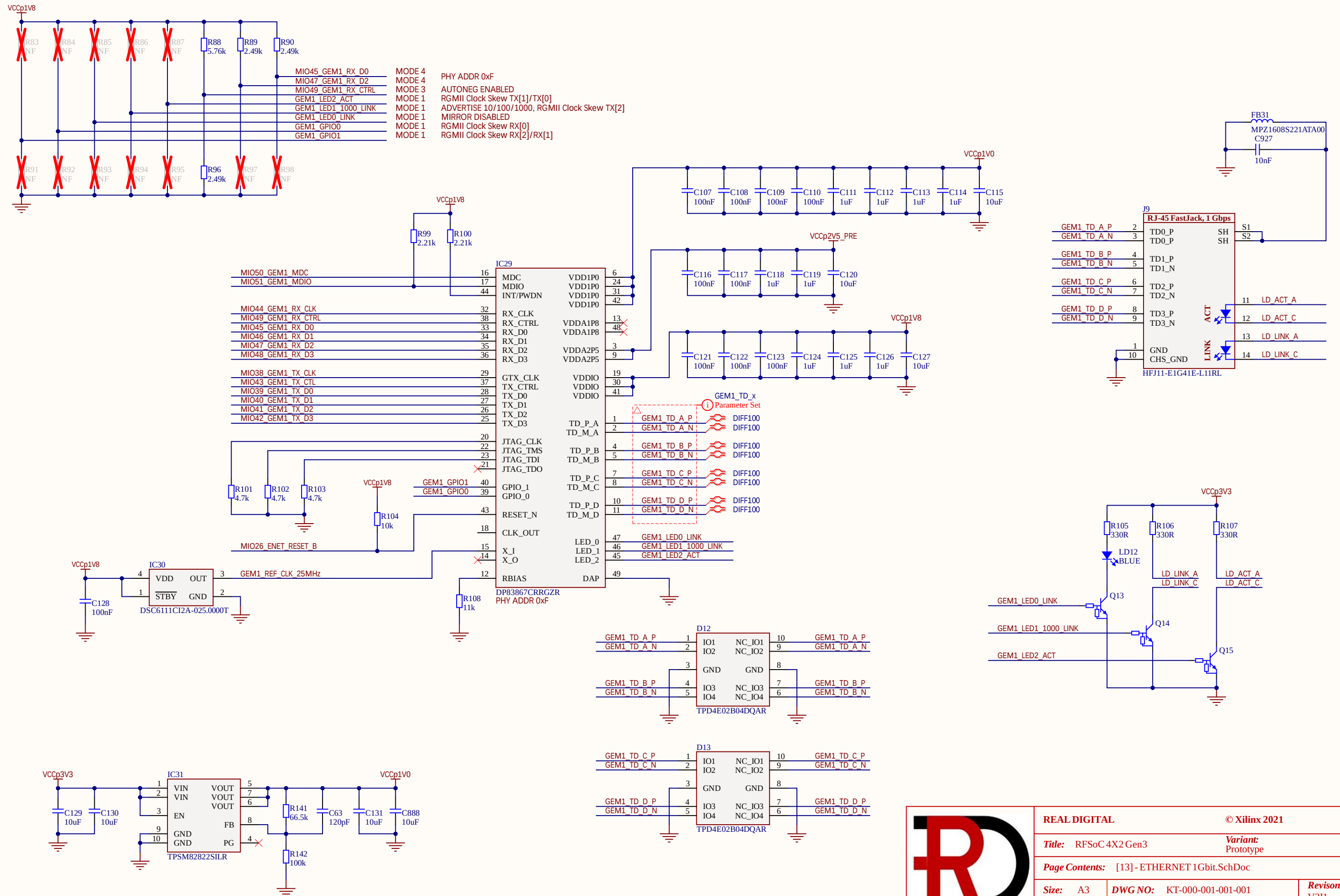
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SD CARD

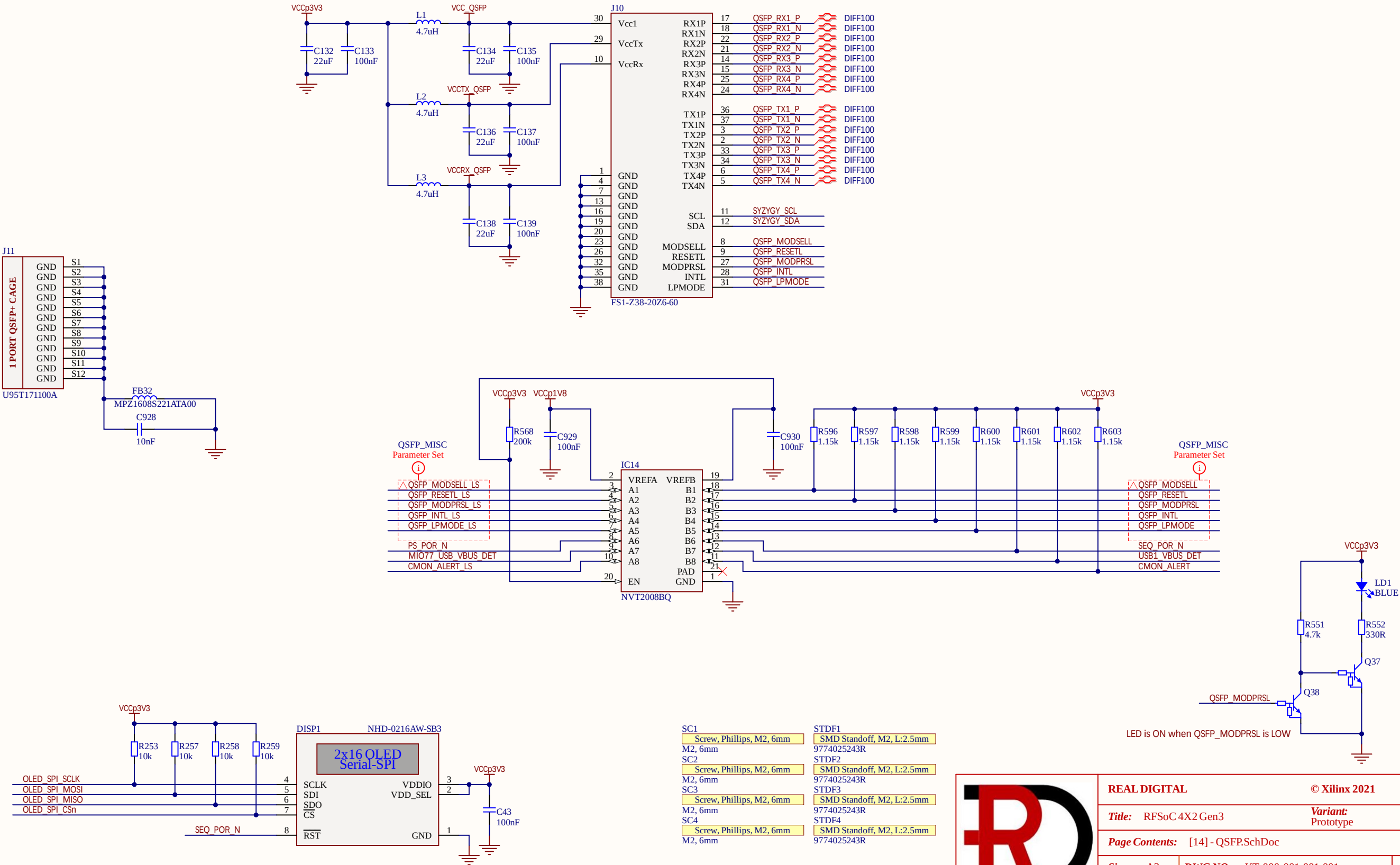


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ETHERNET 1Gbit

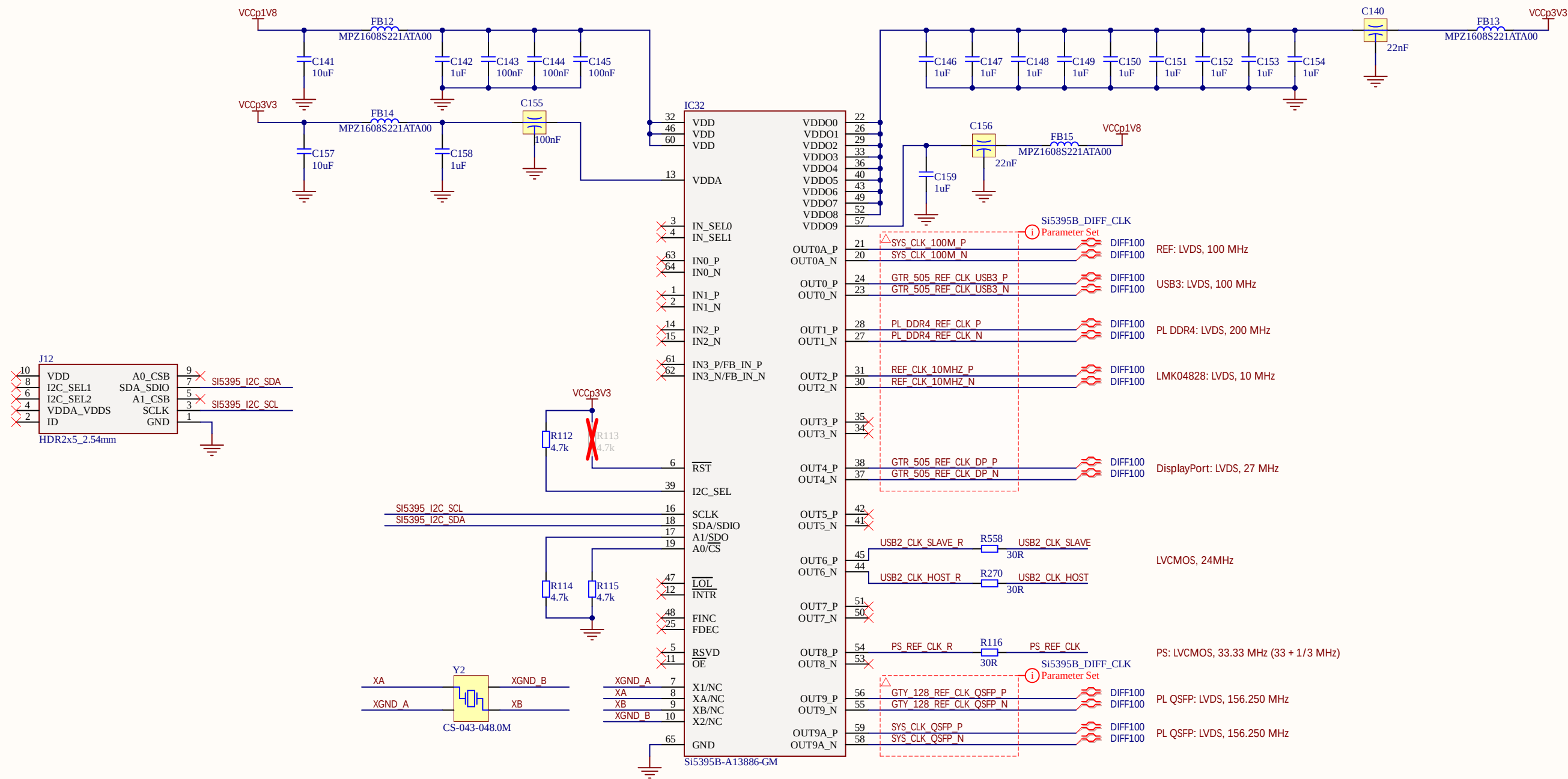


QSFP



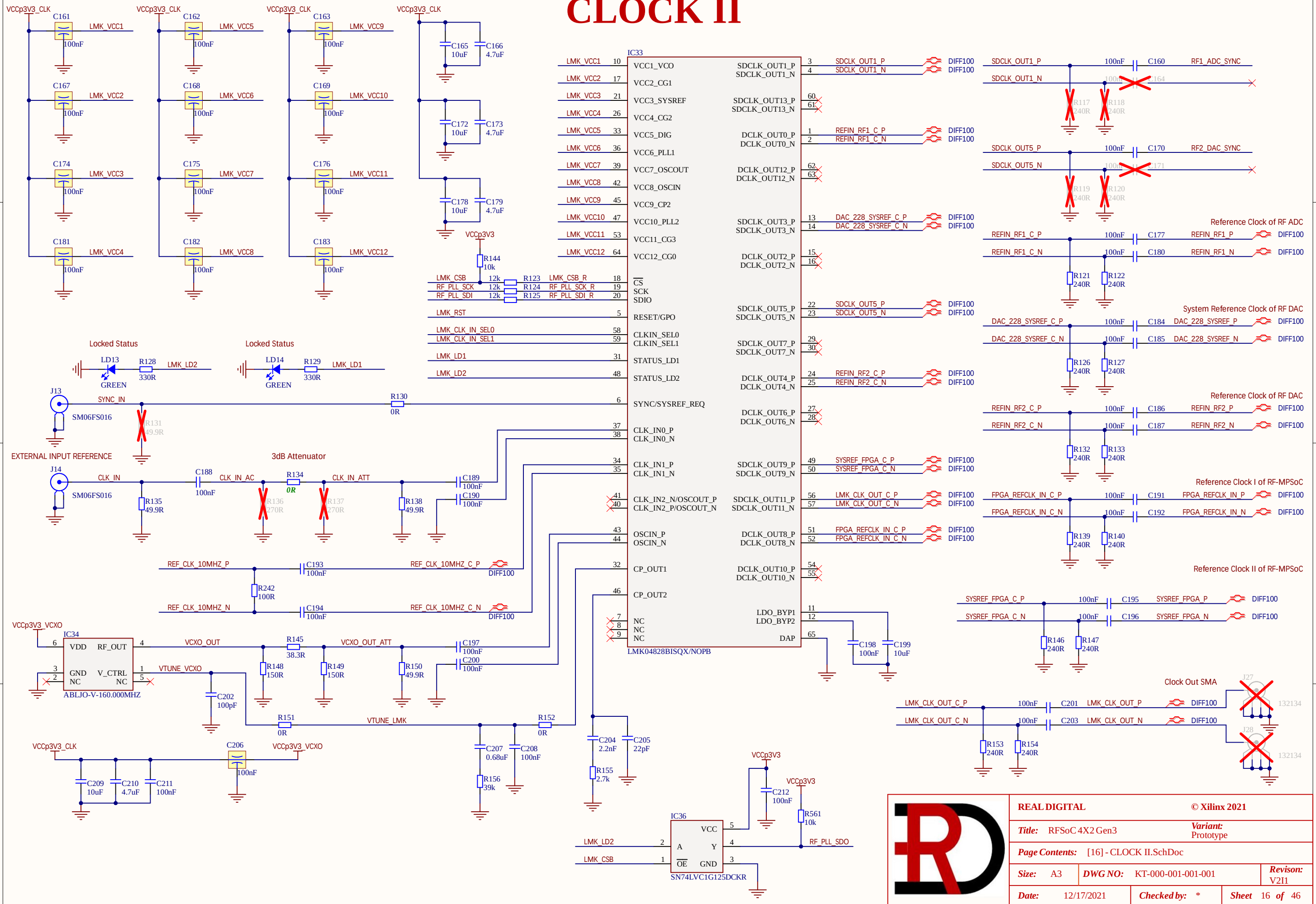
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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CLOCK I: SYS, DDR4, MGT, GTY AND USER

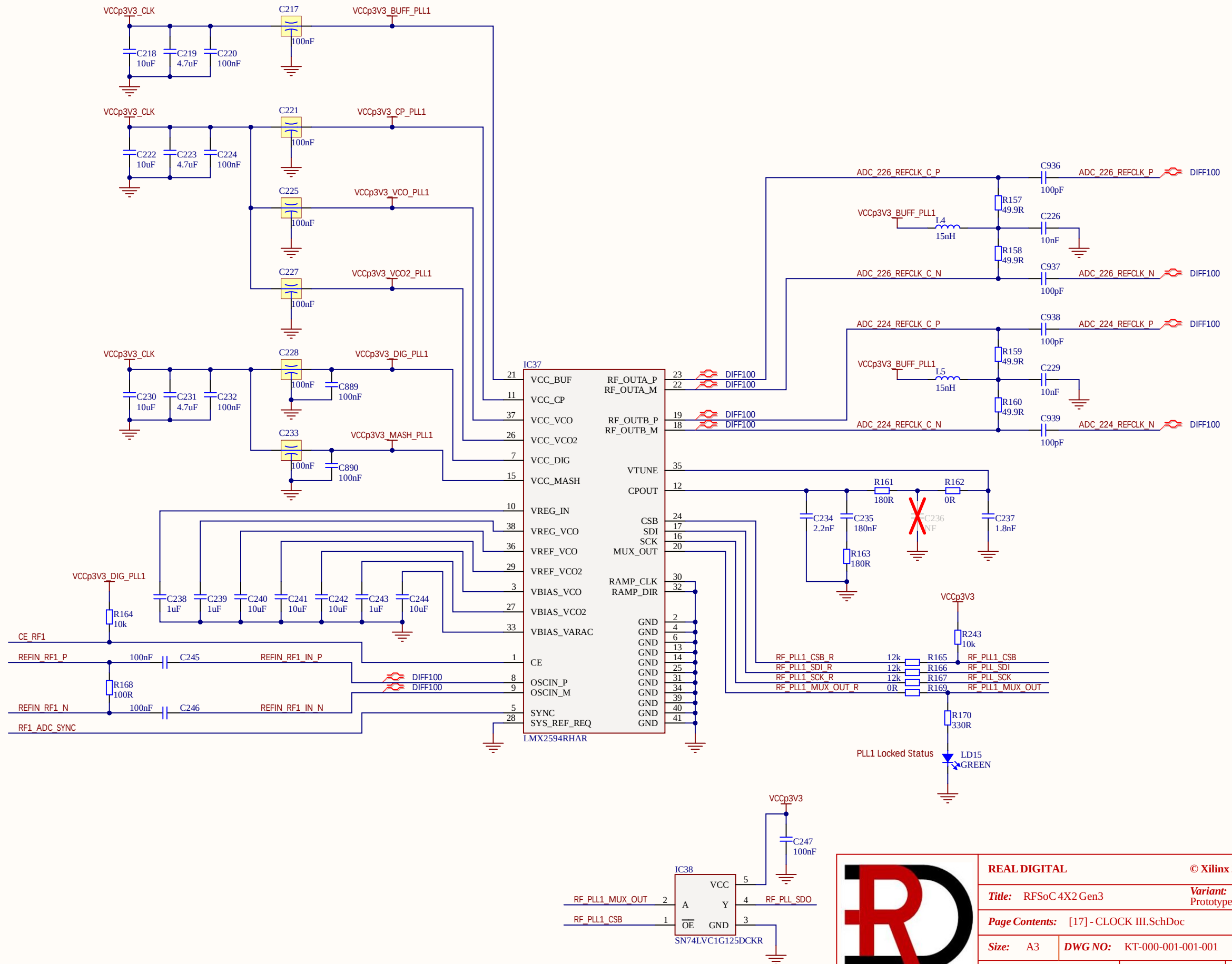


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CLOCK II

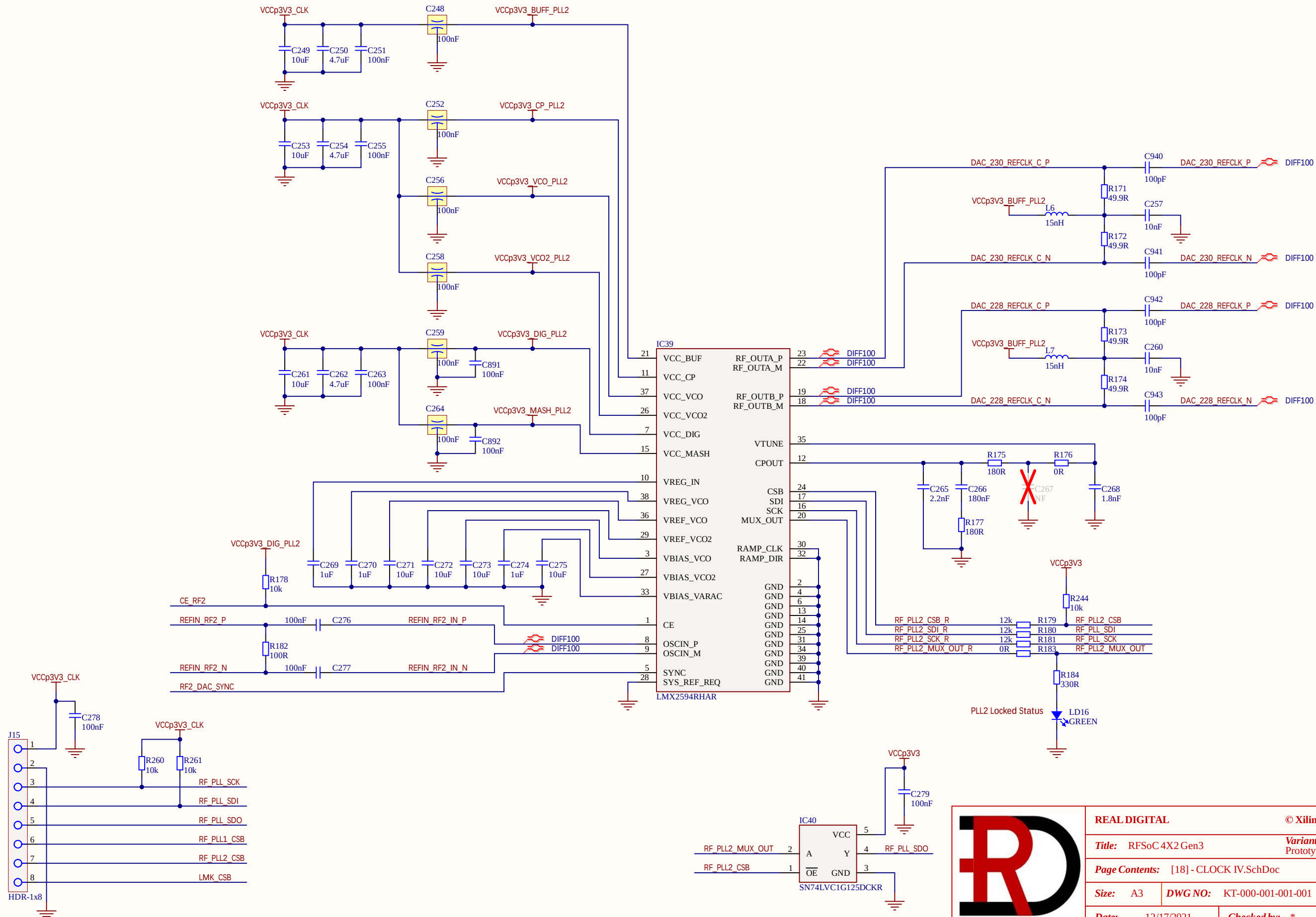


CLOCK III: RF ADC CLOCK



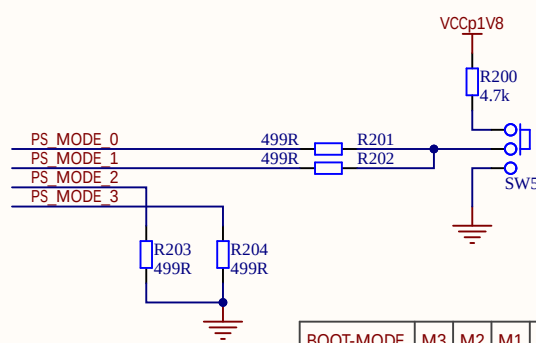
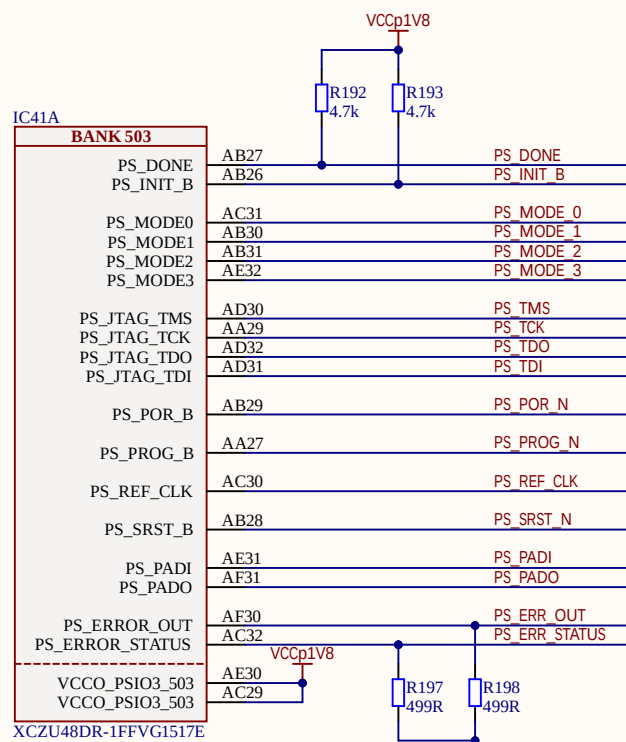
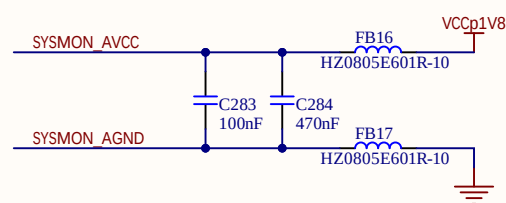
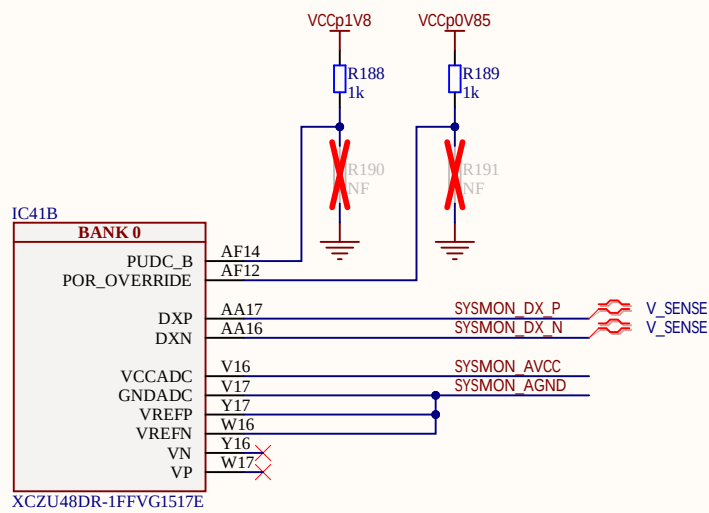
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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CLOCK IV: RF DAC CLOCK

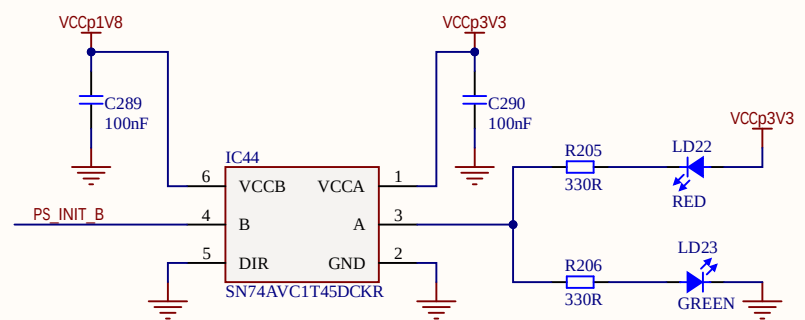
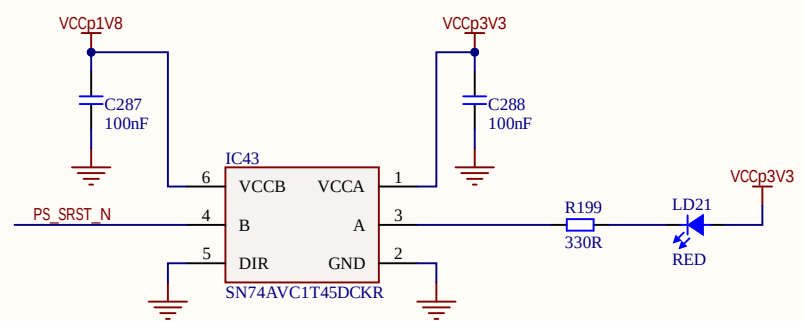
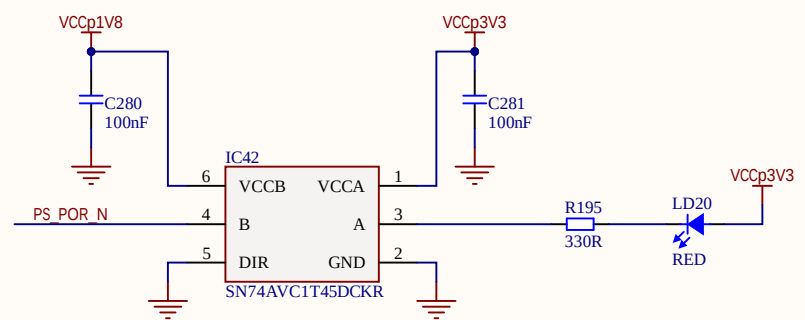
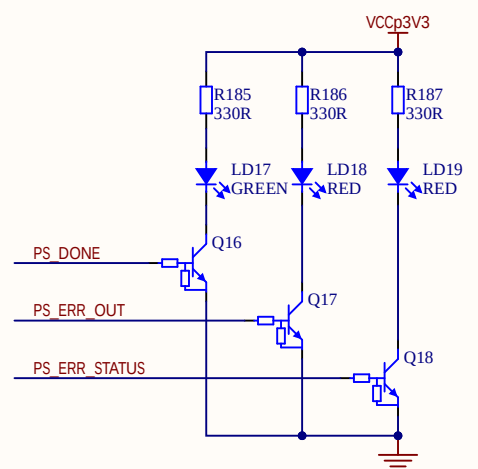
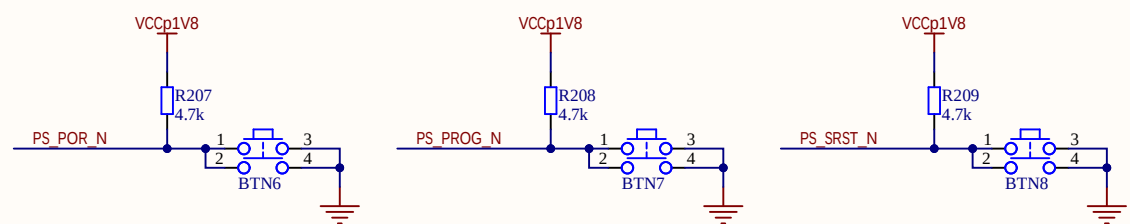


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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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RFSoc CONFIG



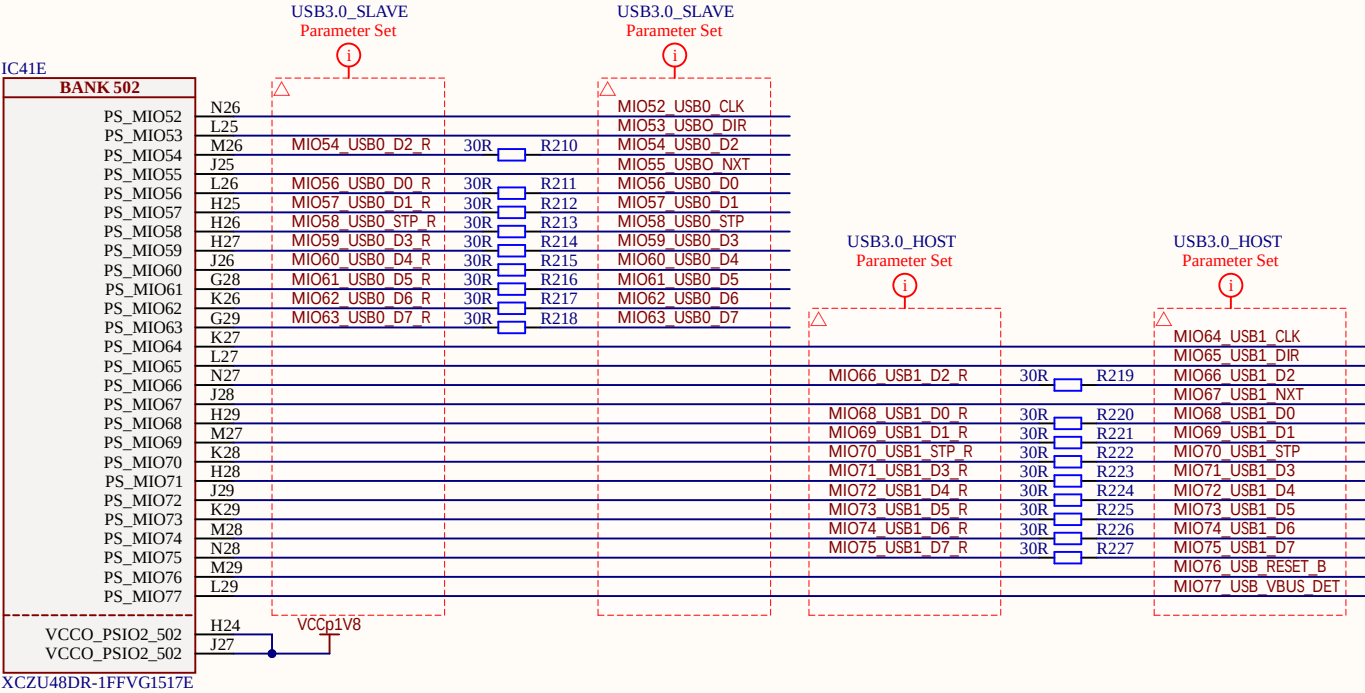
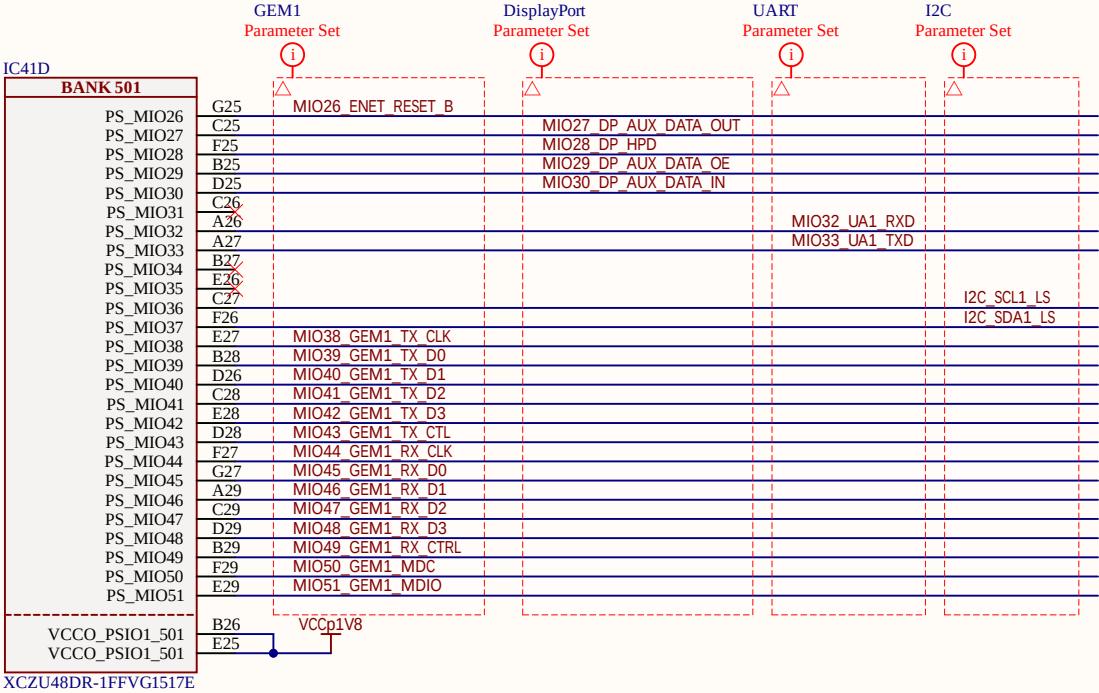
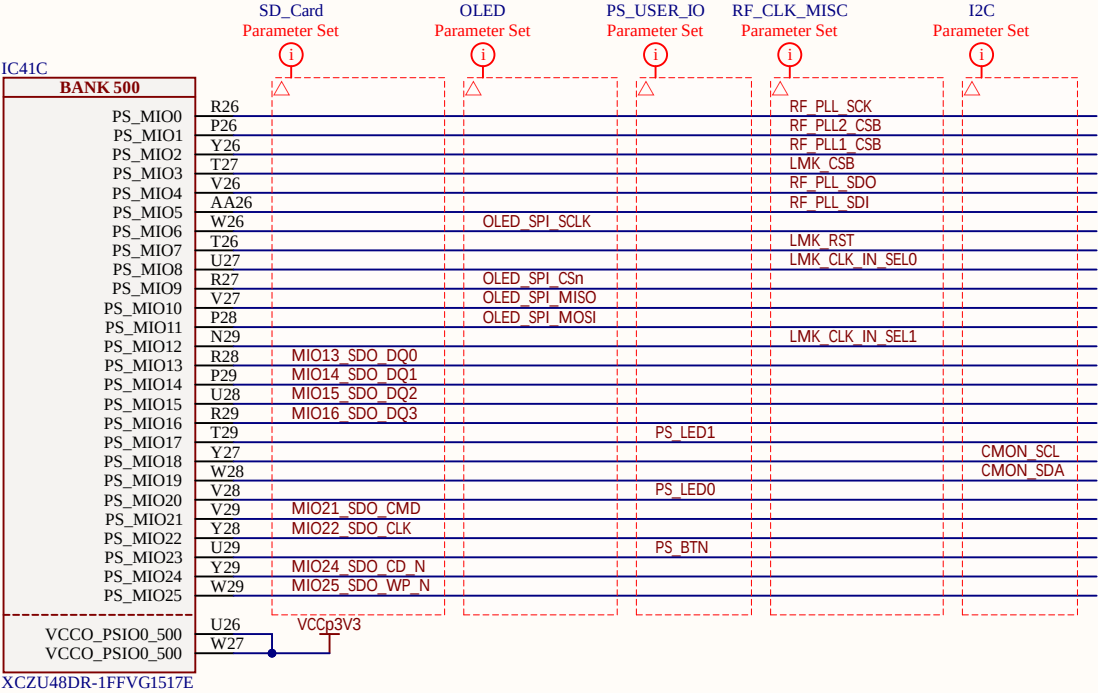
BOOT-MODE	M3	M2	M1	M0
JTAG	L	L	L	L
SD Card	L	L	H	H





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Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [19] - RFSoc CONFIG.SchDoc			
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PS: BANKS 500-502





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Page Contents: [20] - PS BANKS 500-502.SchDoc			
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PS: BANK 504

IC41F

BANK 504 1 OF 2		
PS_DDR_A0	AV31	PS_DDR4_A0
PS_DDR_A1	AW28	PS_DDR4_A1
PS_DDR_A2	AV28	PS_DDR4_A2
PS_DDR_A3	AU29	PS_DDR4_A3
PS_DDR_A4	AW31	PS_DDR4_A4
PS_DDR_A5	AU28	PS_DDR4_A5
PS_DDR_A6	AL29	PS_DDR4_A6
PS_DDR_A7	AM30	PS_DDR4_A7
PS_DDR_A8	AM29	PS_DDR4_A8
PS_DDR_A9	AP29	PS_DDR4_A9
PS_DDR_A10	AT31	PS_DDR4_A10
PS_DDR_A11	AT32	PS_DDR4_A11
PS_DDR_A12	AT30	PS_DDR4_A12
PS_DDR_A13	AU32	PS_DDR4_A13
PS_DDR_A14	AR28	PS_DDR4_A14_WE_N
PS_DDR_A15	AP30	PS_DDR4_A15_CAS_N
PS_DDR_A16	AP28	PS_DDR4_A16_RAS_N
PS_DDR_A17	AK29	
PS_DDR_BA0	AN30	PS_DDR4_BA0
PS_DDR_BA1	AM32	PS_DDR4_BA1
PS_DDR_BG0	AN32	PS_DDR4_BG0
PS_DDR_BG1	AL31	
PS_DDR_CS_N0	AW29	PS_DDR4_CS_N
PS_DDR_CS_N1	AR31	
PS_DDR_ACT_N	AL30	PS_DDR4_ACT_N
PS_DDR_CKE0	AW30	PS_DDR4_CKE
PS_DDR_CKE1	AR32	
PS_DDR_ODT0	AV32	PS_DDR4_ODT
PS_DDR_ODT1	AP31	
PS_DDR_RAM_RST_N	AM33	PS_DDR4_RAM_RESET_N
PS_DDR_PARITY	AN31	PS_DDR4_PARITY
PS_DDR_ALERT_N	AL32	PS_DDR4_ALERT
PS_DDR_CLK0	AU30	PS_DDR4_CLK_P
PS_DDR_CLK_N0	AV30	PS_DDR4_CLK_N
PS_DDR_CLK1	AR29	
PS_DDR_CLK_N1	AT29	
PS_DDR_ZQ	AN33	PS_DDR4_ZQ
VCCO_PSDDR_504	AV34	
VCCO_PSDDR_504	AV29	
VCCO_PSDDR_504	AT33	
VCCO_PSDDR_504	AT28	
VCCO_PSDDR_504	AP32	
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VCCO_PSDDR_504	AM31	

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IC41G

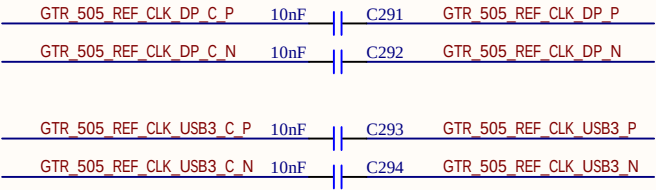
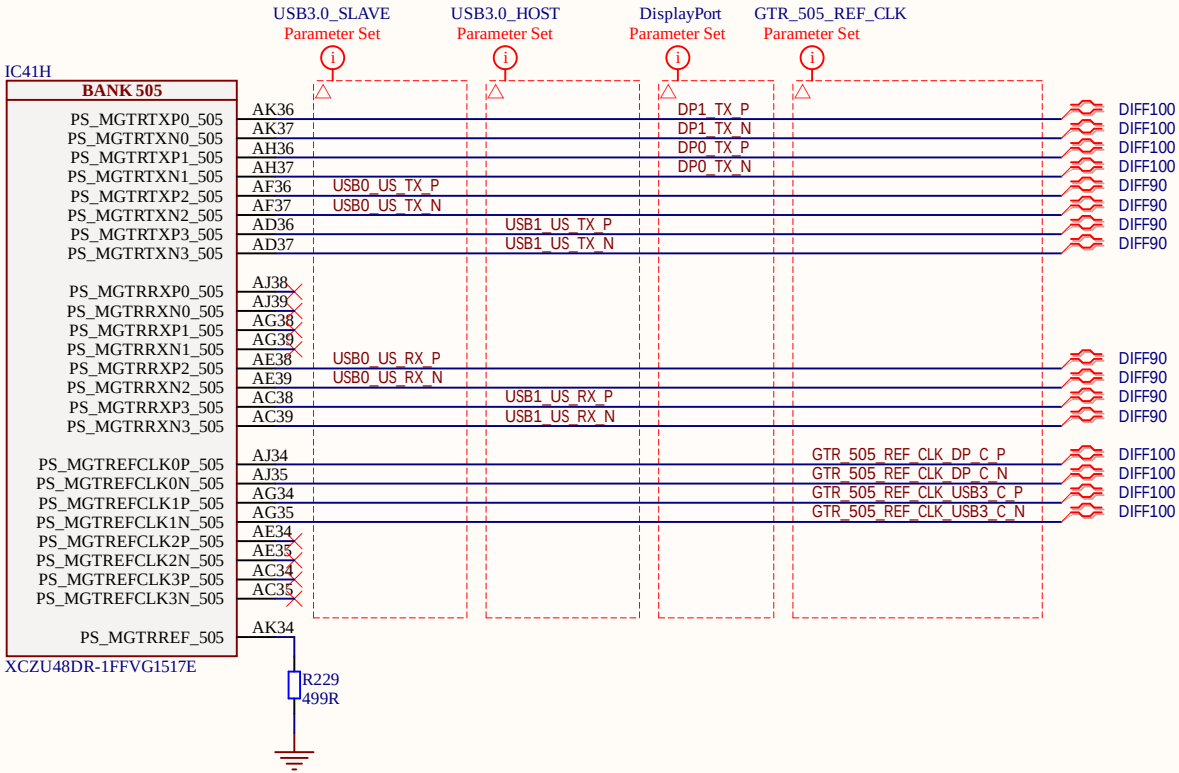
BANK 504 2 OF 2		
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PS_DDR4_DQ3	AW23	PS_DDR_DQ3
PS_DDR4_DQ4	AV23	PS_DDR_DQ4
PS_DDR4_DQ5	AV22	PS_DDR_DQ5
PS_DDR4_DQ6	AR24	PS_DDR_DQ6
PS_DDR4_DQ7	AR23	PS_DDR_DQ7
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PS_DDR4_DQ10	AU25	PS_DDR_DQ10
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PS_DDR4_DQ12	AU27	PS_DDR_DQ12
PS_DDR4_DQ13	AV26	PS_DDR_DQ13
PS_DDR4_DQ14	AV27	PS_DDR_DQ14
PS_DDR4_DQ15	AW26	PS_DDR_DQ15
PS_DDR4_DQS1_P	AR26	PS_DDR_DQS_P1
PS_DDR4_DQS1_N	AT26	PS_DDR_DQS_N1
PS_DDR4_DQM1	AT27	PS_DDR_DM1
PS_DDR4_DQ16	AP25	PS_DDR_DQ16
PS_DDR4_DQ17	AP24	PS_DDR_DQ17
PS_DDR4_DQ18	AP23	PS_DDR_DQ18
PS_DDR4_DQ19	AN25	PS_DDR_DQ19
PS_DDR4_DQ20	AM25	PS_DDR_DQ20
PS_DDR4_DQ21	AK24	PS_DDR_DQ21
PS_DDR4_DQ22	AN23	PS_DDR_DQ22
PS_DDR4_DQ23	AK23	PS_DDR_DQ23
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PS_DDR4_DQ27	AK27	PS_DDR_DQ27
PS_DDR4_DQ28	AN27	PS_DDR_DQ28
PS_DDR4_DQ29	AN26	PS_DDR_DQ29
PS_DDR4_DQ30	AN28	PS_DDR_DQ30
PS_DDR4_DQ31	AM28	PS_DDR_DQ31
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PS_DDR4_DQ33	AU38	PS_DDR_DQ33
PS_DDR4_DQ34	AU37	PS_DDR_DQ34
PS_DDR4_DQ35	AU35	PS_DDR_DQ35
PS_DDR4_DQ36	AV38	PS_DDR_DQ36
PS_DDR4_DQ37	AW36	PS_DDR_DQ37
PS_DDR4_DQ38	AV35	PS_DDR_DQ38
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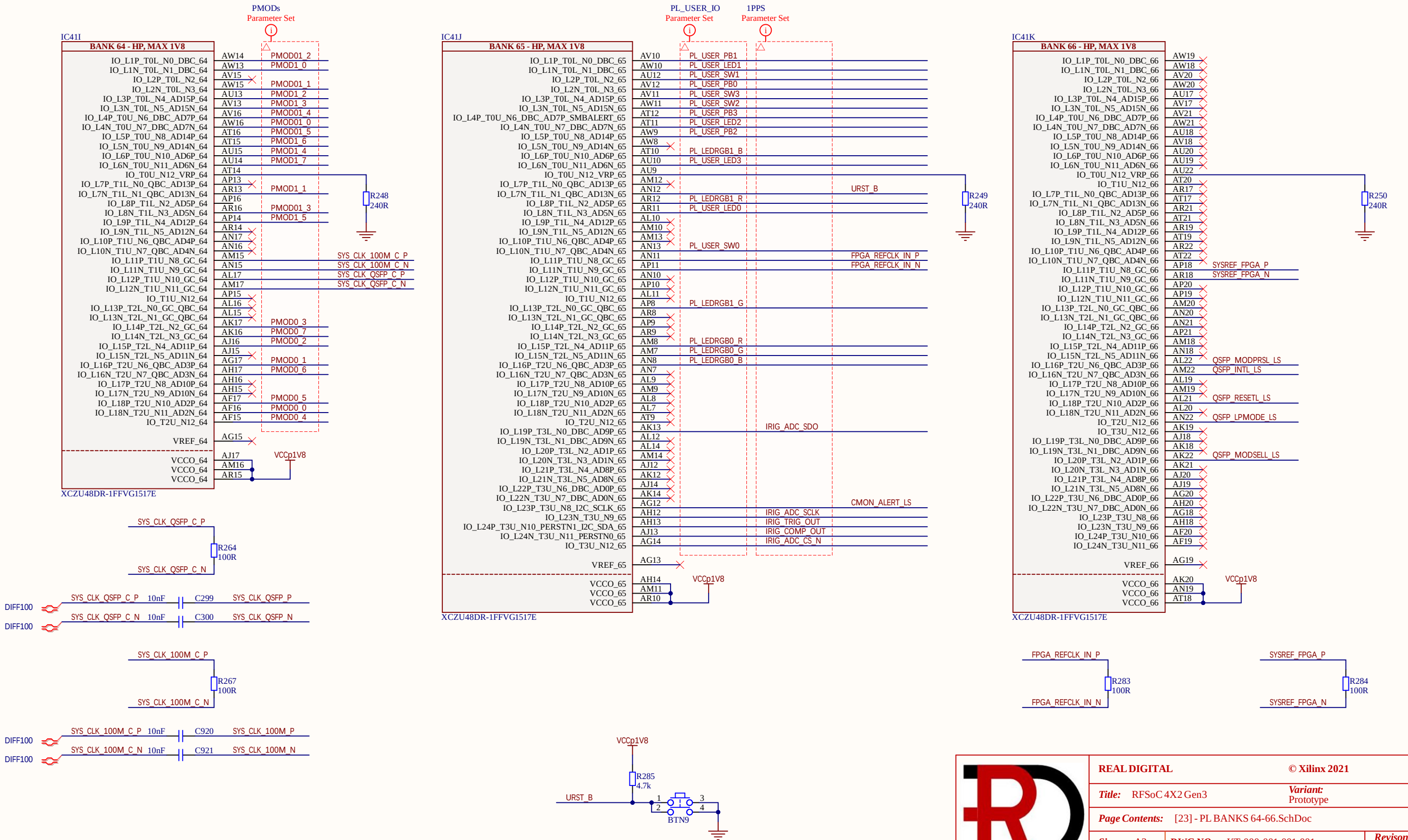
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Size: A3		DWG NO: KT-000-001-001-001			Revision: V2I1
Date: 12/17/2021		Checked by: *		Sheet 21 of 46	

PS: MGT



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	Size: A3	DWG NO: KT-000-001-001-001			Revision: V2I1
	Date: 12/17/2021	Checked by: *		Sheet	22 of 46

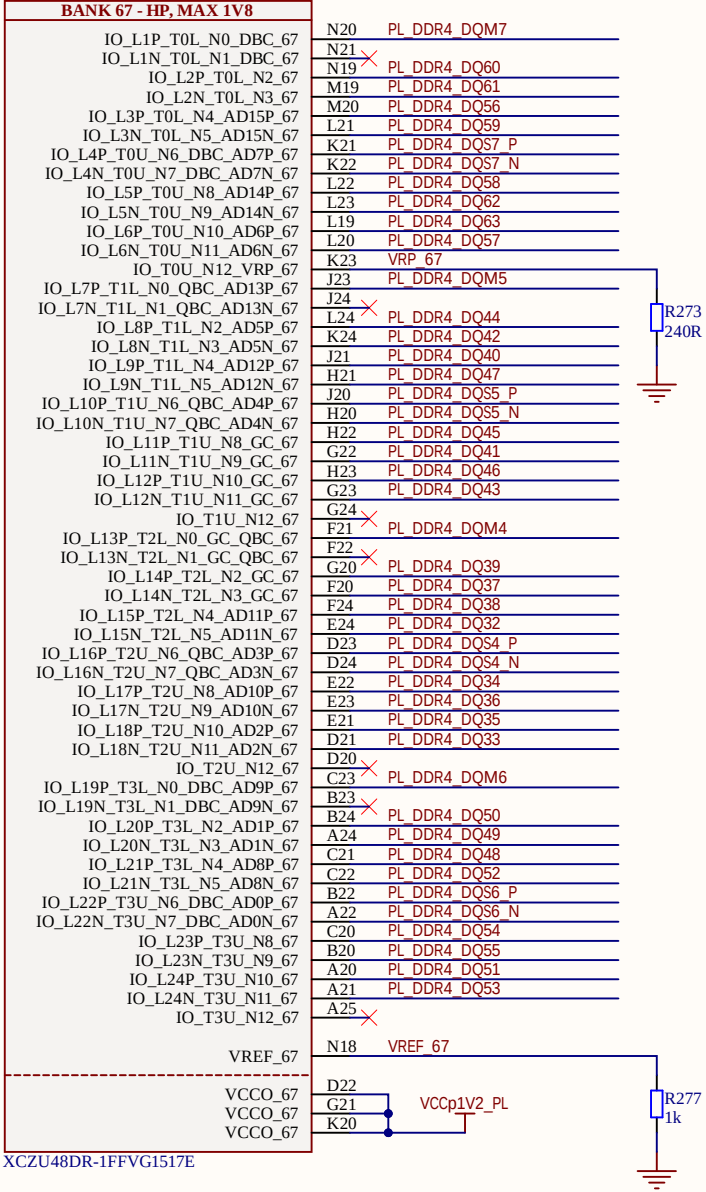
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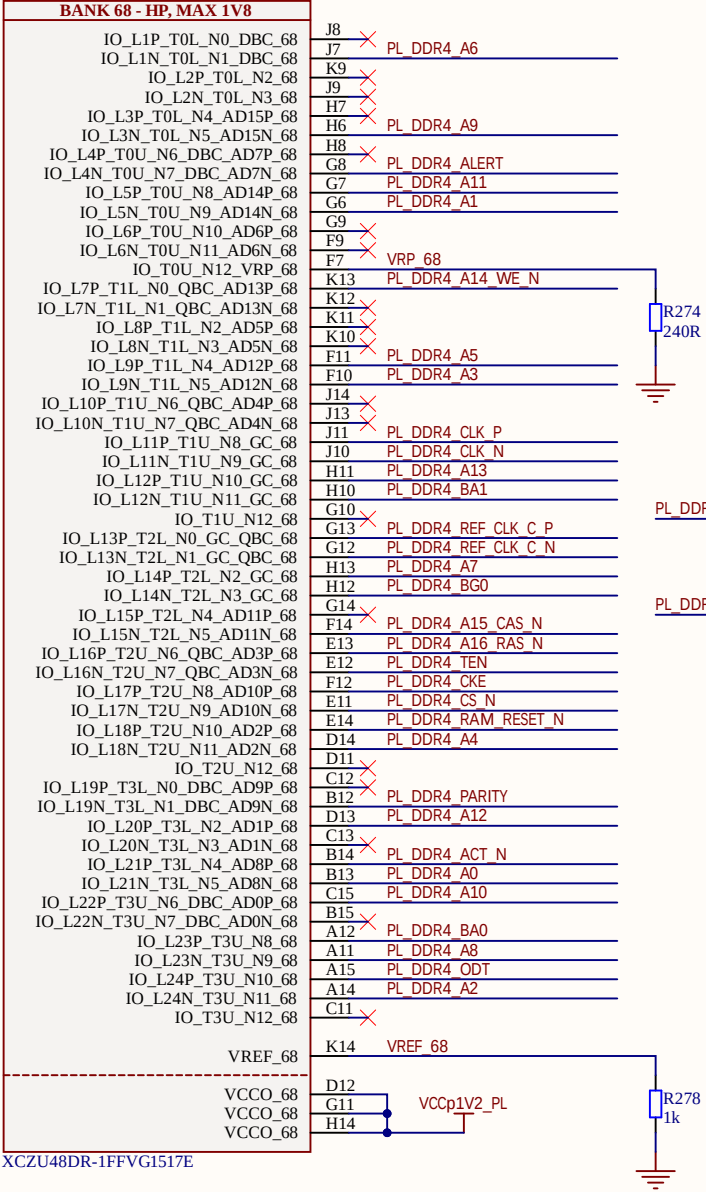
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Date: 12/17/2021	Checked by: *	Sheet 23	of 46

PL: BANKS 67-69

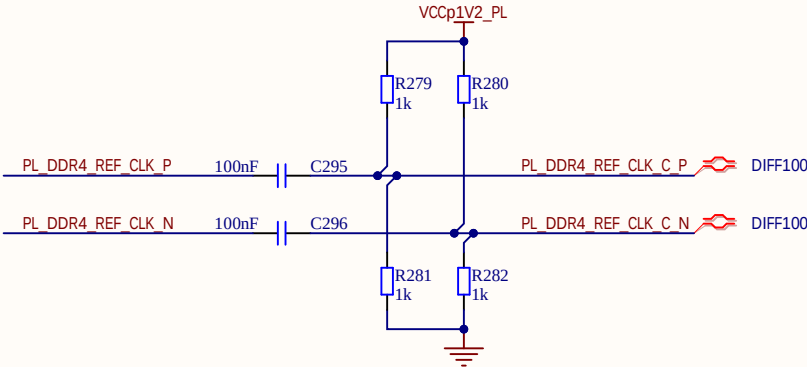
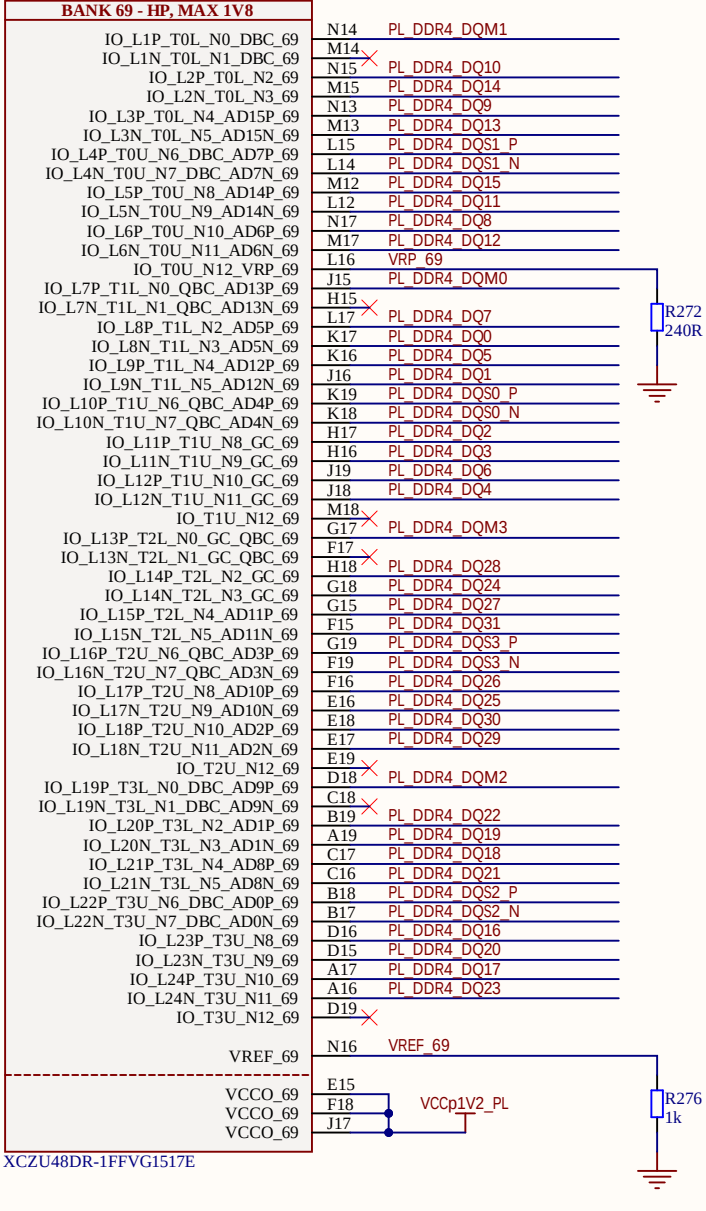
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IC41M

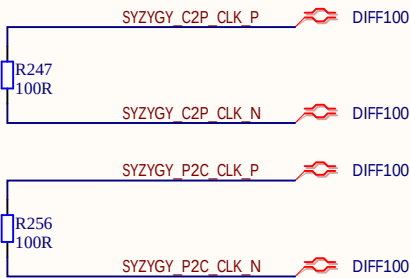
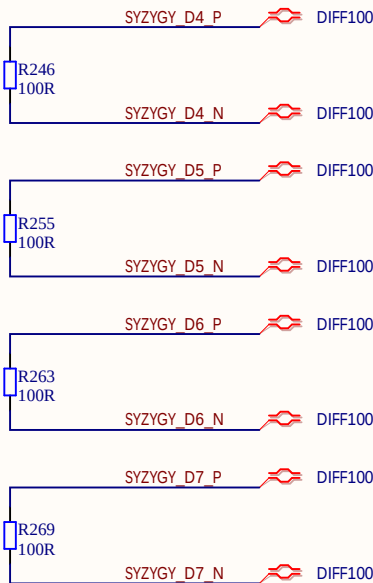
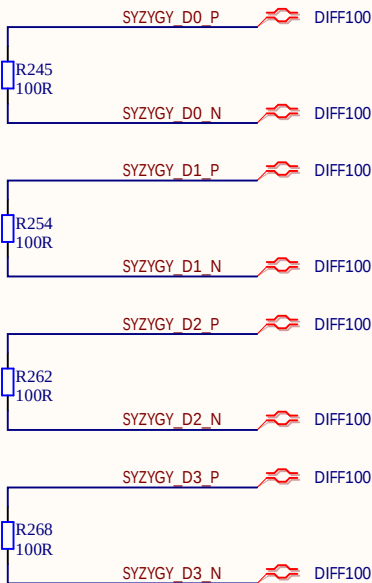
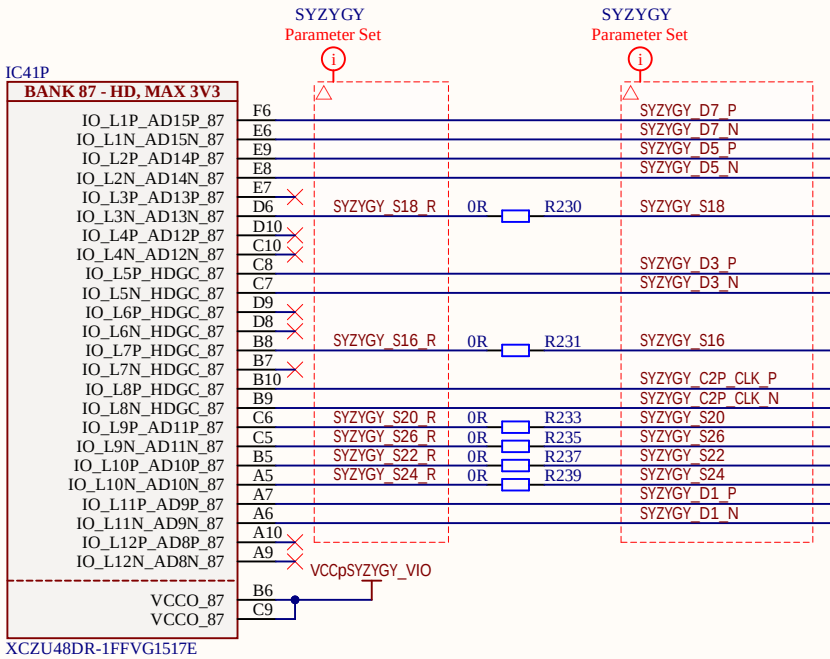
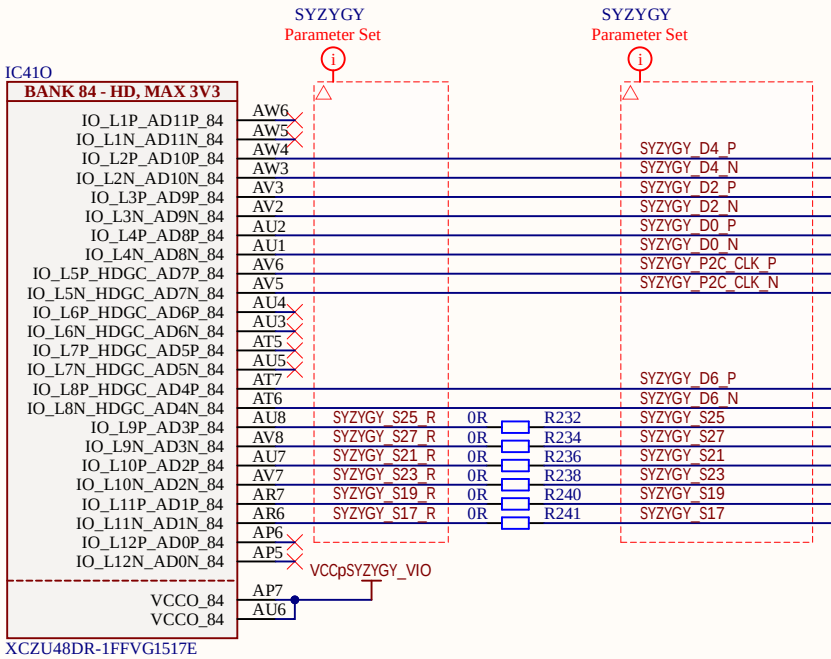


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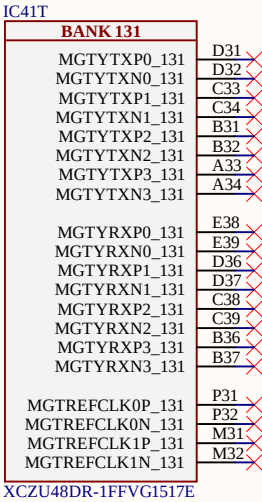
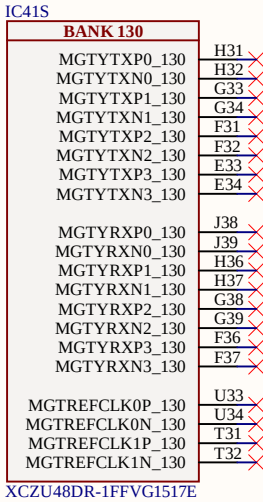
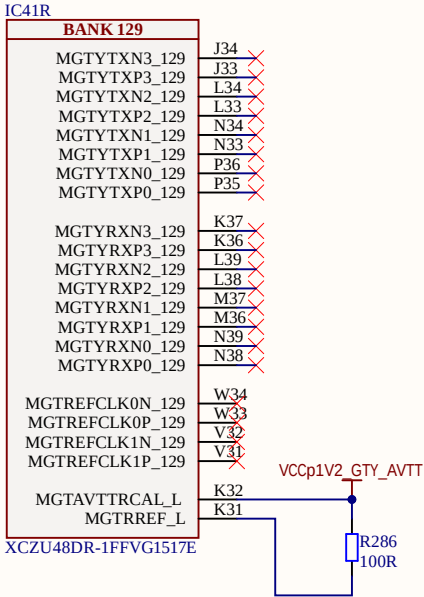
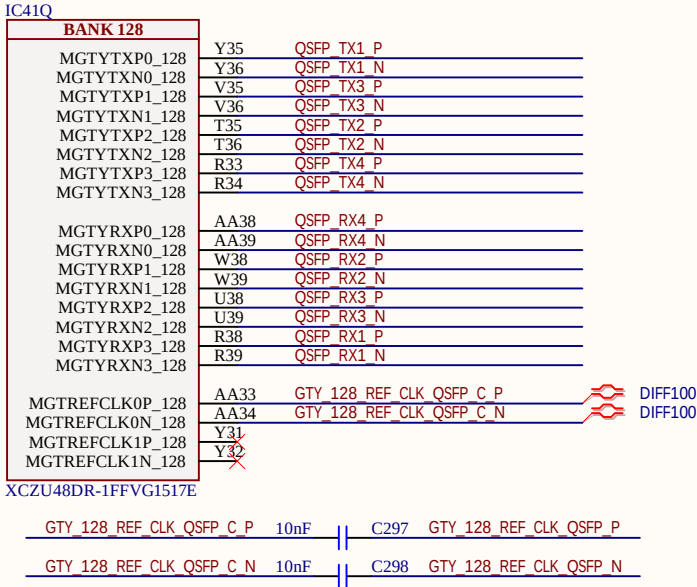
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V211
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PL: BANKS 84, 87



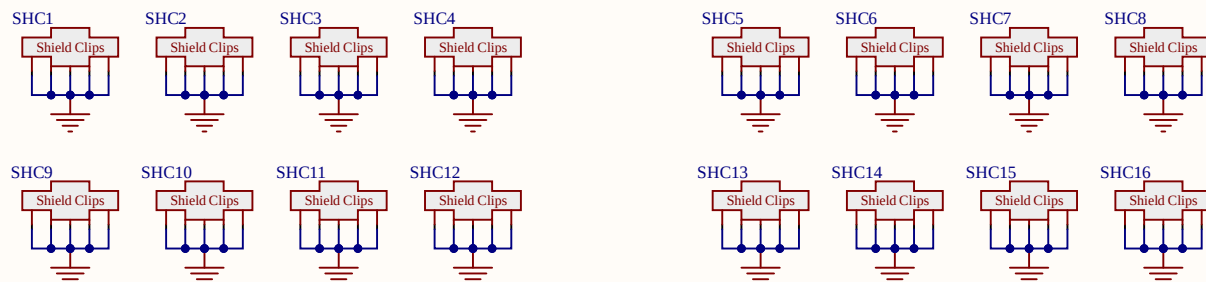
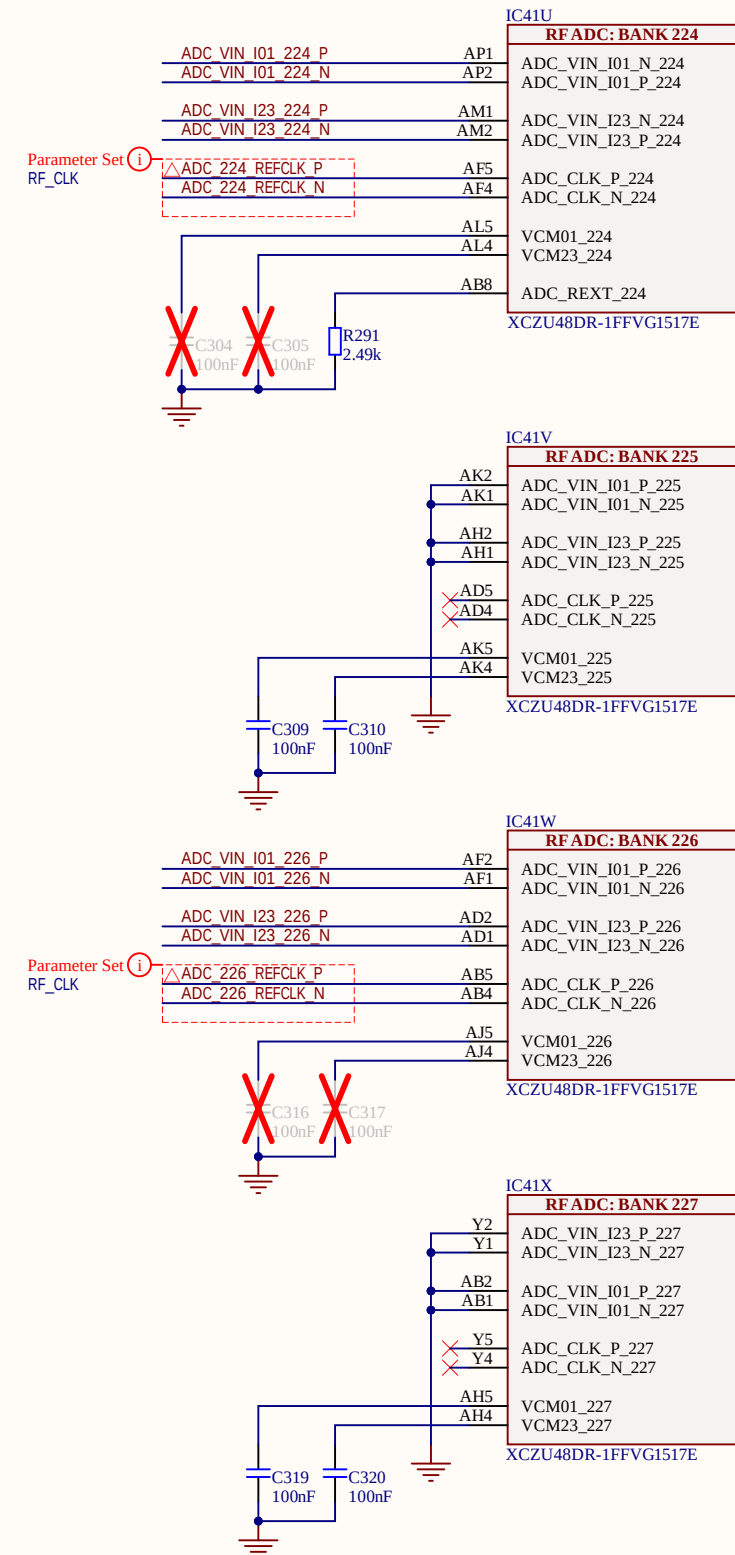
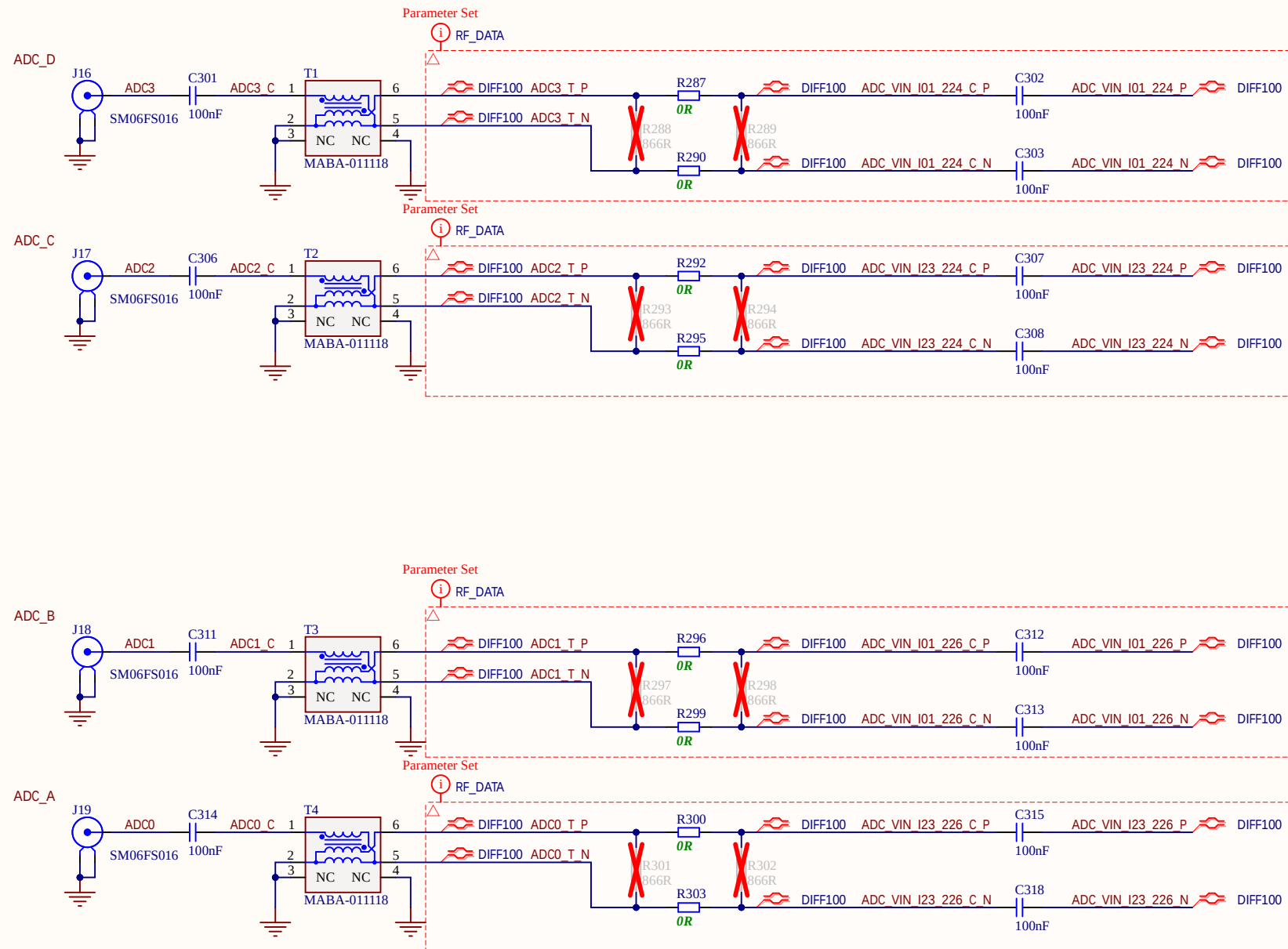
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Date: 12/17/2021		Checked by: *		Sheet 25 of 46	

PL: GTY



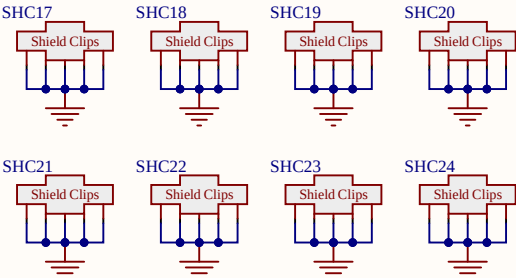
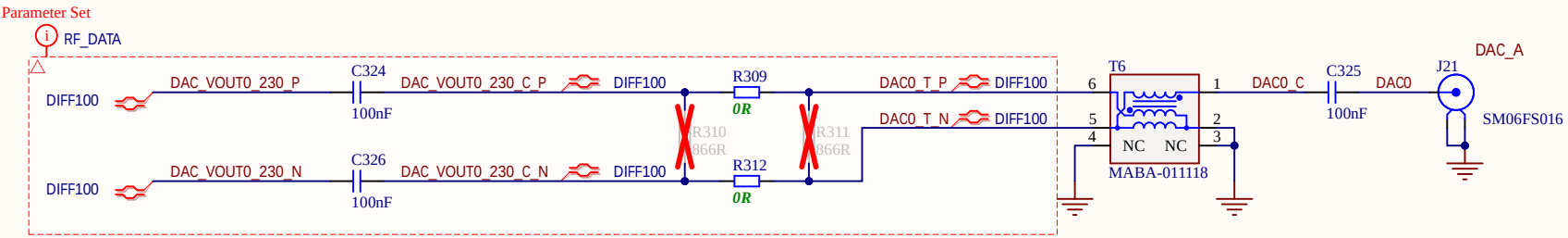
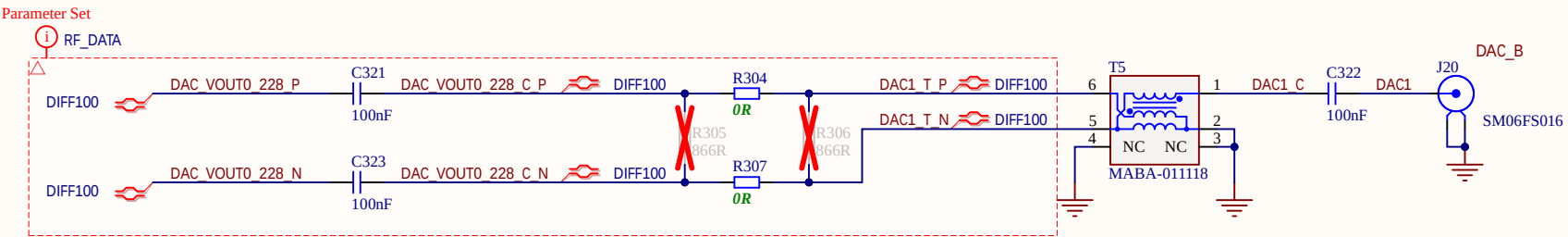
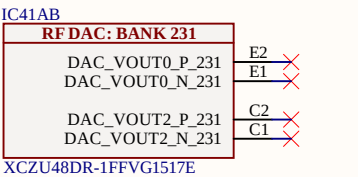
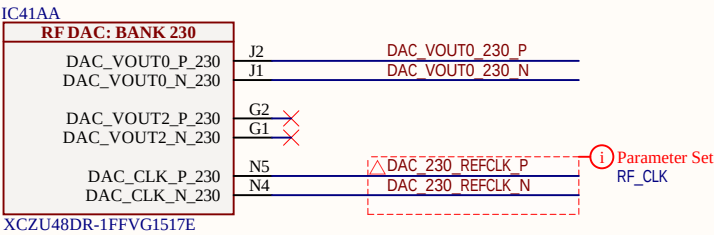
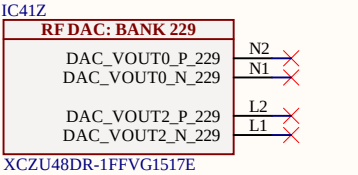
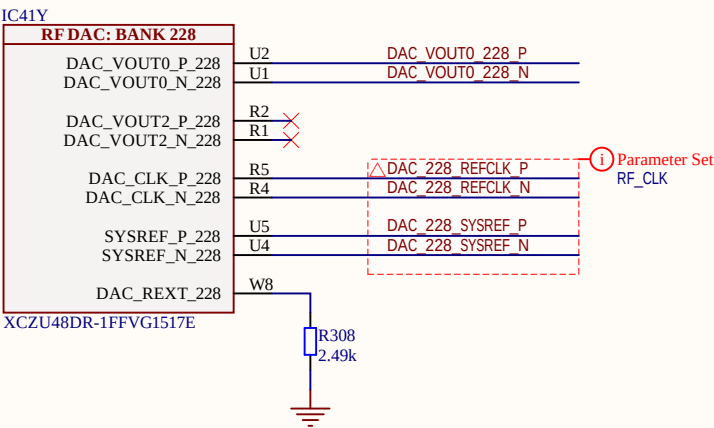
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
Date: 12/17/2021	Checked by: *		Sheet 26 of 46

RF ADC



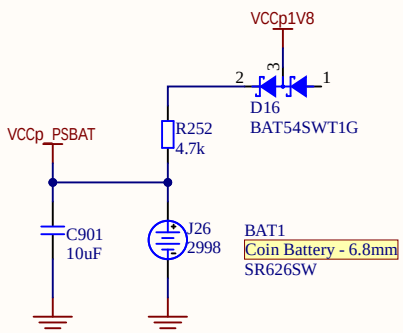
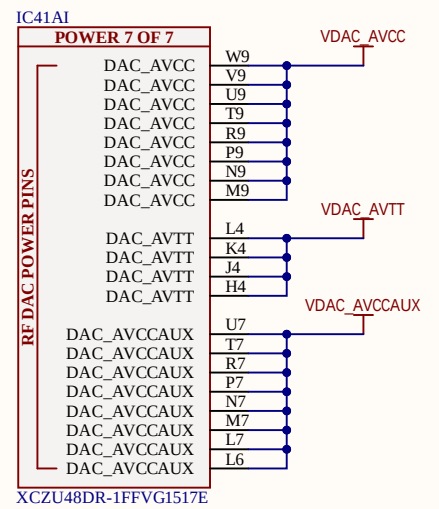
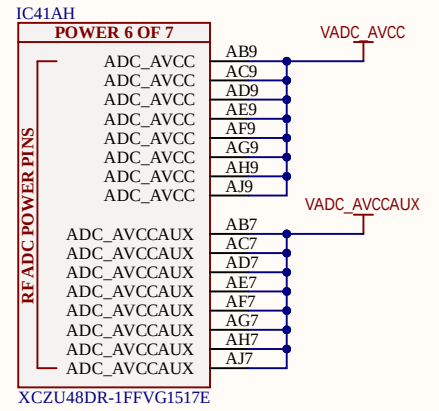
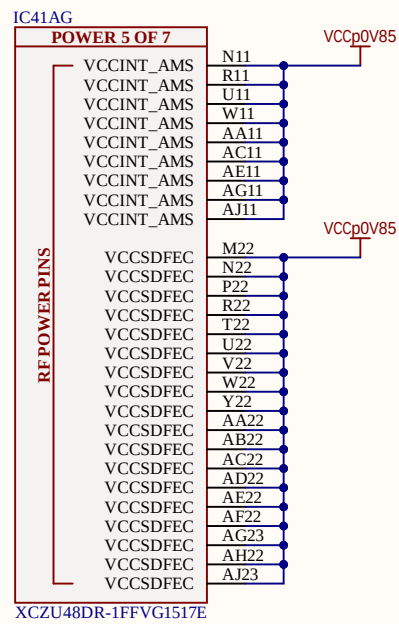
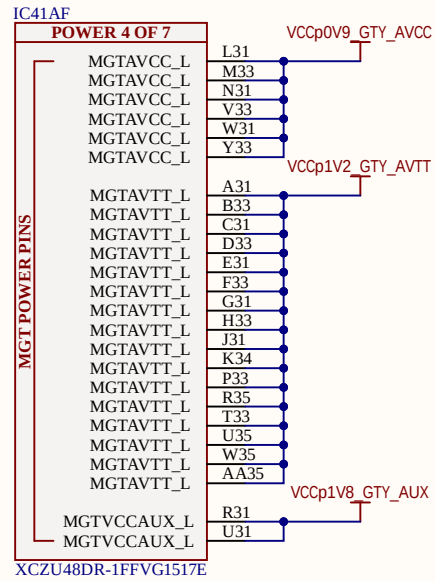
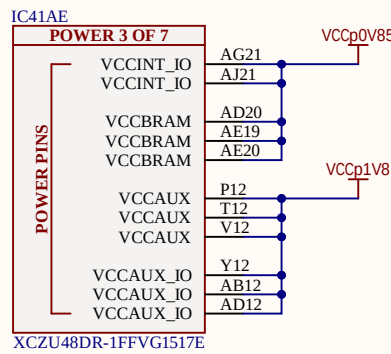
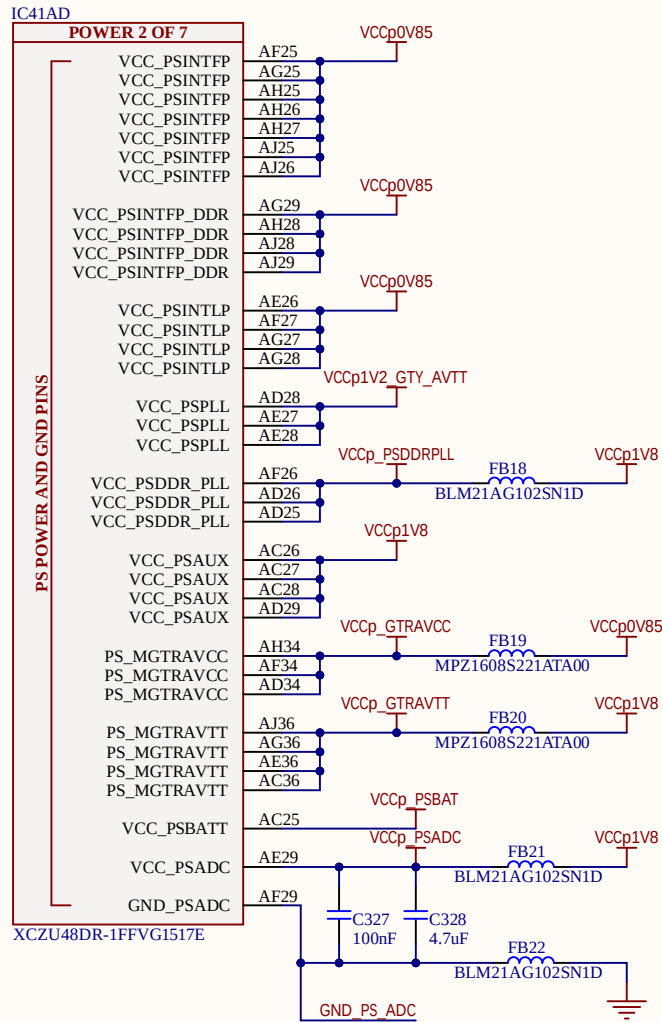
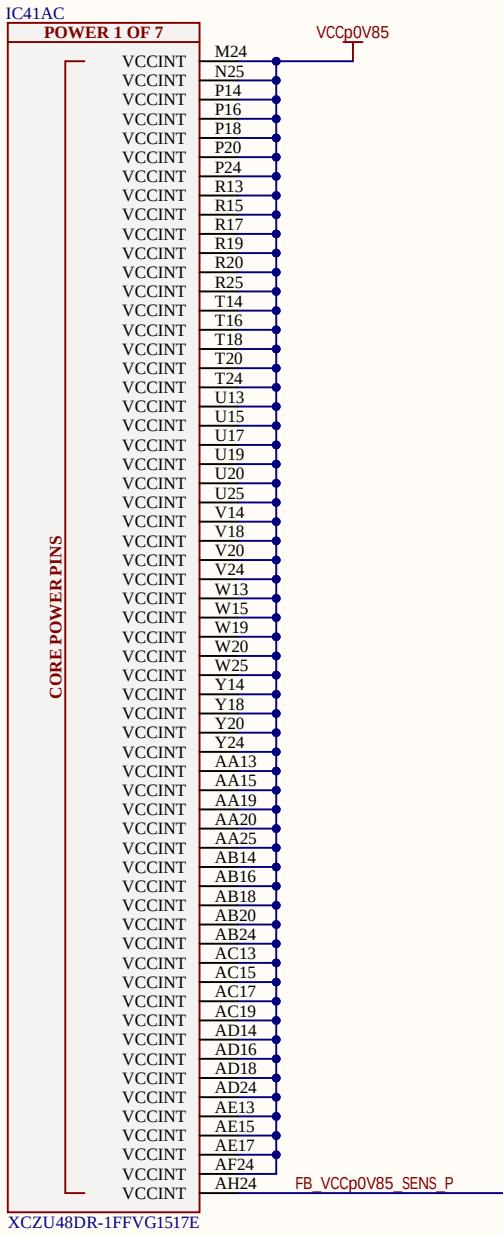
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
Date: 12/17/2021	Checked by: *	Sheet 27	of 46

RF DAC



REAL DIGITAL		© Xilinx 2021	
Title: RFSoC 4X2 Gen3		Variant: Prototype	
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Date: 12/17/2021	Checked by: *		Sheet 28 of 46

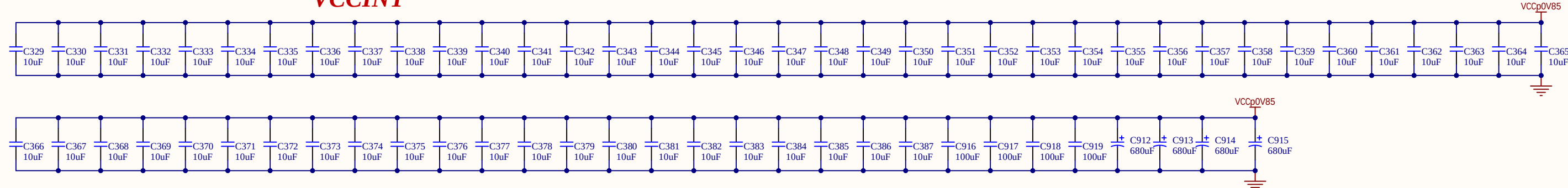
RFSoc POWER Pins



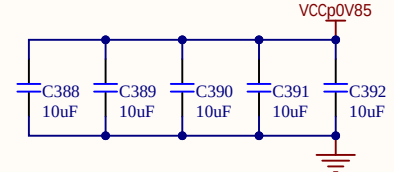
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V211
Date: 12/17/2021	Checked by: *		Sheet 29 of 46

DECOUPLING

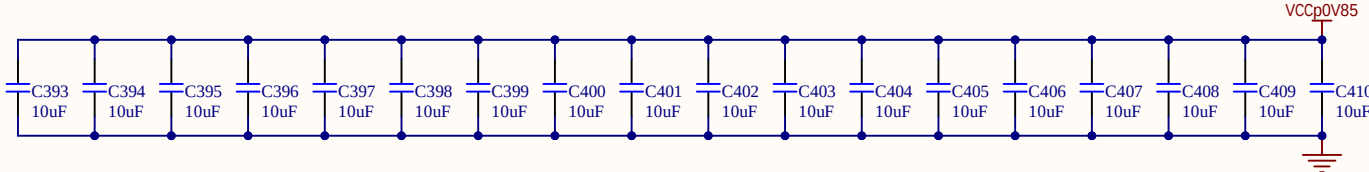
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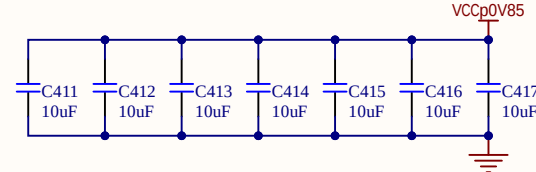
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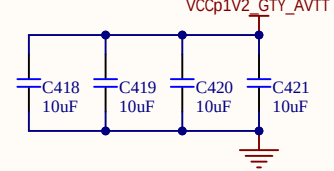
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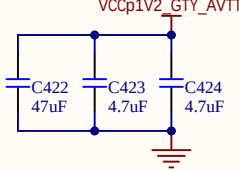
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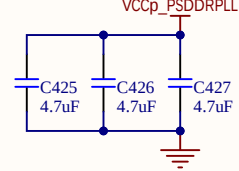
GTY AVTT



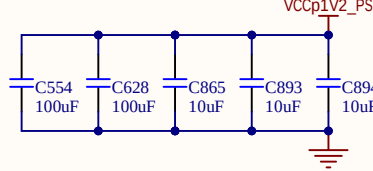
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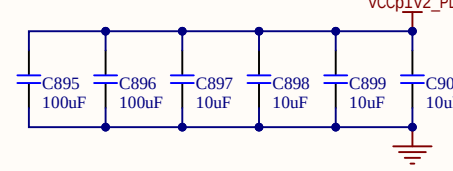
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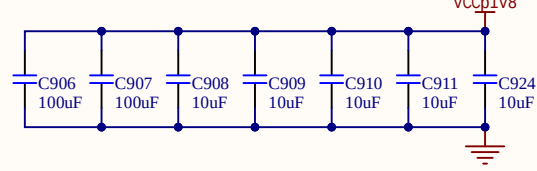
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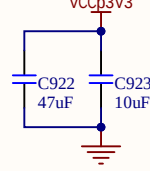
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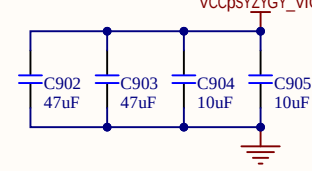
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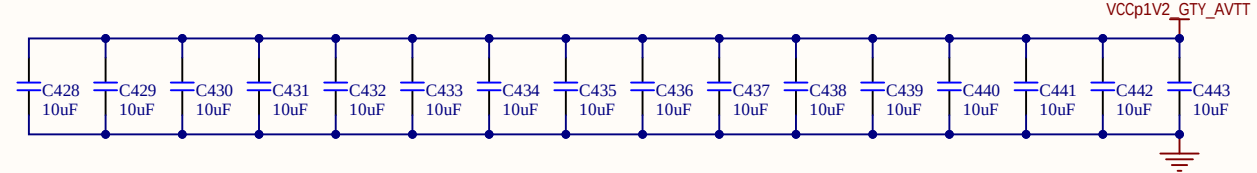
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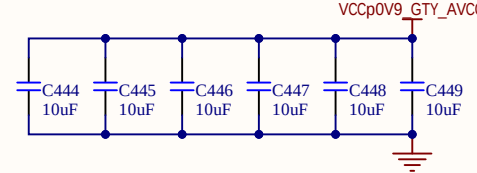
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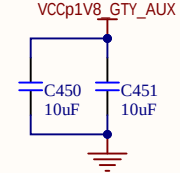
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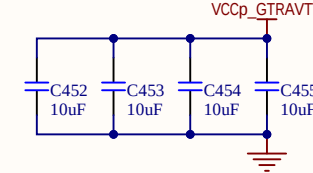
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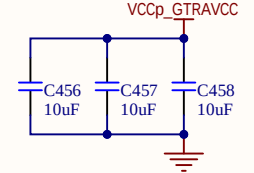
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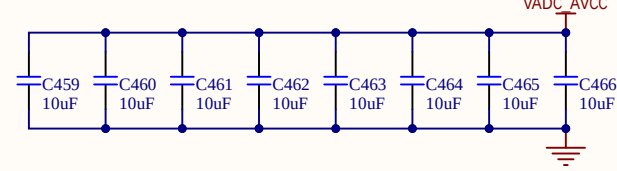
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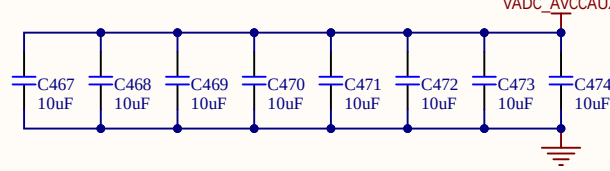
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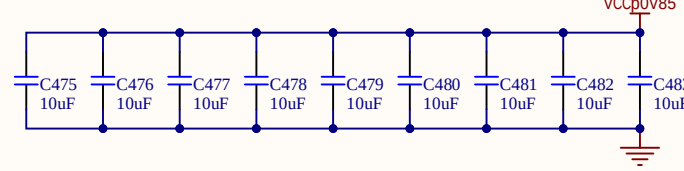
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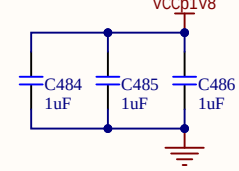
VADC_AVCCAUX



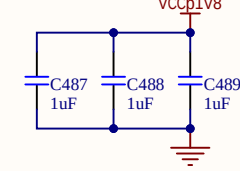
VCCINT_AMS



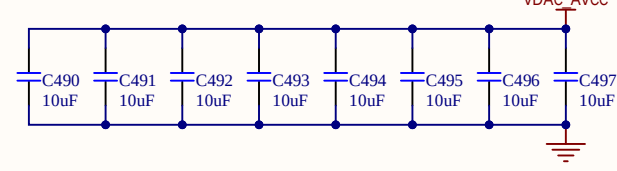
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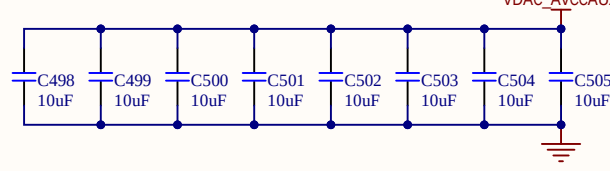
VCCAUX_IO



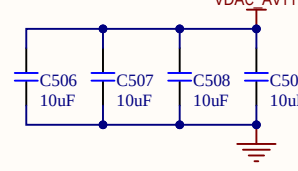
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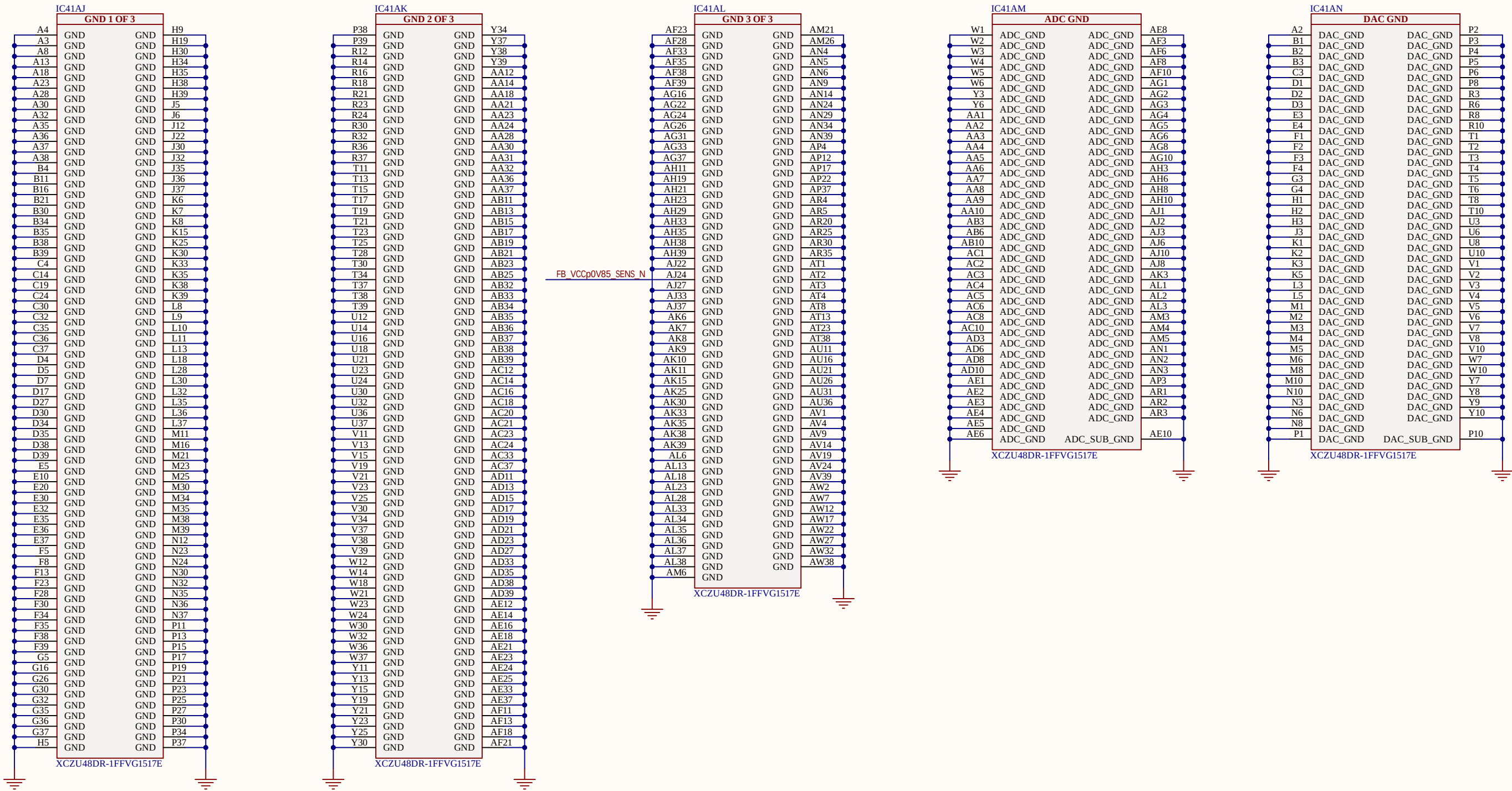


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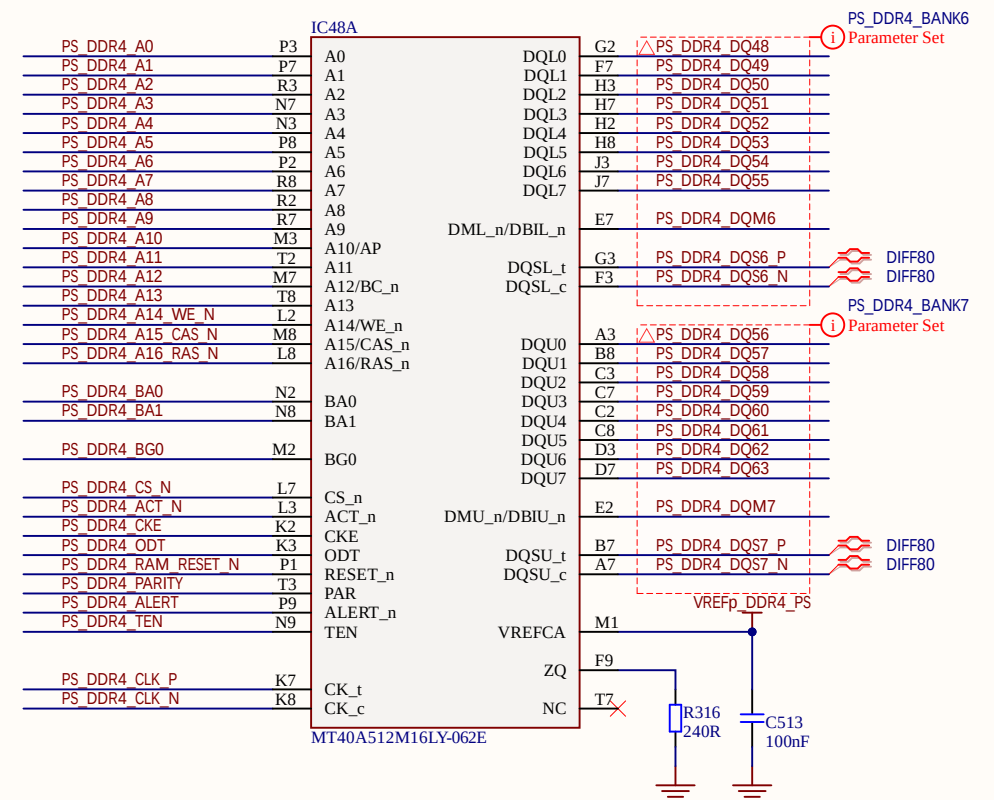
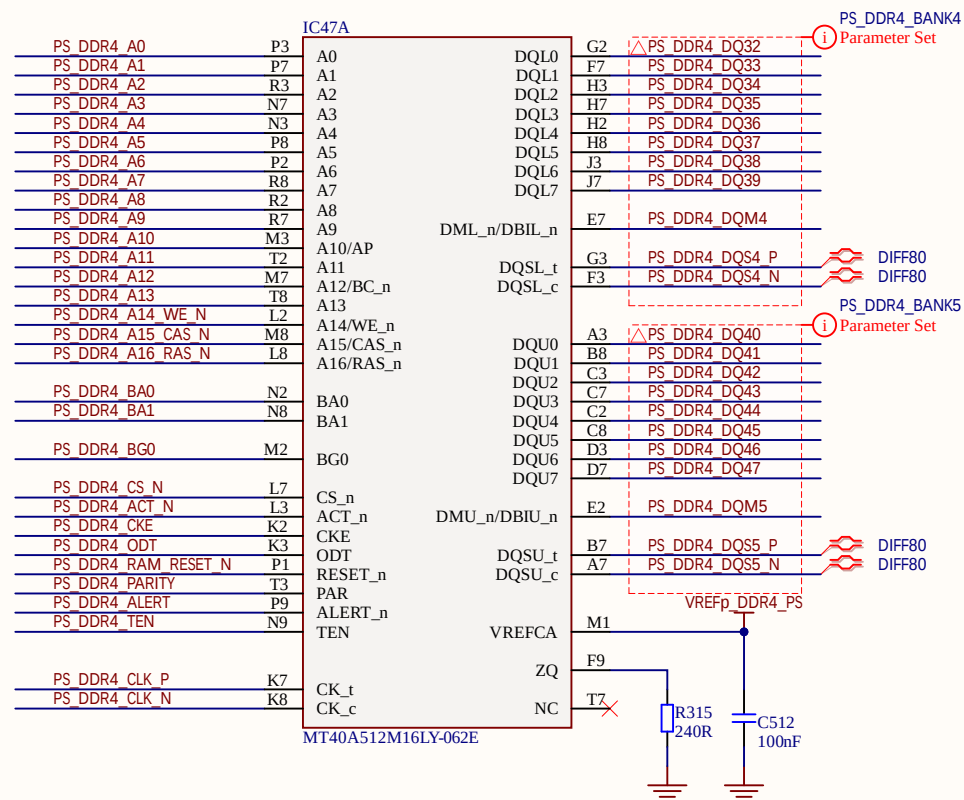
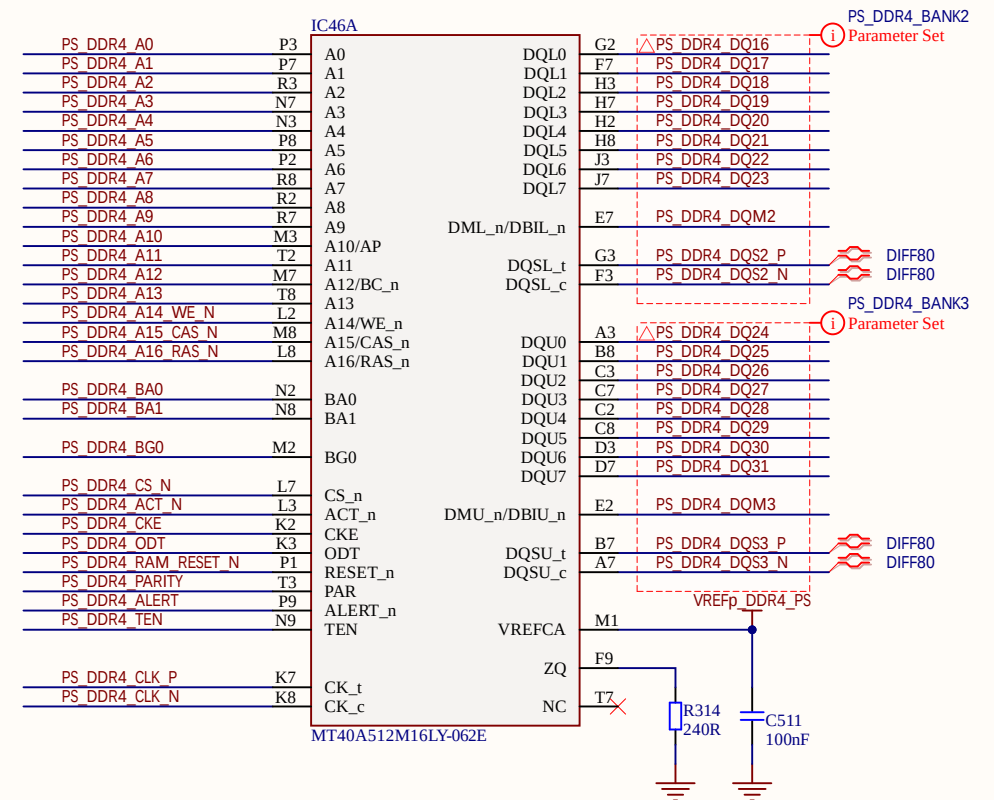
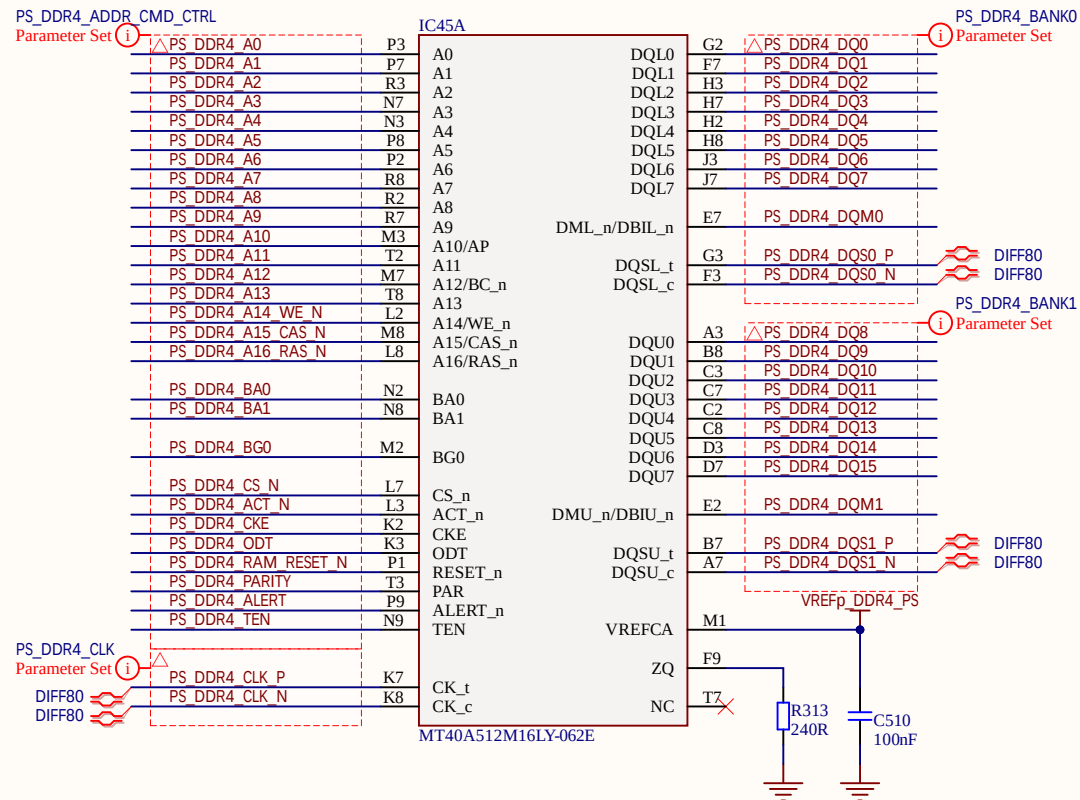
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Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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RFSoc GND Pins



REAL DIGITAL		© Xilinx 2021	
Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [31] - RFSoc GND Pins.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V211
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DDR4 MEMORY PS I



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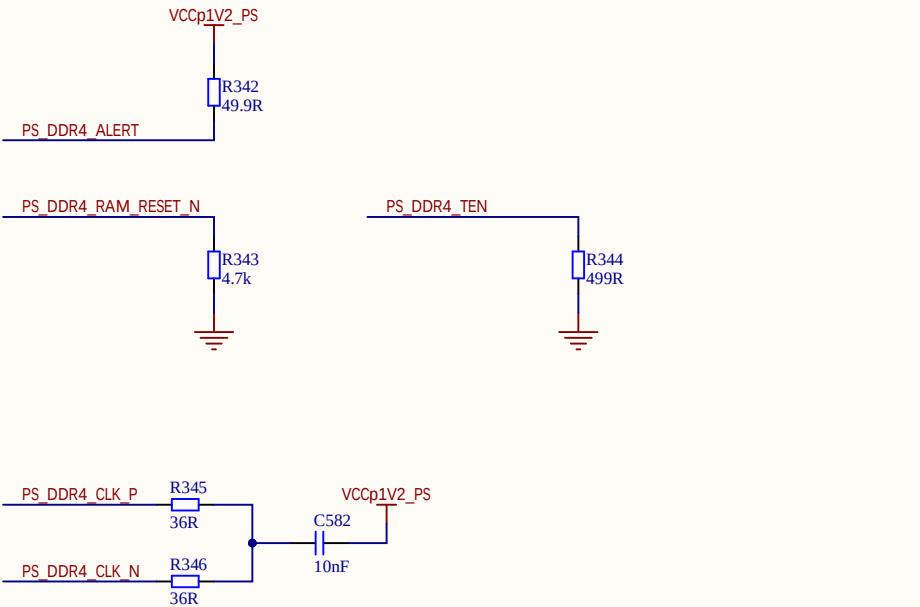
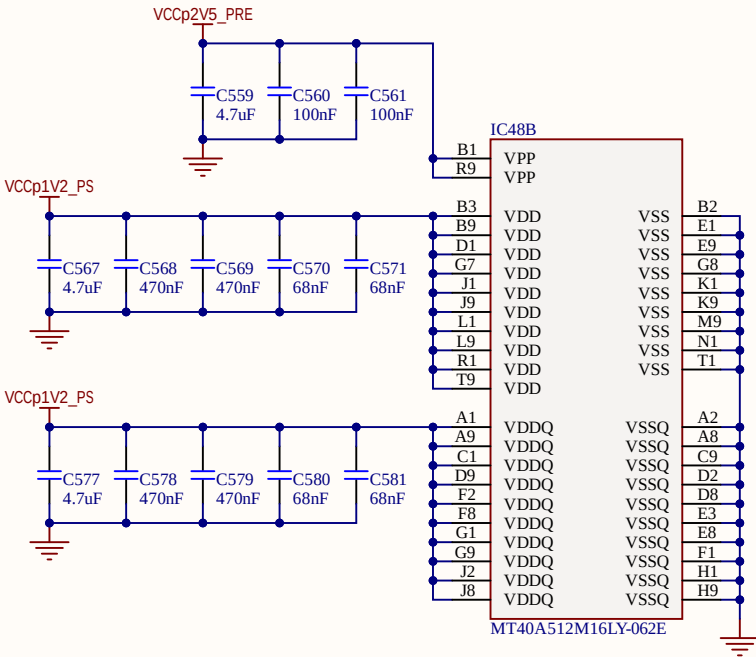
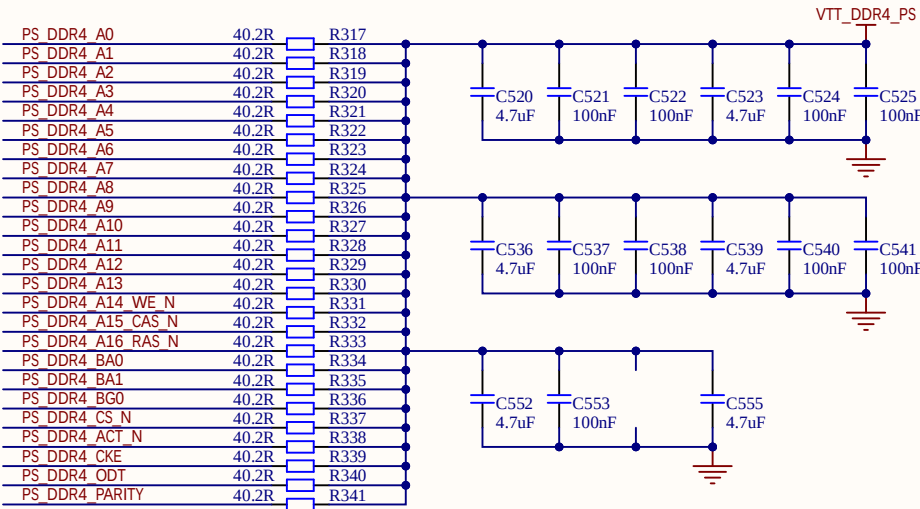
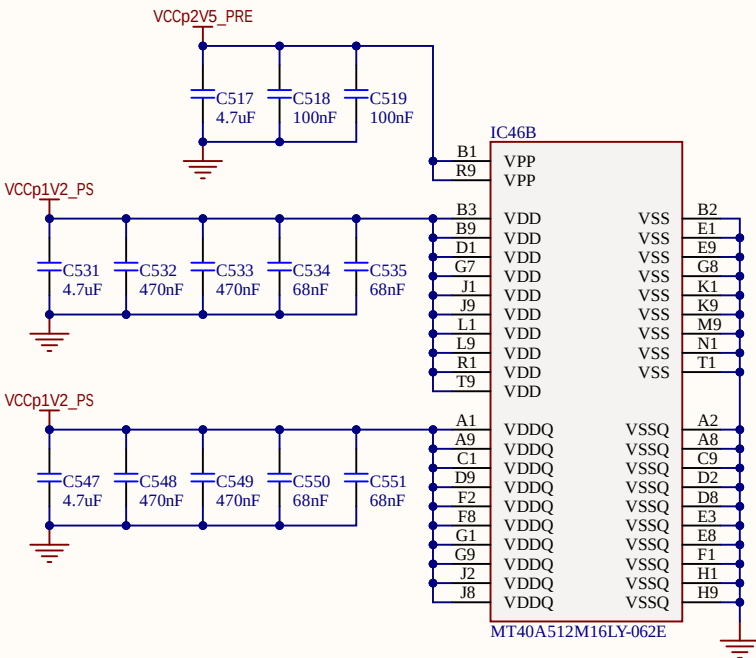
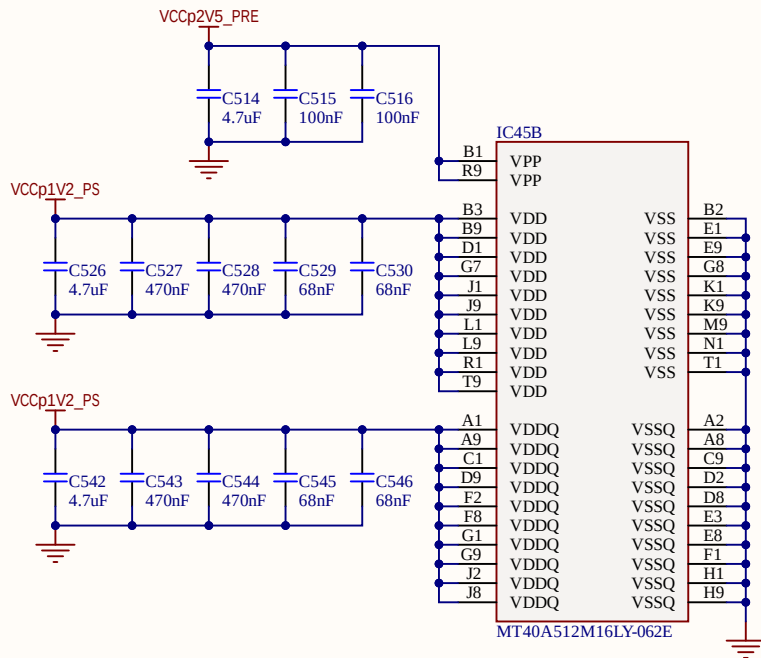
Title: RFSoc 4X2 Gen3	Variant: Prototype
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Page Contents: [32] - DDR4 MEMORY PS I.SchDoc

Size: A3	DWG NO: KT-000-001-001-001	Revision: V211
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Date: 12/17/2021	Checked by: *	Sheet 32 of 46
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DDR4 MEMORY PS II



DDR4 MEMORY PL I

PL_DDR4_ADDR_CMD_CTRL

Parameter Set

PL_DDR4_A0	P3
PL_DDR4_A1	P7
PL_DDR4_A2	R3
PL_DDR4_A3	N7
PL_DDR4_A4	N3
PL_DDR4_A5	P8
PL_DDR4_A6	P2
PL_DDR4_A7	R8
PL_DDR4_A8	R2
PL_DDR4_A9	R7
PL_DDR4_A10	M3
PL_DDR4_A11	T2
PL_DDR4_A12	M7
PL_DDR4_A13	T8
PL_DDR4_A14_WE_N	L2
PL_DDR4_A15_CAS_N	M8
PL_DDR4_A16_RAS_N	L8

PL_DDR4_BA0	N2
PL_DDR4_BA1	N8
PL_DDR4_BG0	M2

PL_DDR4_CS_N	L7
PL_DDR4_ACT_N	L3
PL_DDR4_CKE	K2
PL_DDR4_ODT	K3
PL_DDR4_RAM_RESET_N	P1
PL_DDR4_PARITY	T3
PL_DDR4_ALERT	P9
PL_DDR4_TEN	N9

PL_DDR4_CLK

Parameter Set

DIFF80

DIFF80

PL_DDR4_CLK_P	K7
PL_DDR4_CLK_N	K8

IC49A

A0	DQL0
A1	DQL1
A2	DQL2
A3	DQL3
A4	DQL4
A5	DQL5
A6	DQL6
A7	DQL7
A8	
A9	DML_n/DBIL_n
A10/AP	
A11	DQSL_t
A12/BC_n	DQSL_c
A13	
A14/WE_n	
A15/CAS_n	DQU0
A16/RAS_n	DQU1
	DQU2
	DQU3
	DQU4
	DQU5
	DQU6
	DQU7
BA0	
BA1	
BG0	
CS_n	
ACT_n	DMU_n/DBIU_n
CKE	
ODT	DQSU_t
RESET_n	DQSU_c
PAR	
ALERT_n	VREFCA
TEN	
CK_t	ZQ
CK_c	NC

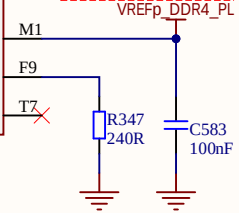
MT40A512M16LY-062E

G2	PL_DDR4_DQ0
F7	PL_DDR4_DQ1
H3	PL_DDR4_DQ2
H7	PL_DDR4_DQ3
H2	PL_DDR4_DQ4
H8	PL_DDR4_DQ5
J3	PL_DDR4_DQ6
J7	PL_DDR4_DQ7
E7	PL_DDR4_DQM0

G3	PL_DDR4_DQS0_P
F3	PL_DDR4_DQS0_N

A3	PL_DDR4_DQ8
B8	PL_DDR4_DQ9
C3	PL_DDR4_DQ10
C7	PL_DDR4_DQ11
C2	PL_DDR4_DQ12
C8	PL_DDR4_DQ13
D3	PL_DDR4_DQ14
D7	PL_DDR4_DQ15
E2	PL_DDR4_DQM1

B7	PL_DDR4_DQS1_P
A7	PL_DDR4_DQS1_N



PL_DDR4_BANK0

Parameter Set

PL_DDR4_DQ0	G2
PL_DDR4_DQ1	F7
PL_DDR4_DQ2	H3
PL_DDR4_DQ3	H7
PL_DDR4_DQ4	H2
PL_DDR4_DQ5	H8
PL_DDR4_DQ6	J3
PL_DDR4_DQ7	J7
PL_DDR4_DQM0	E7

PL_DDR4_DQS0_P	G3
PL_DDR4_DQS0_N	F3

PL_DDR4_DQ8	A3
PL_DDR4_DQ9	B8
PL_DDR4_DQ10	C3
PL_DDR4_DQ11	C7
PL_DDR4_DQ12	C2
PL_DDR4_DQ13	C8
PL_DDR4_DQ14	D3
PL_DDR4_DQ15	D7
PL_DDR4_DQM1	E2

PL_DDR4_DQS1_P	B7
PL_DDR4_DQS1_N	A7



PL_DDR4_BANK4

Parameter Set

PL_DDR4_DQ32	G2
PL_DDR4_DQ33	F7
PL_DDR4_DQ34	H3
PL_DDR4_DQ35	H7
PL_DDR4_DQ36	H2
PL_DDR4_DQ37	H8
PL_DDR4_DQ38	J3
PL_DDR4_DQ39	J7
PL_DDR4_DQM4	E7

PL_DDR4_DQS4_P	G3
PL_DDR4_DQS4_N	F3

PL_DDR4_DQ40	A3
PL_DDR4_DQ41	B8
PL_DDR4_DQ42	C3
PL_DDR4_DQ43	C7
PL_DDR4_DQ44	C2
PL_DDR4_DQ45	C8
PL_DDR4_DQ46	D3
PL_DDR4_DQ47	D7
PL_DDR4_DQM5	E2

PL_DDR4_DQS5_P	B7
PL_DDR4_DQS5_N	A7



PL_DDR4_BANK5

Parameter Set

PL_DDR4_DQ40	A3
PL_DDR4_DQ41	B8
PL_DDR4_DQ42	C3
PL_DDR4_DQ43	C7
PL_DDR4_DQ44	C2
PL_DDR4_DQ45	C8
PL_DDR4_DQ46	D3
PL_DDR4_DQ47	D7
PL_DDR4_DQM5	E2

PL_DDR4_DQS5_P	B7
PL_DDR4_DQS5_N	A7

IC50A

A0	DQL0
A1	DQL1
A2	DQL2
A3	DQL3
A4	DQL4
A5	DQL5
A6	DQL6
A7	DQL7
A8	
A9	DML_n/DBIL_n
A10/AP	
A11	DQSL_t
A12/BC_n	DQSL_c
A13	
A14/WE_n	
A15/CAS_n	DQU0
A16/RAS_n	DQU1
	DQU2
	DQU3
	DQU4
	DQU5
	DQU6
	DQU7
BA0	
BA1	
BG0	
CS_n	
ACT_n	DMU_n/DBIU_n
CKE	
ODT	DQSU_t
RESET_n	DQSU_c
PAR	
ALERT_n	VREFCA
TEN	
CK_t	ZQ
CK_c	NC

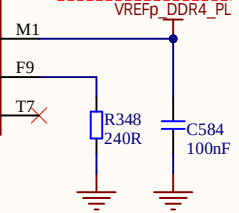
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G2	PL_DDR4_DQ16
F7	PL_DDR4_DQ17
H3	PL_DDR4_DQ18
H7	PL_DDR4_DQ19
H2	PL_DDR4_DQ20
H8	PL_DDR4_DQ21
J3	PL_DDR4_DQ22
J7	PL_DDR4_DQ23
E7	PL_DDR4_DQM2

PL_DDR4_DQS2_P	G3
PL_DDR4_DQS2_N	F3

PL_DDR4_DQ24	A3
PL_DDR4_DQ25	B8
PL_DDR4_DQ26	C3
PL_DDR4_DQ27	C7
PL_DDR4_DQ28	C2
PL_DDR4_DQ29	C8
PL_DDR4_DQ30	D3
PL_DDR4_DQ31	D7
PL_DDR4_DQM3	E2

PL_DDR4_DQS3_P	B7
PL_DDR4_DQS3_N	A7



IC52A

A0	DQL0
A1	DQL1
A2	DQL2
A3	DQL3
A4	DQL4
A5	DQL5
A6	DQL6
A7	DQL7
A8	
A9	DML_n/DBIL_n
A10/AP	
A11	DQSL_t
A12/BC_n	DQSL_c
A13	
A14/WE_n	
A15/CAS_n	DQU0
A16/RAS_n	DQU1
	DQU2
	DQU3
	DQU4
	DQU5
	DQU6
	DQU7
BA0	
BA1	
BG0	
CS_n	
ACT_n	DMU_n/DBIU_n
CKE	
ODT	DQSU_t
RESET_n	DQSU_c
PAR	
ALERT_n	VREFCA
TEN	
CK_t	ZQ
CK_c	NC

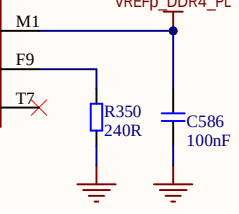
MT40A512M16LY-062E

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F7	PL_DDR4_DQ49
H3	PL_DDR4_DQ50
H7	PL_DDR4_DQ51
H2	PL_DDR4_DQ52
H8	PL_DDR4_DQ53
J3	PL_DDR4_DQ54
J7	PL_DDR4_DQ55
E7	PL_DDR4_DQM6

PL_DDR4_DQS6_P	G3
PL_DDR4_DQS6_N	F3

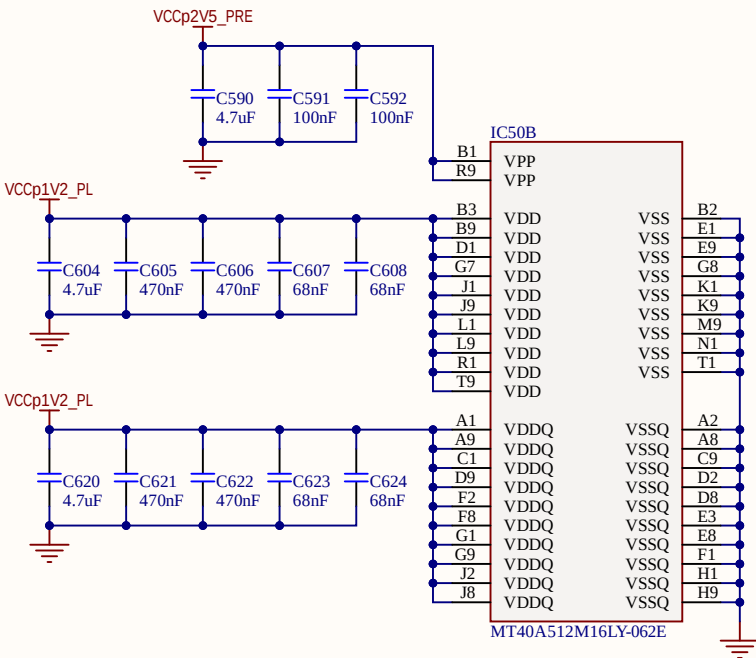
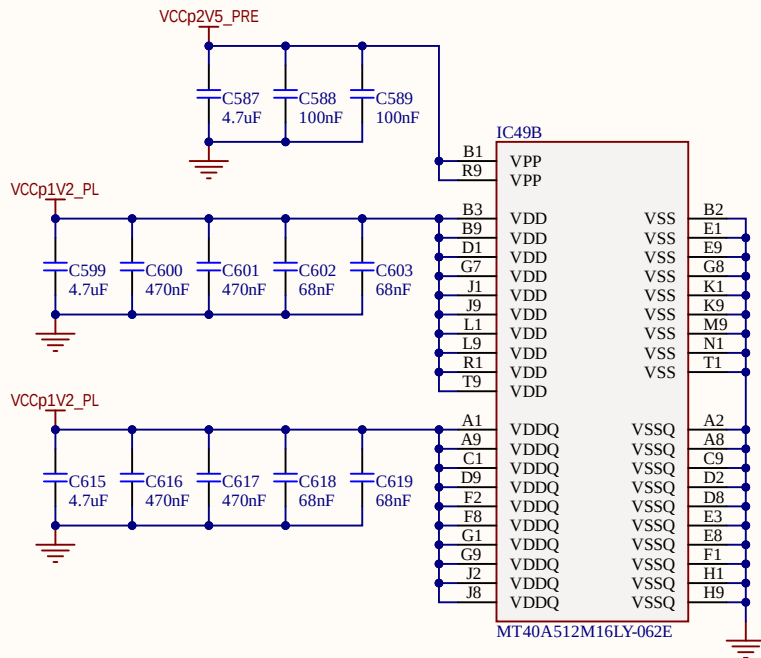
PL_DDR4_DQ56	A3
PL_DDR4_DQ57	B8
PL_DDR4_DQ58	C3
PL_DDR4_DQ59	C7
PL_DDR4_DQ60	C2
PL_DDR4_DQ61	C8
PL_DDR4_DQ62	D3
PL_DDR4_DQ63	D7
PL_DDR4_DQM7	E2

PL_DDR4_DQS7_P	B7
PL_DDR4_DQS7_N	A7

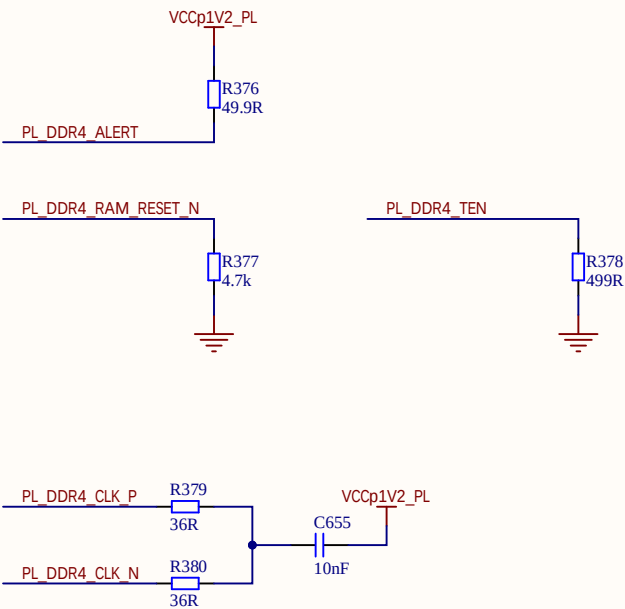
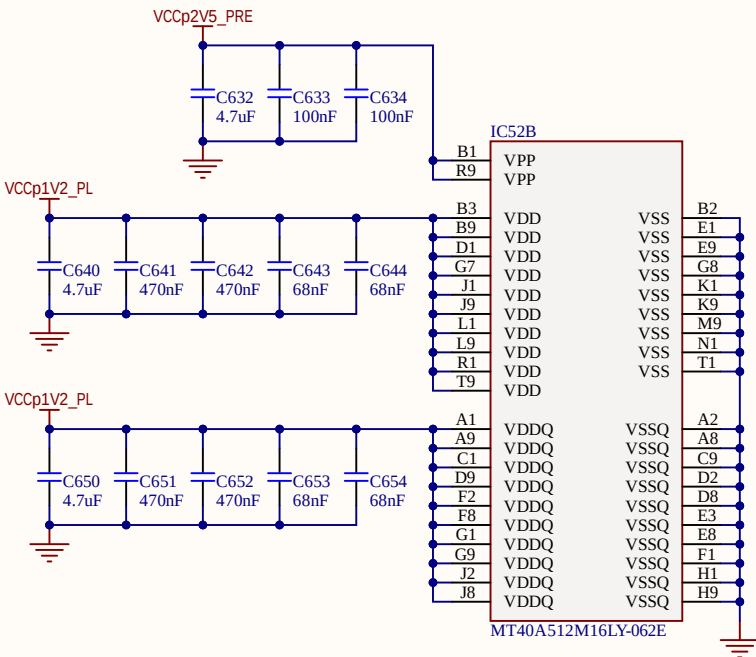
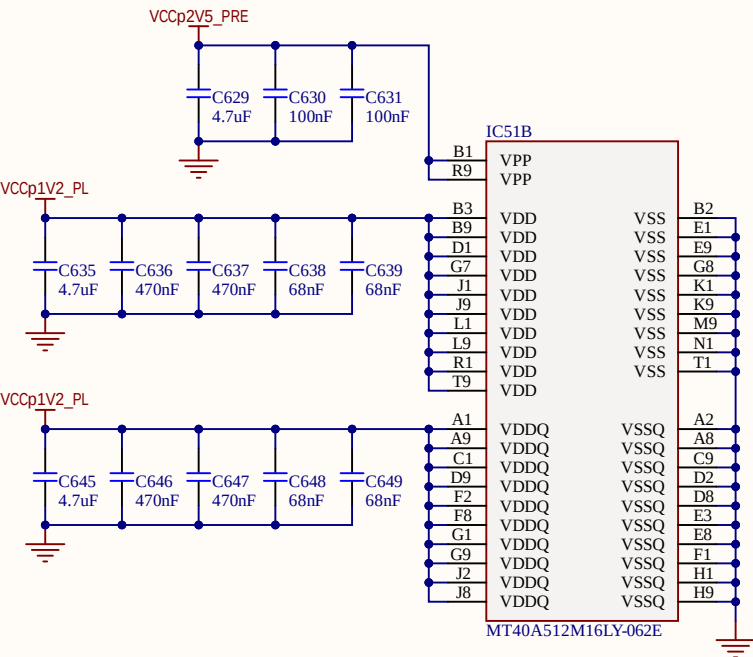


REAL DIGITAL		© Xilinx 2021	
Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [34] - DDR4 MEMORY PL I.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
Date: 12/17/2021	Checked by: *	Sheet 34	of 46

DDR4 MEMORY PL II



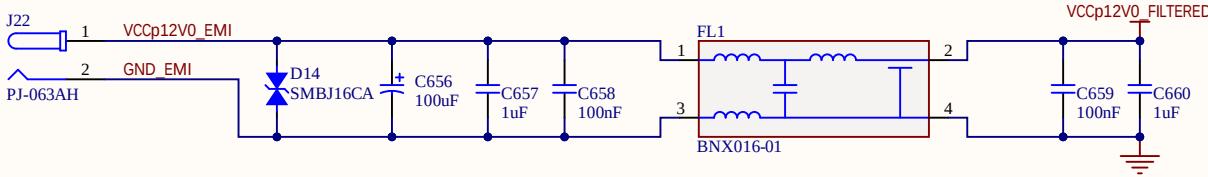
PL DDR4 A0	40.2R	R351
PL DDR4 A1	40.2R	R352
PL DDR4 A2	40.2R	R353
PL DDR4 A3	40.2R	R354
PL DDR4 A4	40.2R	R355
PL DDR4 A5	40.2R	R356
PL DDR4 A6	40.2R	R357
PL DDR4 A7	40.2R	R358
PL DDR4 A8	40.2R	R359
PL DDR4 A9	40.2R	R360
PL DDR4 A10	40.2R	R361
PL DDR4 A11	40.2R	R362
PL DDR4 A12	40.2R	R363
PL DDR4 A13	40.2R	R364
PL DDR4 A14 WE N	40.2R	R365
PL DDR4 A15 CAS N	40.2R	R366
PL DDR4 A16 RAS N	40.2R	R367
PL DDR4 BA0	40.2R	R368
PL DDR4 BA1	40.2R	R369
PL DDR4 BG0	40.2R	R370
PL DDR4 CS N	40.2R	R371
PL DDR4 ACT N	40.2R	R372
PL DDR4 CKE	40.2R	R373
PL DDR4 ODT	40.2R	R374
PL DDR4 PARITY	40.2R	R375



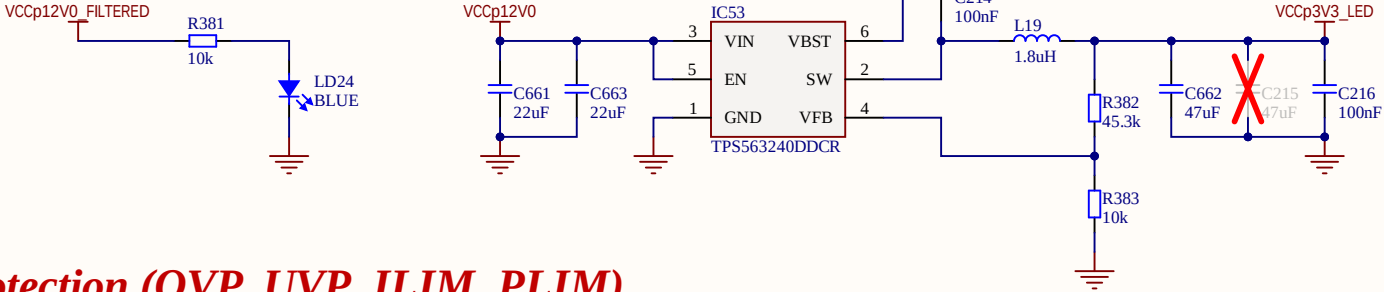
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Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [35] - DDR4 MEMORY PL II.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V211
Date: 12/17/2021	Checked by: *	Sheet 35	of 46

POWER INPUT AND FAN CONTROLLER

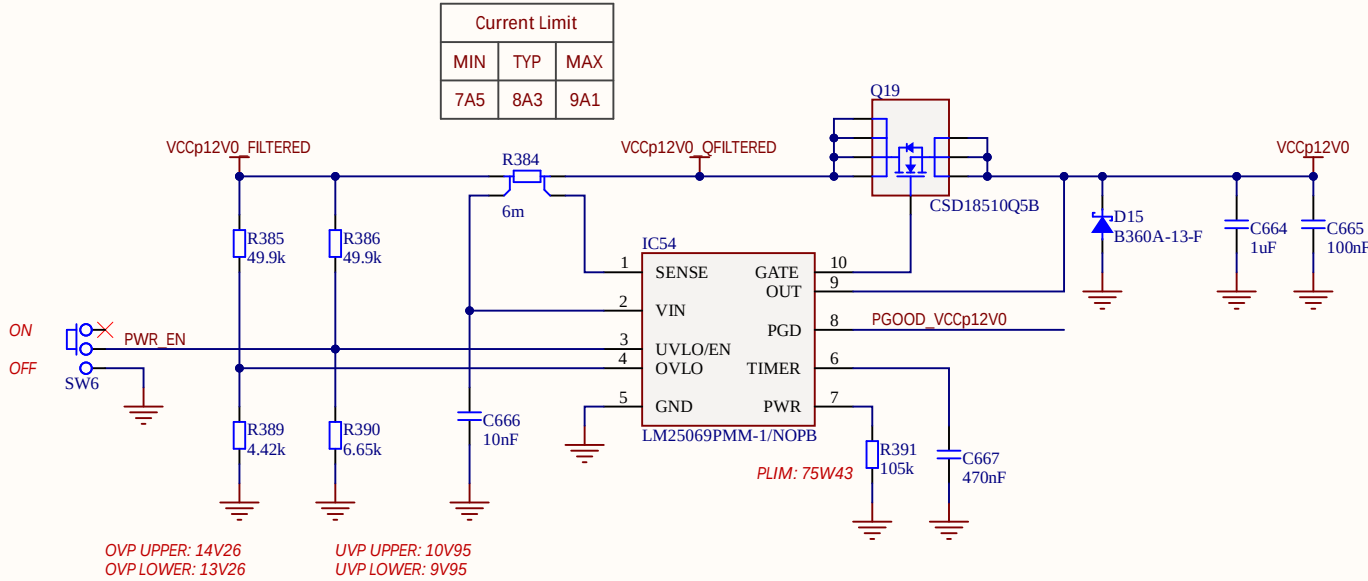
EMI Filter



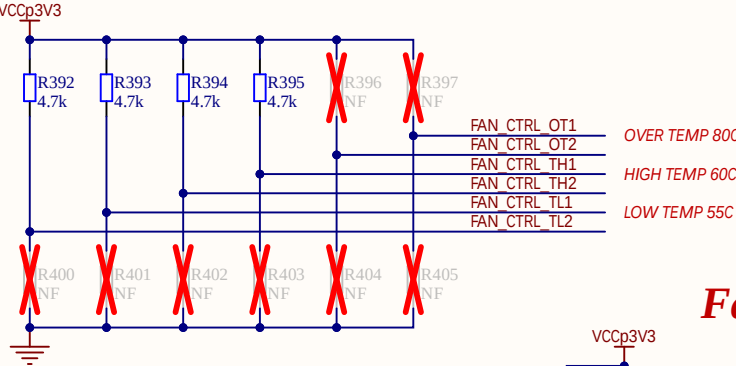
12V0 LED



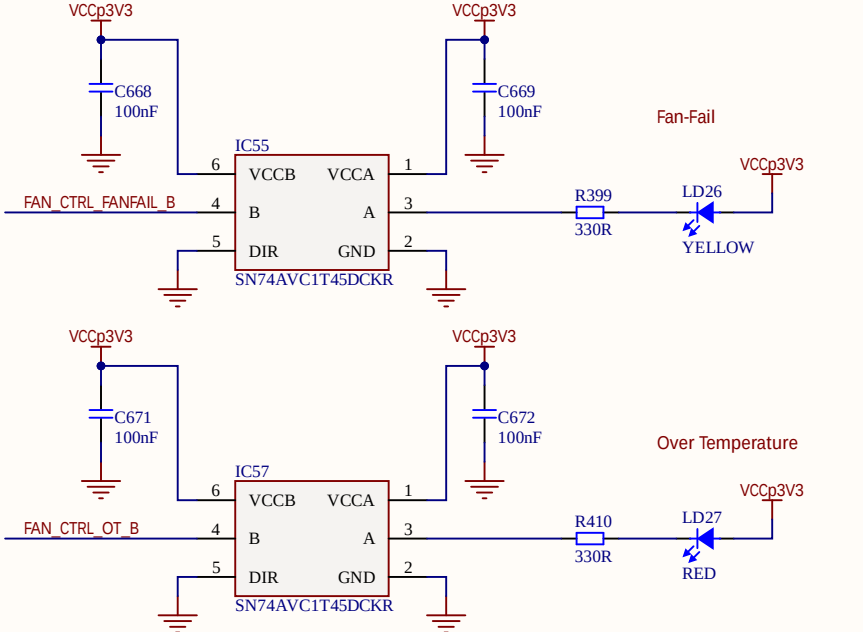
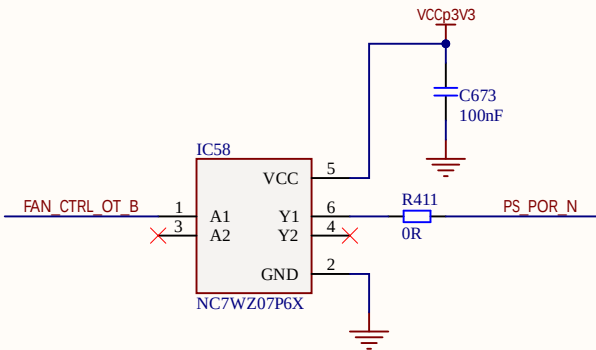
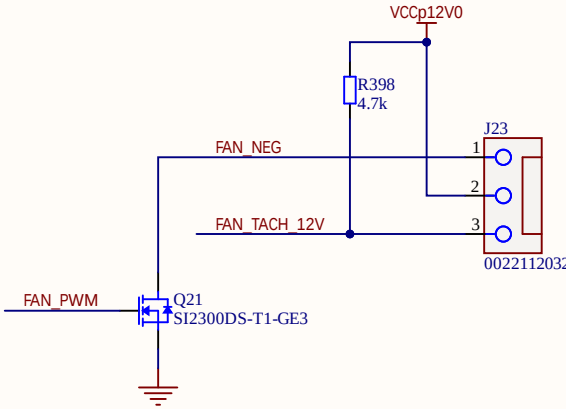
Input Protection (OVP, UVP, ILIM, PLIM)



HS1
Heatsink+Fan
FA+K30B+T725

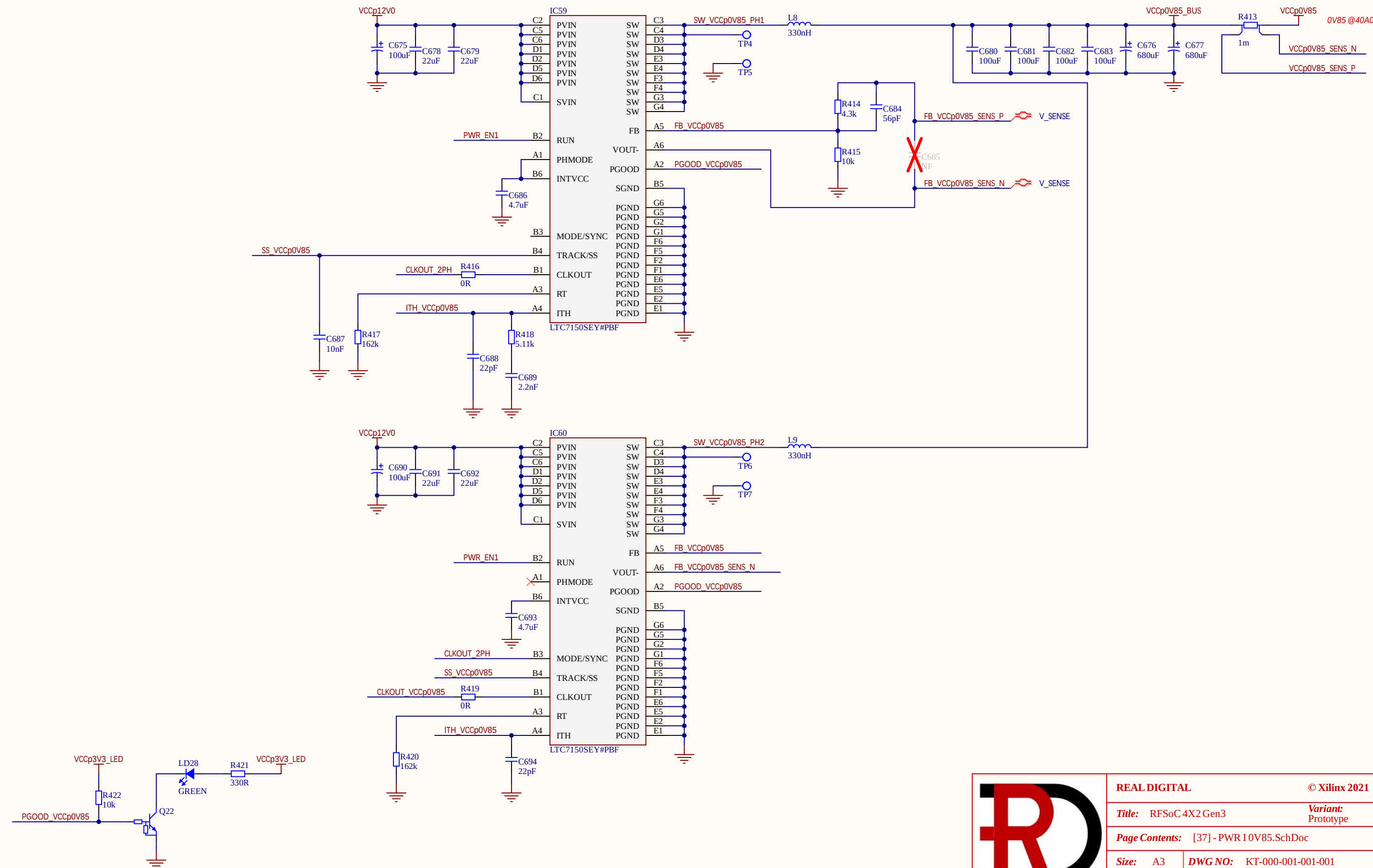


Fan Controller



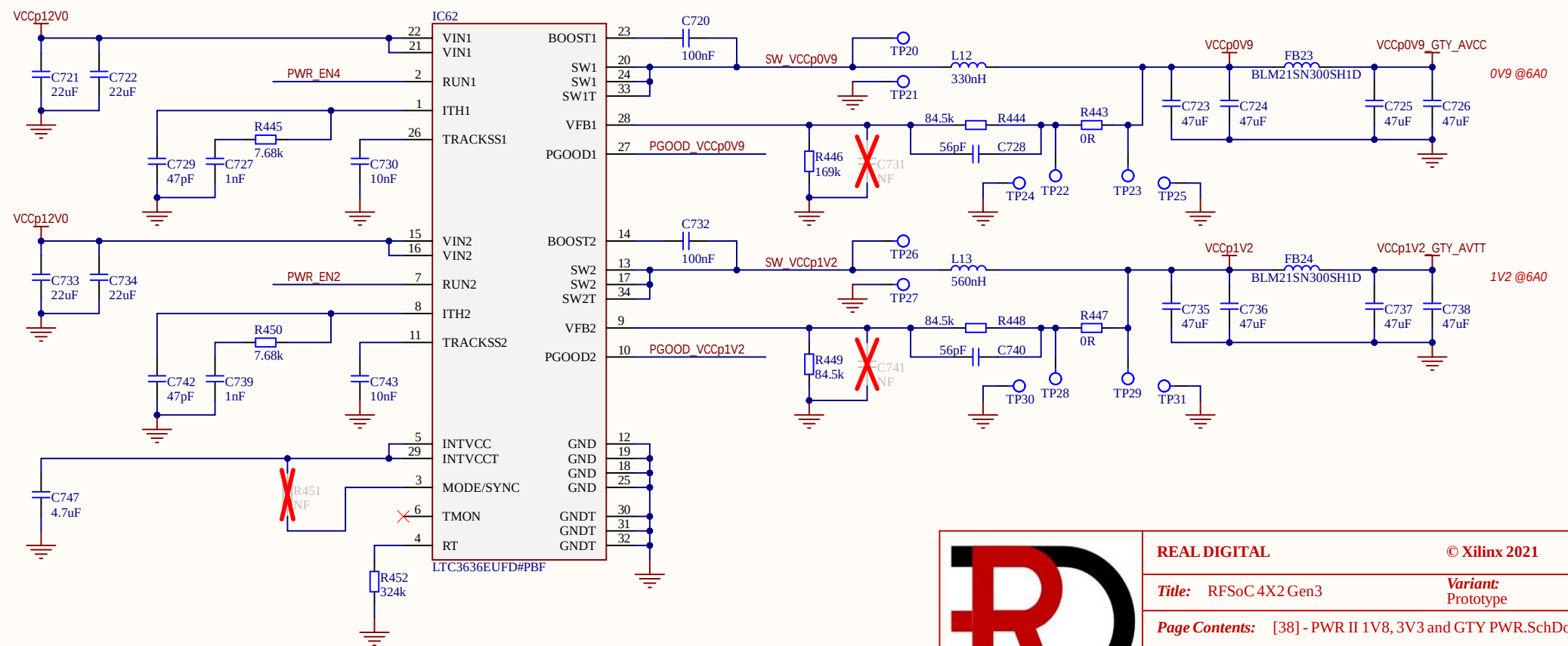
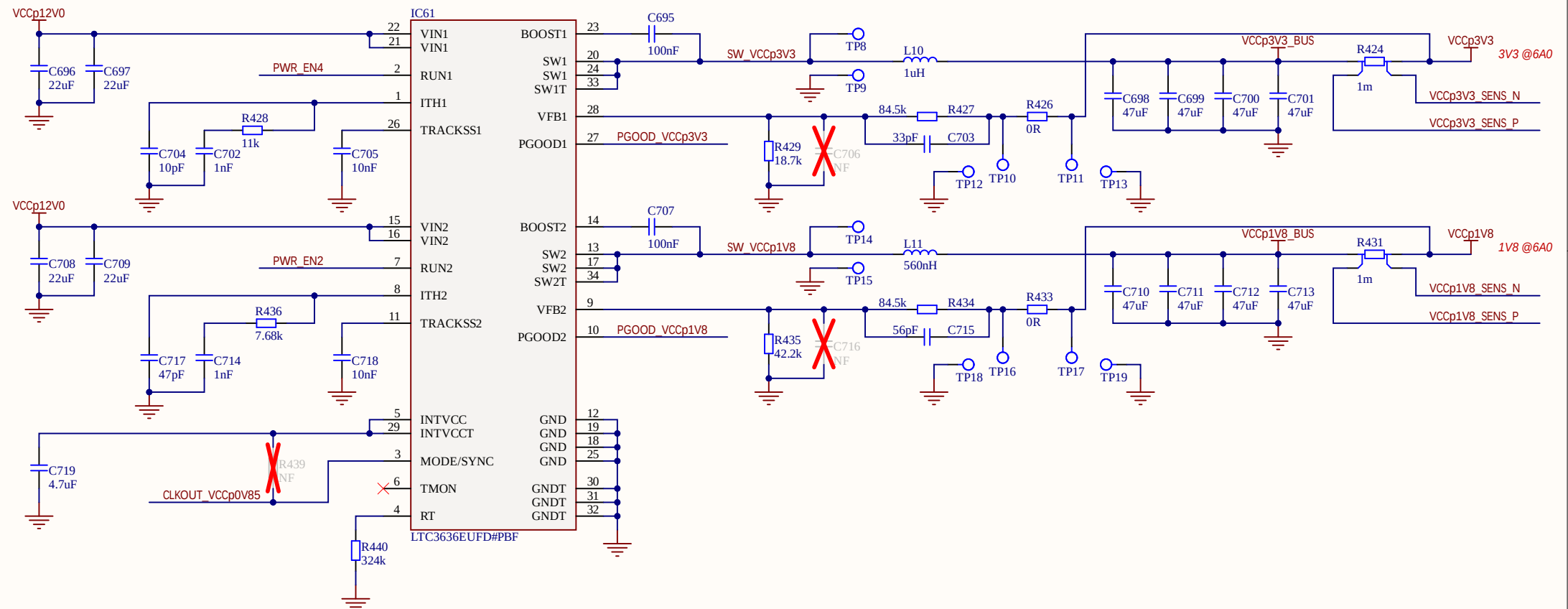
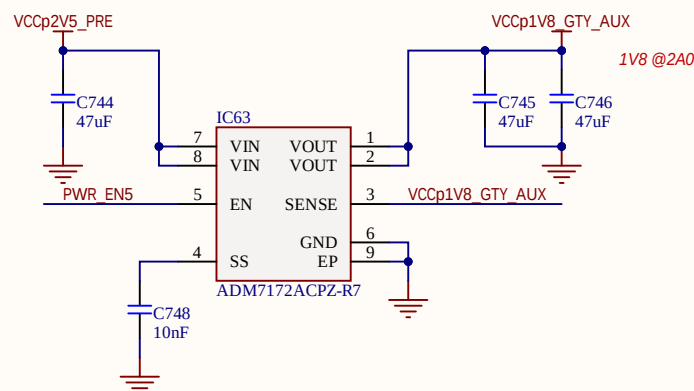
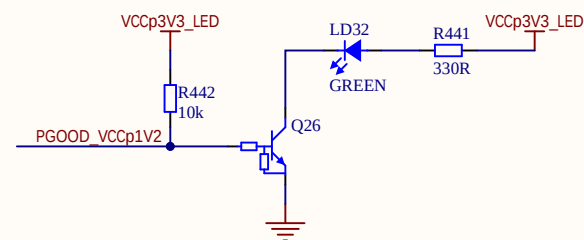
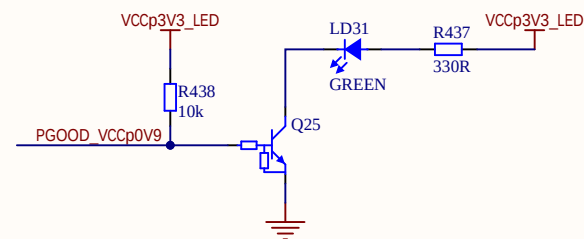
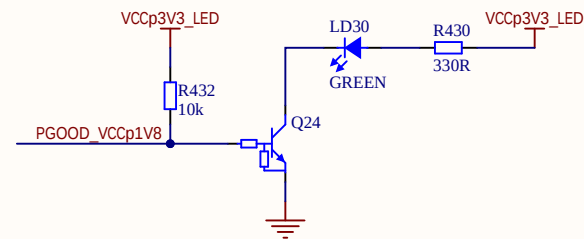
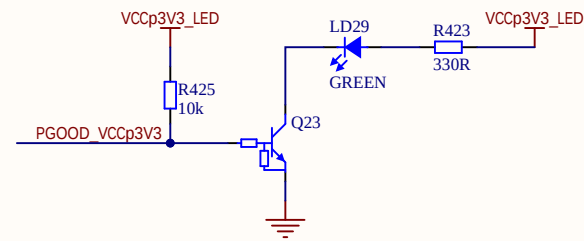
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Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [36] - PWR INPUT AND FAN CONTROLLER.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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POWER I: VCCp0V85



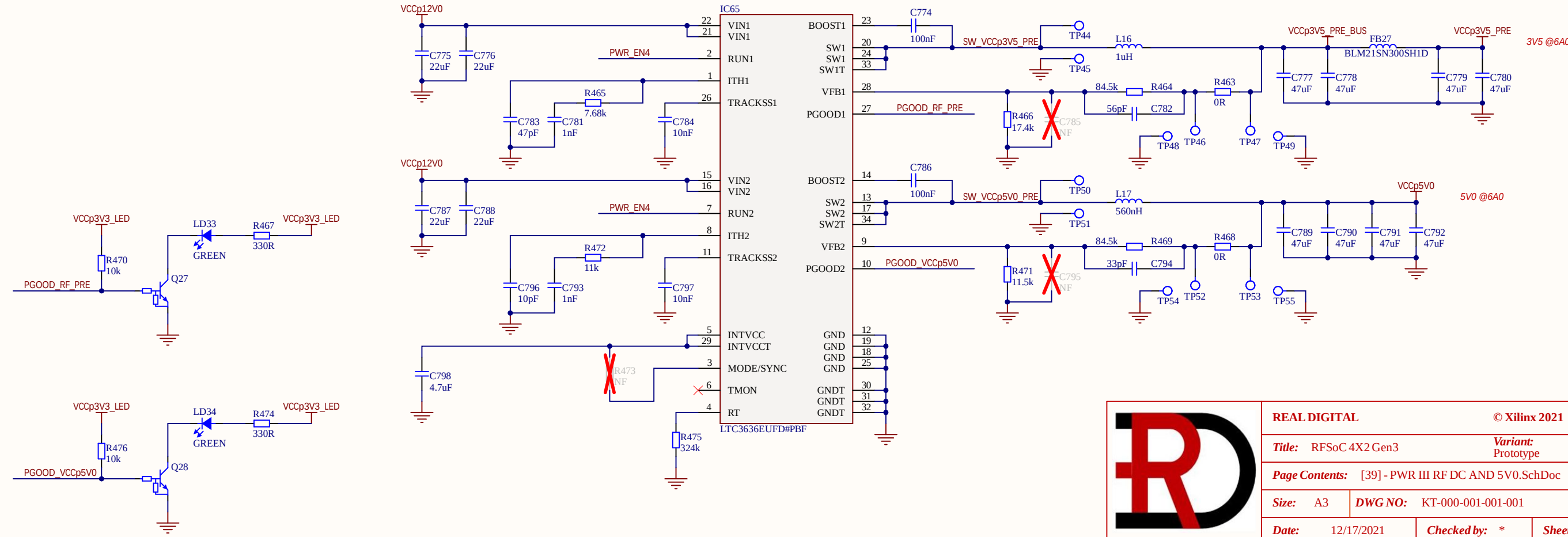
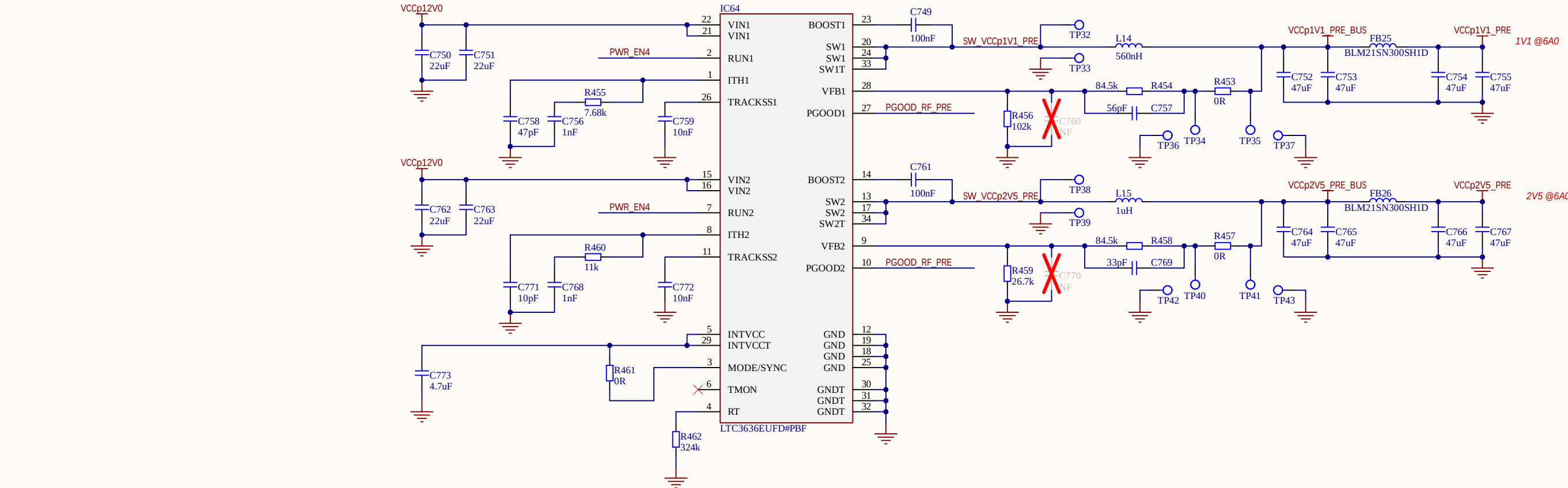
REAL DIGITAL		© Xilinx 2021	
Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [37] - PWR I 0V85.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
Date: 12/17/2021	Checked by: *	Sheet 37	of 46

POWER II: VCCp1V8, VCCp3V3 and GTY PWR



REAL DIGITAL		© Xilinx 2021	
Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [38] - PWR II 1V8, 3V3 and GTY PWR.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V211
Date: 12/17/2021	Checked by: *		Sheet 38 of 46

POWER III: RF DC/DC AND 5V0

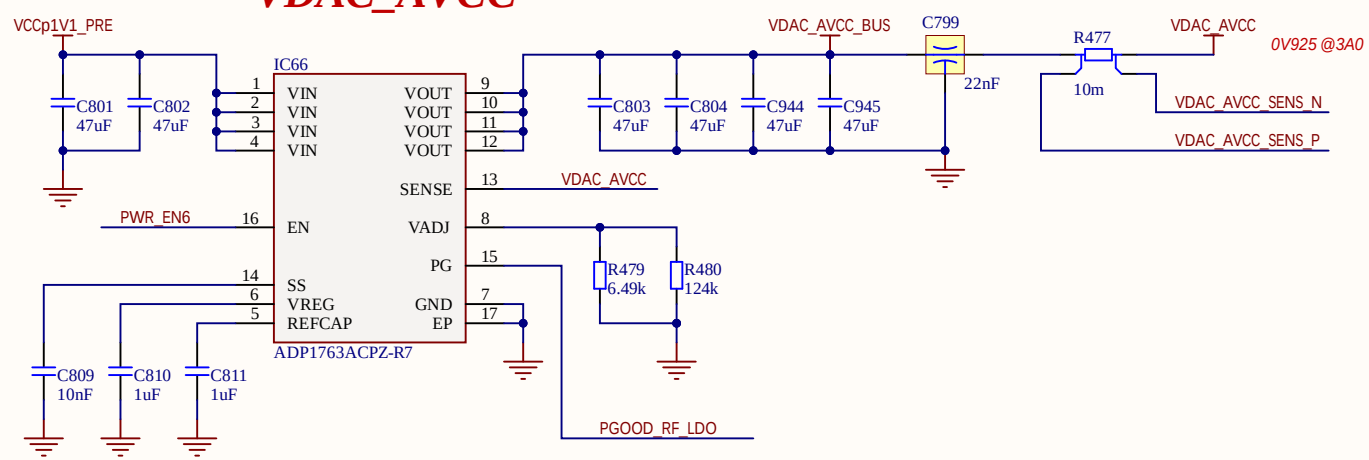




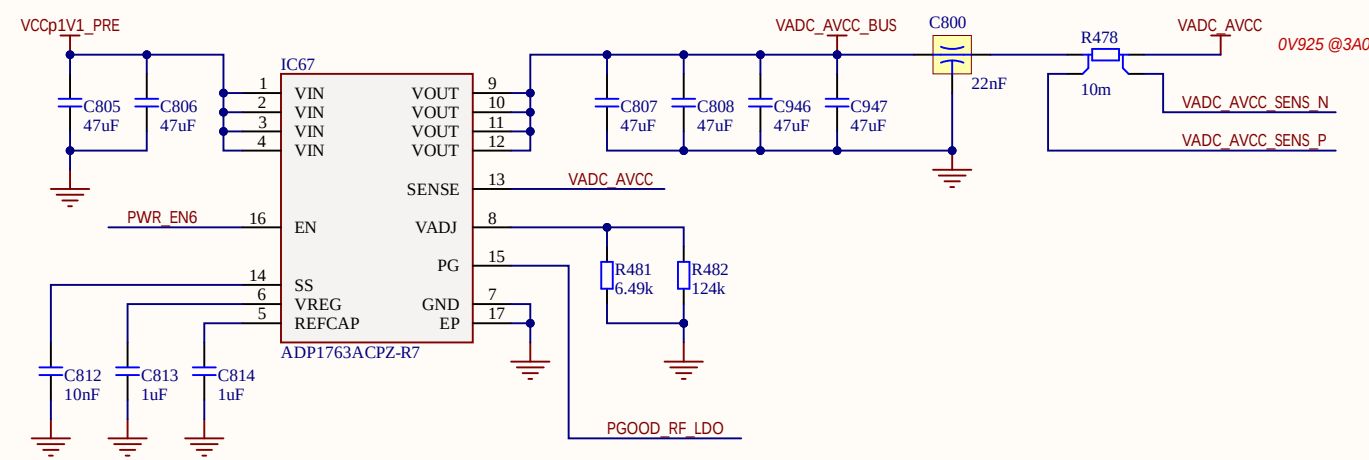
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Page Contents: [39] - PWR III RF DC AND 5V0.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001	Revision: V2I1	
Date: 12/17/2021	Checked by: *	Sheet 39 of 46	

POWER IV: RF LDO

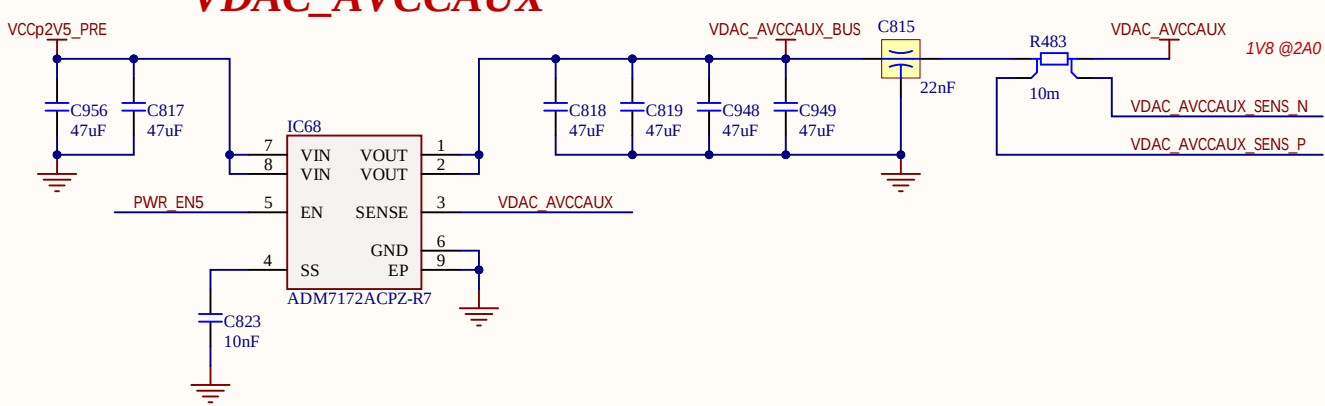
VDAC_AVCC



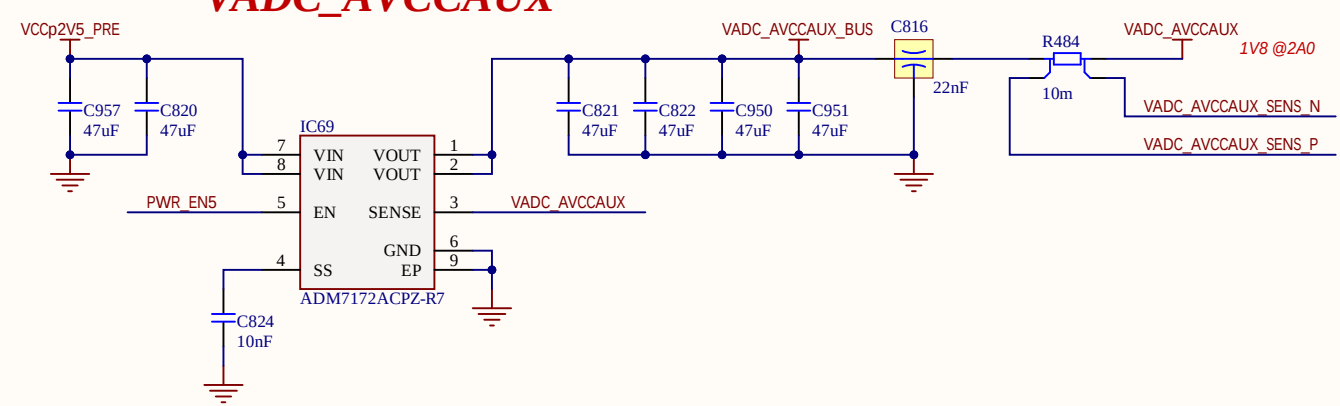
VADC_AVCC



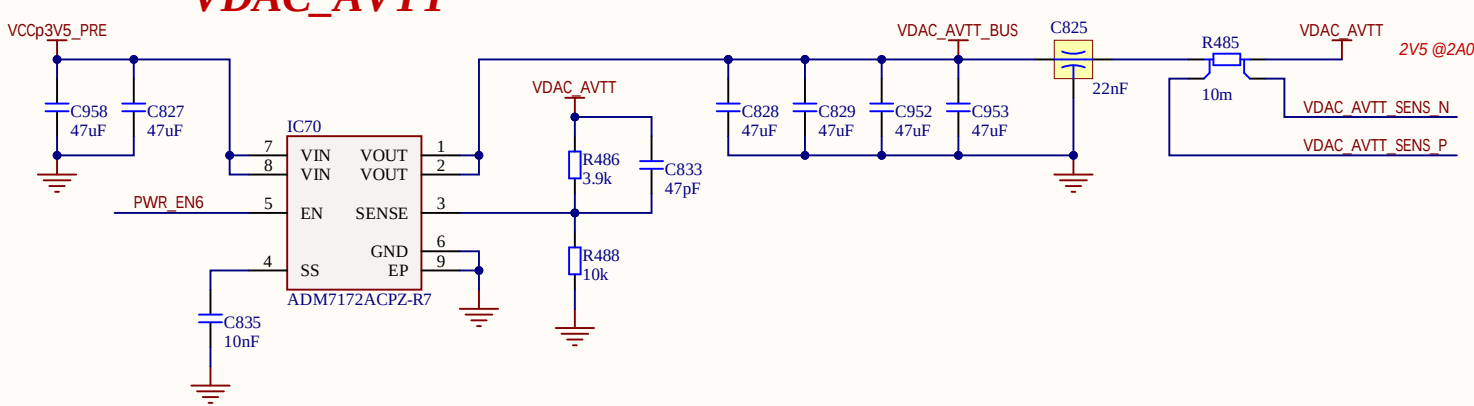
VDAC_AVCCAUX



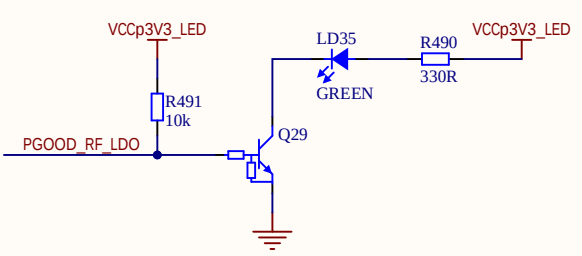
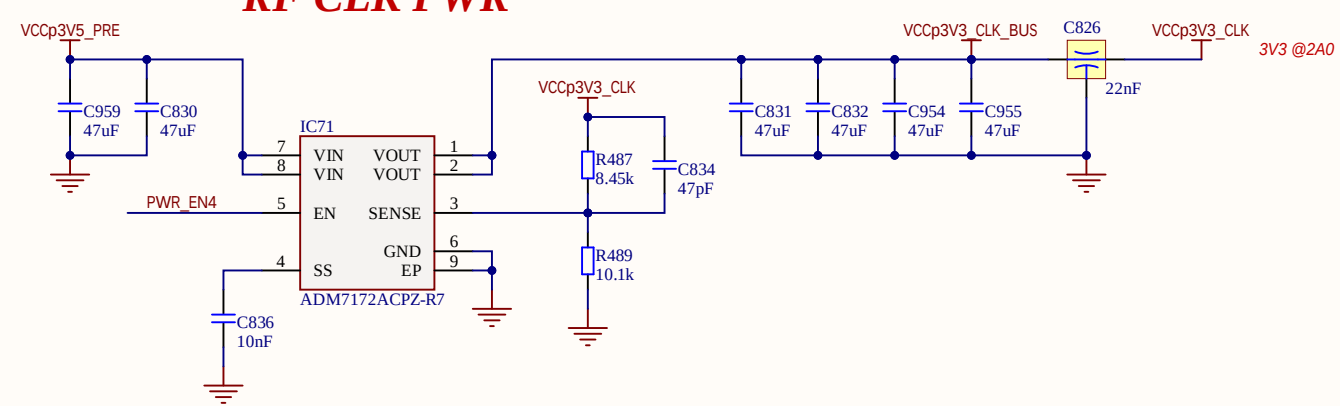
VADC_AVCCAUX



VDAC_AVTT

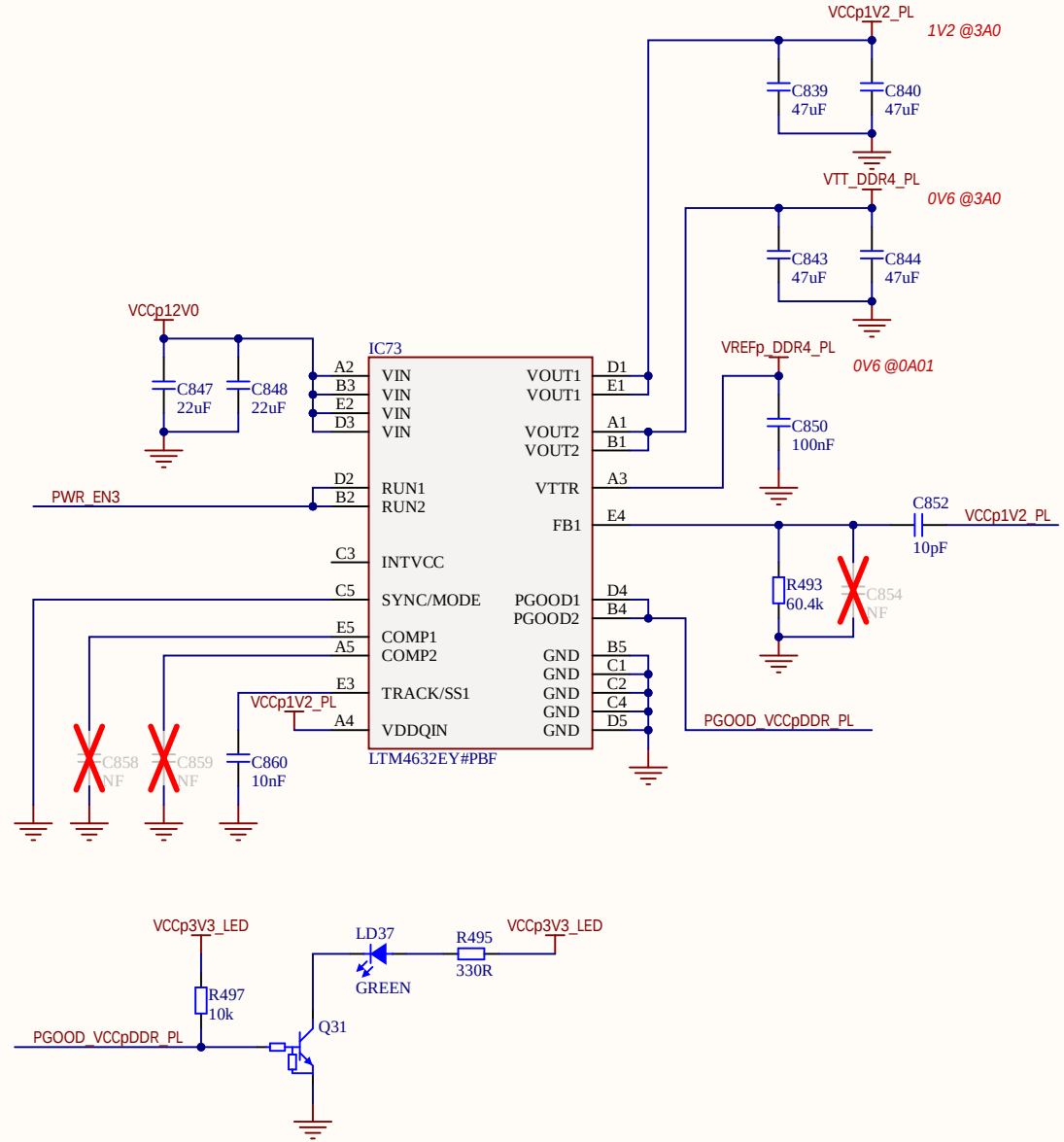
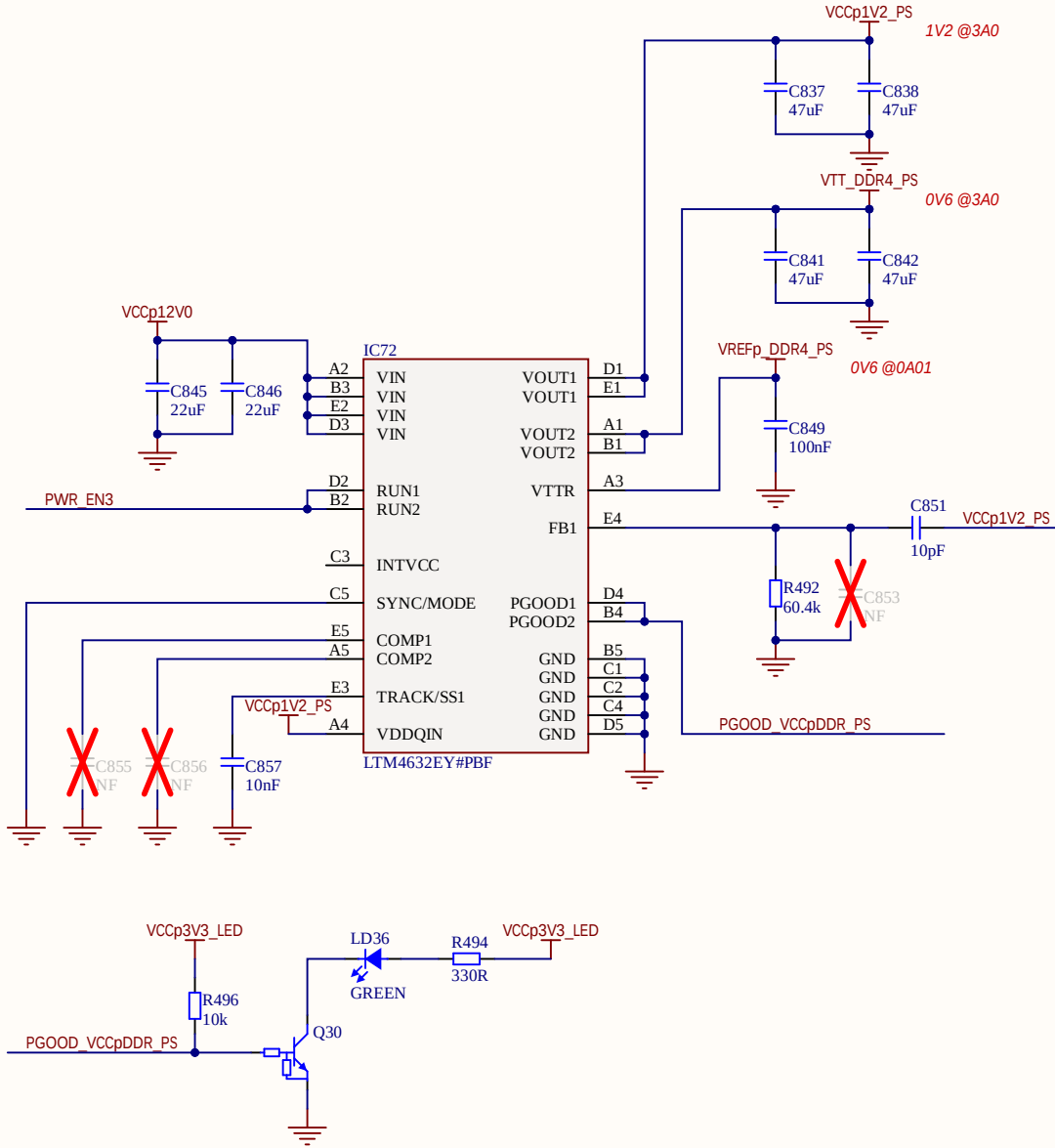


RF CLK PWR



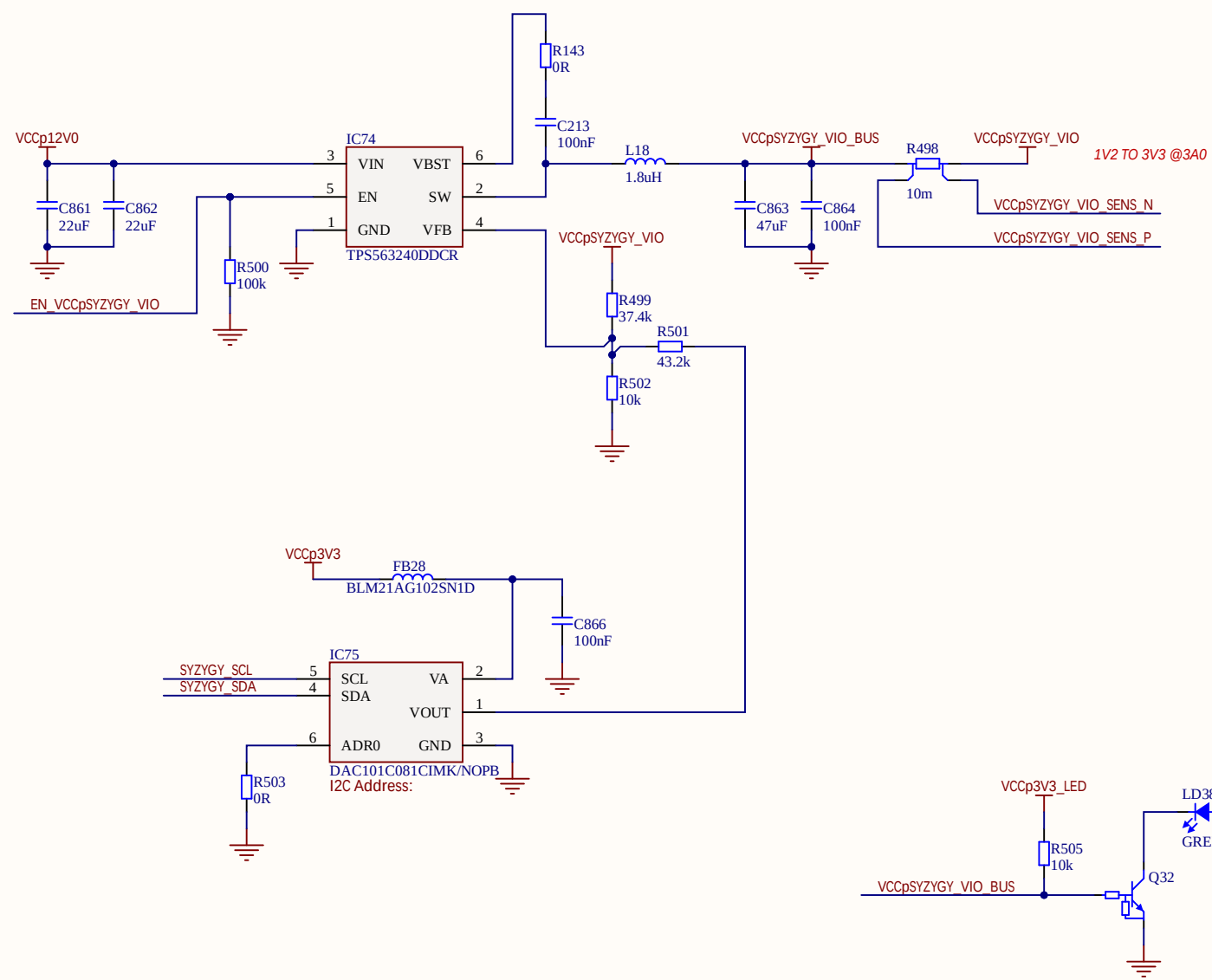
REAL DIGITAL		© Xilinx 2021	
Title: RFSoc 4X2 Gen3		Variant: Prototype	
Page Contents: [40] - PWR IV RF LDO.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
Date: 12/17/2021	Checked by: *		Sheet 40 of 46

POWER V: DDR4



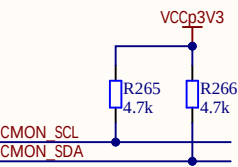
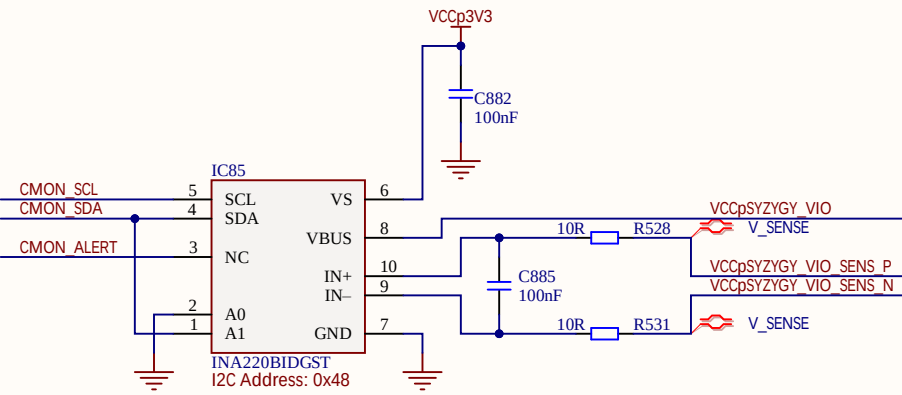
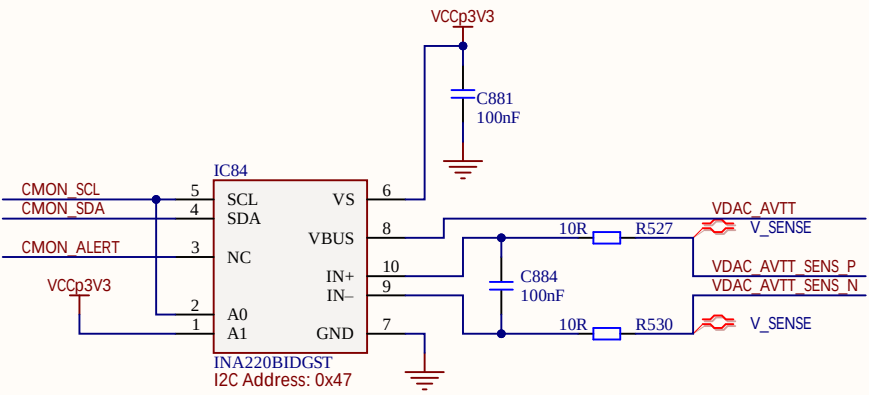
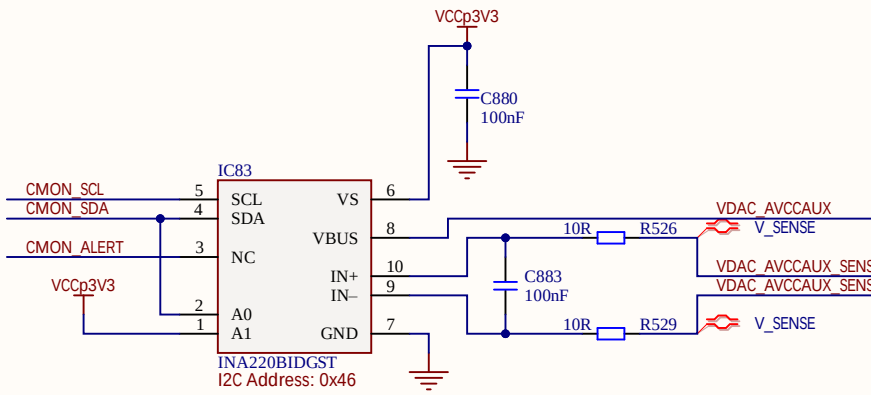
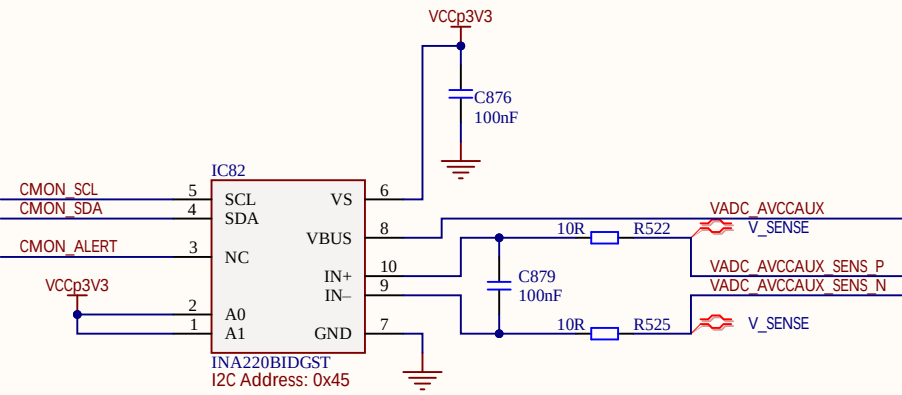
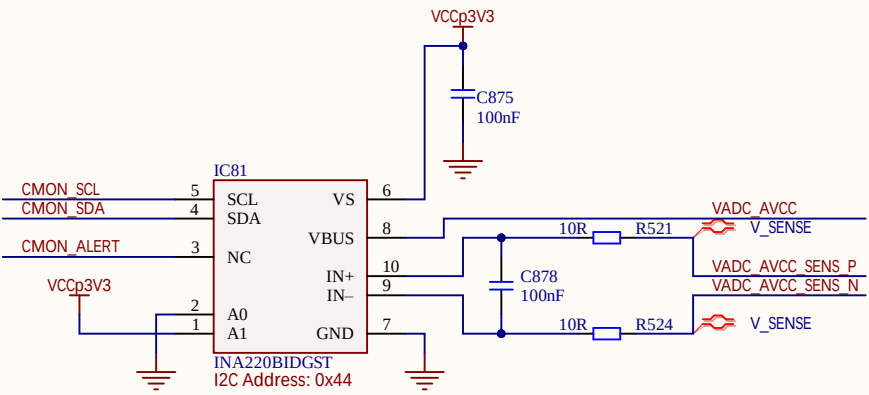
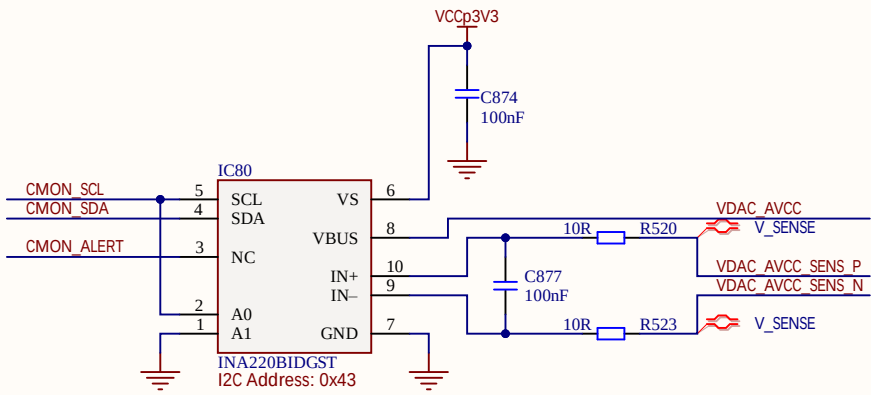
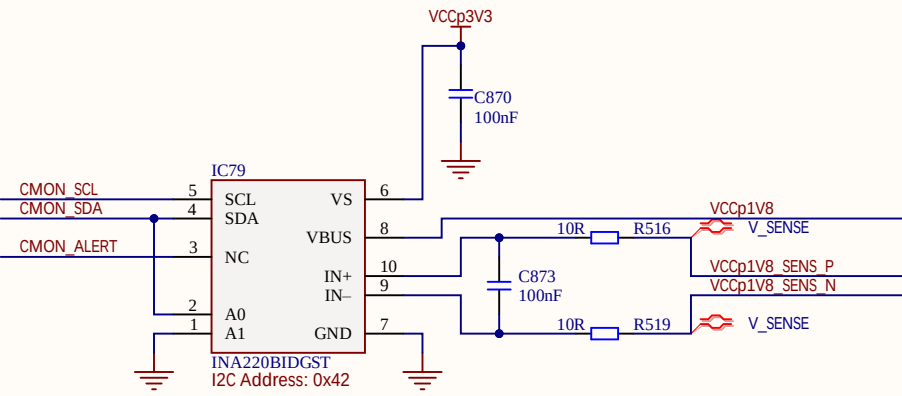
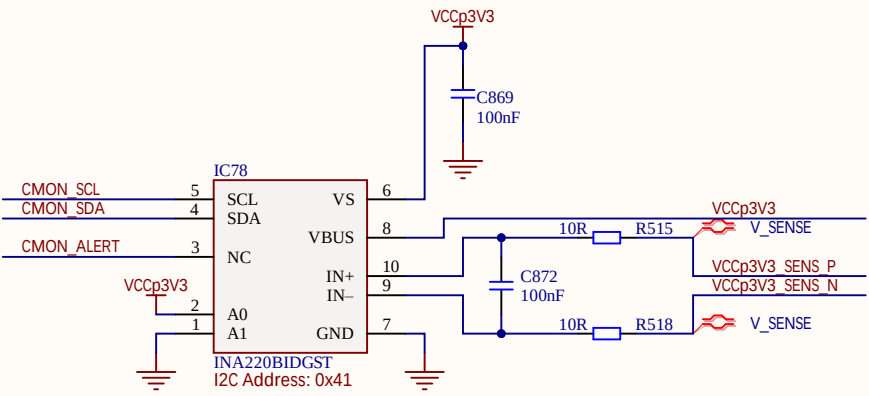
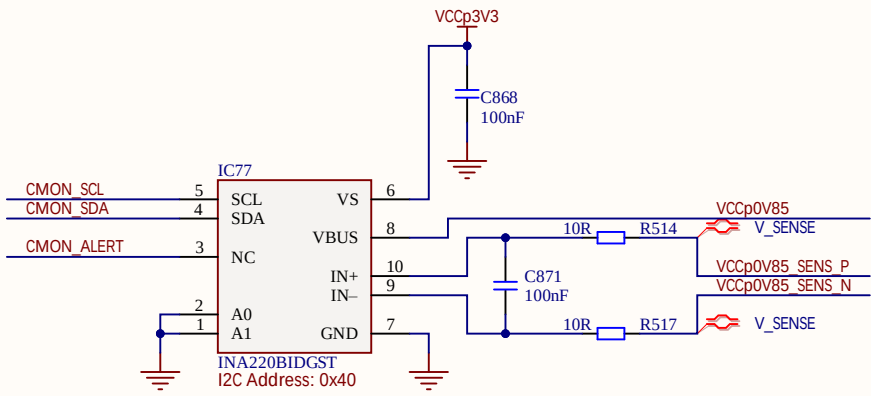
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Title: RFSoc4X2 Gen3		Variant: Prototype	
Page Contents: [41] - PWR V DDR4.SchDoc			
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POWER VI: SYZYGY



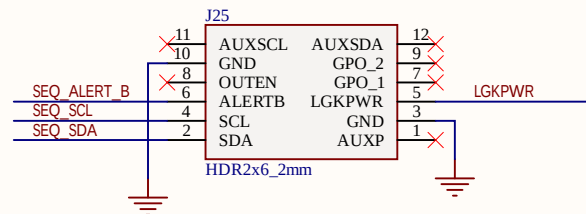
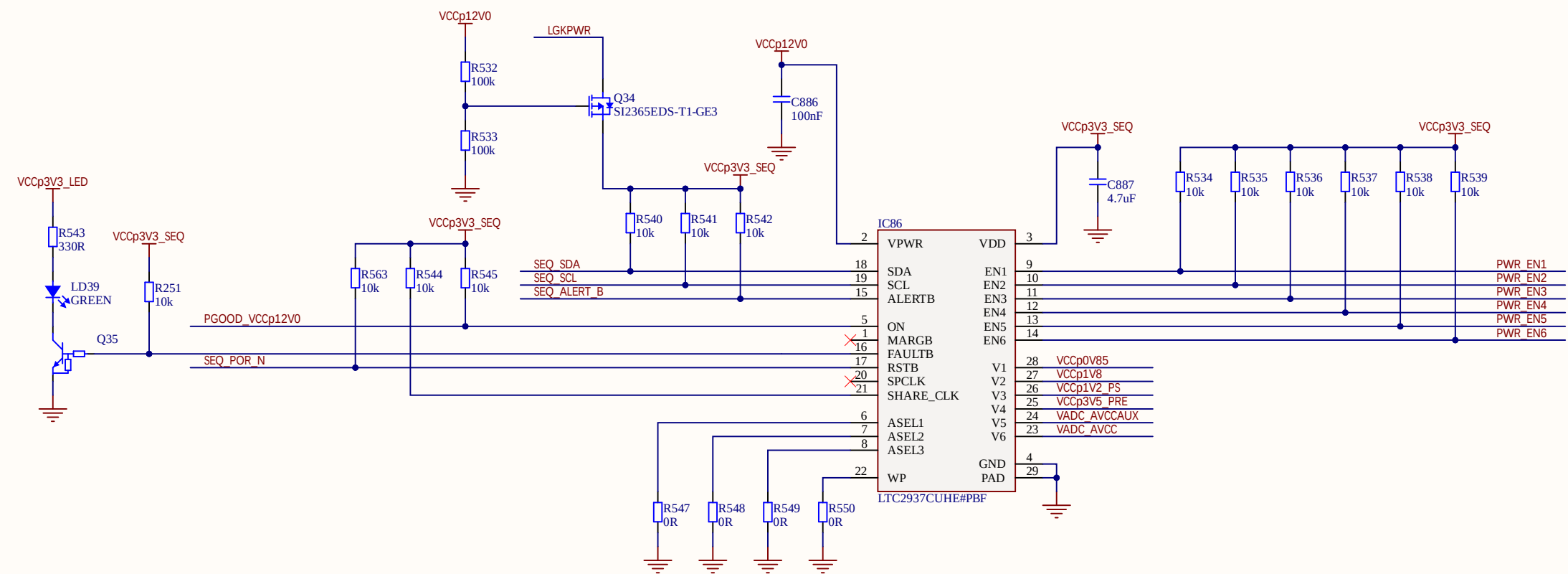
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	Title: RFSoc 4X2 Gen3		Variant: Prototype	
	Page Contents: [42] - PWR VII SYZYGY.SchDoc			
	Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
	Date: 12/17/2021	Checked by: *		Sheet 42 of 46

CURRENT MONITOR



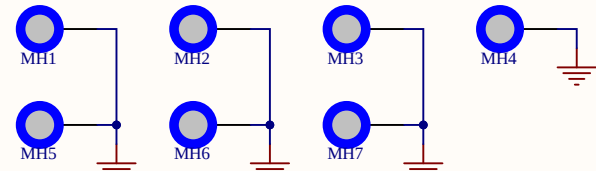
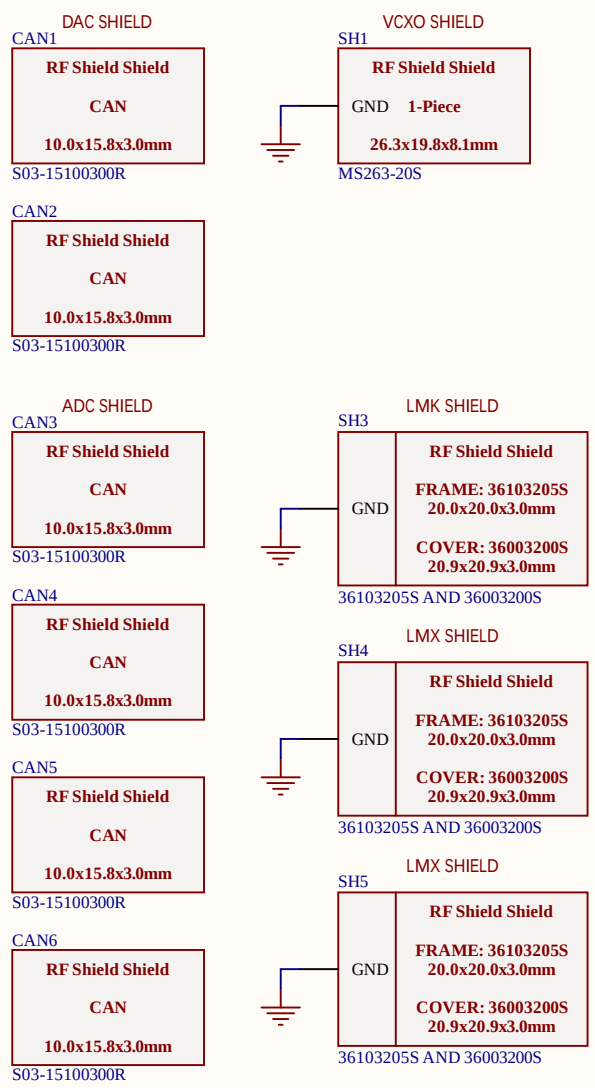
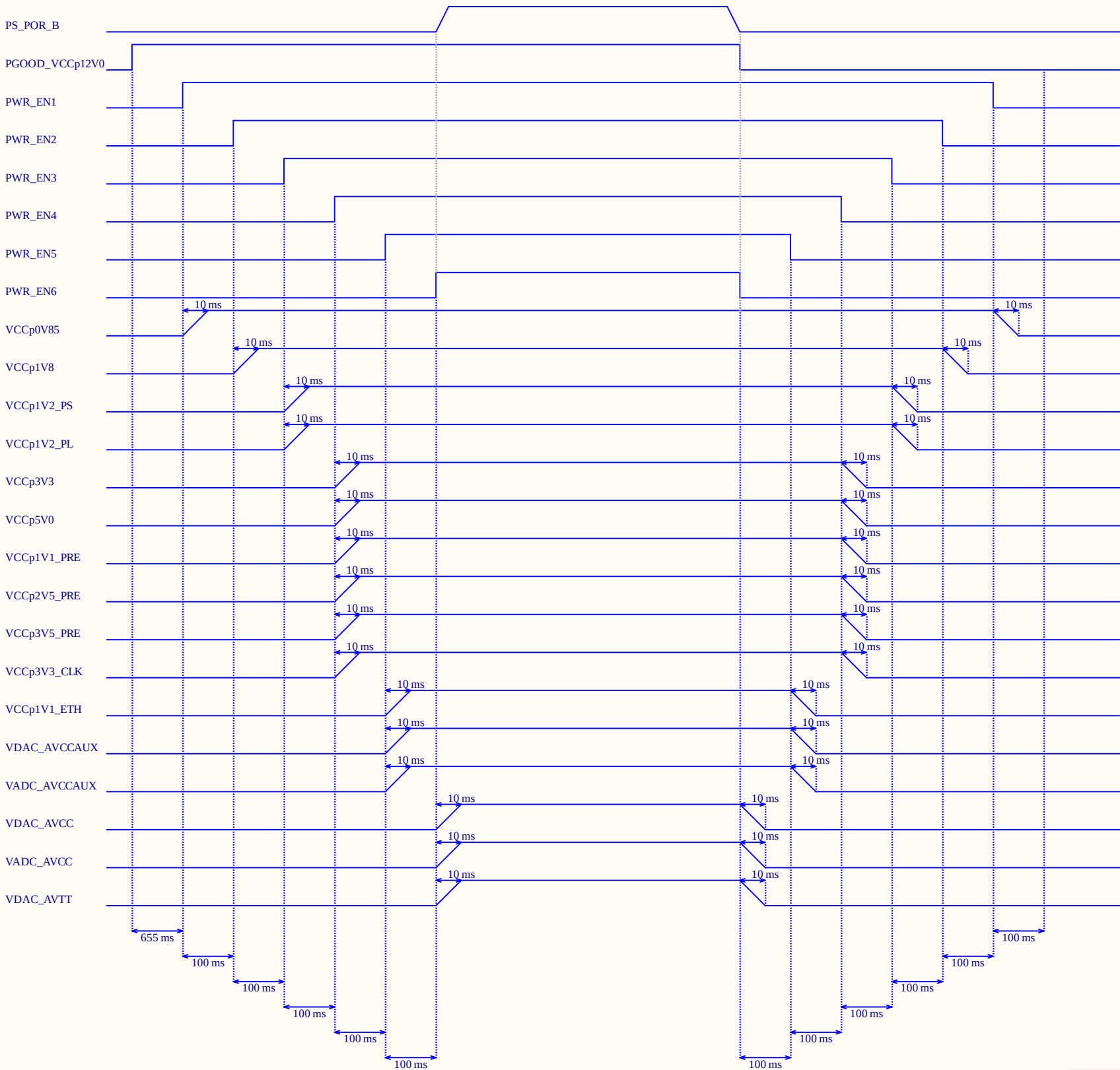
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	Title: RFSoc 4X2 Gen3		Variant: Prototype	
	Page Contents: [43] - CURRENT MONITOR.SchDoc			
	Size: A3	DWG NO: KT-000-001-001-001		Revision: V2I1
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SEQUENCER



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MECHANICAL AND POWER SEQUENCING



SC5	SC6	SC7	SC8	SC9	SC10	SC11
Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm	Screw, Phillips, M3, 6mm
M3, 6mm	M3, 6mm	M3, 6mm	M3, 6mm	M3, 6mm	M3, 6mm	M3, 6mm
STDF5	STDF6	STDF7	STDF8	STDF9	STDF10	STDF11
Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm	Standoff, M3, L:5.0mm
970050351	970050351	970050351	970050351	970050351	970050351	970050351

Real Digital
LG1
AMD Xilinx
LG2
PYNQ
LG3



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DOC: REVISION HISTORY

Schematic:

1. Update Title Block: “CONFIDENTIAL Do not distribute” and “CR 2021 REAL DIGITAL” from all schematic pages
2. Update Cover Page (Sheet 1)
3. Update Block Diagram (Sheet 2)
4. Update Power Diagram (Sheet 3)
5. Remove design notes (Sheet 4, Sheet 18, and Sheet 28)
6. Update POWER SEQUENCING diagram (Sheet 45)

Schematic and PCB

1. Swap MIO33_UA1_RXD and MIO32_UA1_TXD (Sheet 20)
2. Change Sheet 12 name from “SD CARD” to “SD CARD AND EEPROM”. Add the EEPROM memory AT24MAC402-MAHM-T connected to the Syzygy I2C bus.
3. Change the status for the resistors connected to SPI_CLK/SMCLK (38) and SPI_DO/SMDAT (39) to “No Load” (Sheet 9, USB5742/2G).
4. Change the status for the capacitors connected to VCM01_224 (AL5), VCM23_224 (AL4), VCM01_226 (AJ5), and VCM23_226 (AJ4) to “NoLoad” (Sheet 27).
5. Rename the net between the power supply sequencer IC86.17 and the OLED display DISP1.8 to be SEQ_POR_N and add a pull-up resistor (10k) to Vccp3v3_SEQ on SEQ_POR_N (Sheet 44).
6. Connect SEQ_POR_N to NVT2008BQ level shifter pin B6 and connect PS_POR_N to NVT2008BQ level shifter pin A6 (Sheet 14).
7. Change the status for the pull-up resistor connected to PS_POR_N to “Load” (Sheet 19).
8. Change DDR4 memory part number from "MT40A512M16JY-083E" to "MT40A512M16LY-062E".
10. Add the AC decoupling capacitors for the RF clocks.
11. Remove the 3dB attenuator for the external input reference clock.
12. Increase the output capacitance for the LDOs (Sheet 40).
13. Silkscreen changes:
 - Remove the QR Code;
 - Change the Xilinx logo to be AMD_Xilinx;
 - Add PYNQ logo;
 - Change "USD DEVICE" to "USB DEVICE";
 - Add labels for the programming headers: JTAG, SI5395 PROG, SEQ PROG, CLK PROG
 - Change DAC0, DAC1, ADC0, ADC1, etc. to DAC_A, DAC_B, ADC_A, ADC_B, etc.
14. Add 200k pull-up resistors connected for the NVT2008BQ "EN" pin, update "VREFB" connection, and add pull-ups on the B side of the level translators. (Sheet 05 - 3 ICs, Sheet 10 - 1 IC, Sheet 14 - 1 IC)
15. Increase the input capacitance for the ADM7172ACPZ-R7 LDOs (Sheet 40).
16. Update the USB3.0 Slave connector schematic symbol and footprint (Sheet 8).
17. Increased the value of the resistors to reduce the brightness of the white and RGB user LEDs
 - Change R2, R3, R4, and R5 resistors values from 330R to 1k
 - Change R16, R20, R24, and R26 resistors values from 86R6 to 270R
 - Change R16, R20, R24, and R26 resistors values from 150R to 470R

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