RFSoC 4X2 Gen3

Variant: Prototype

12/17/2021
V2I1

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Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
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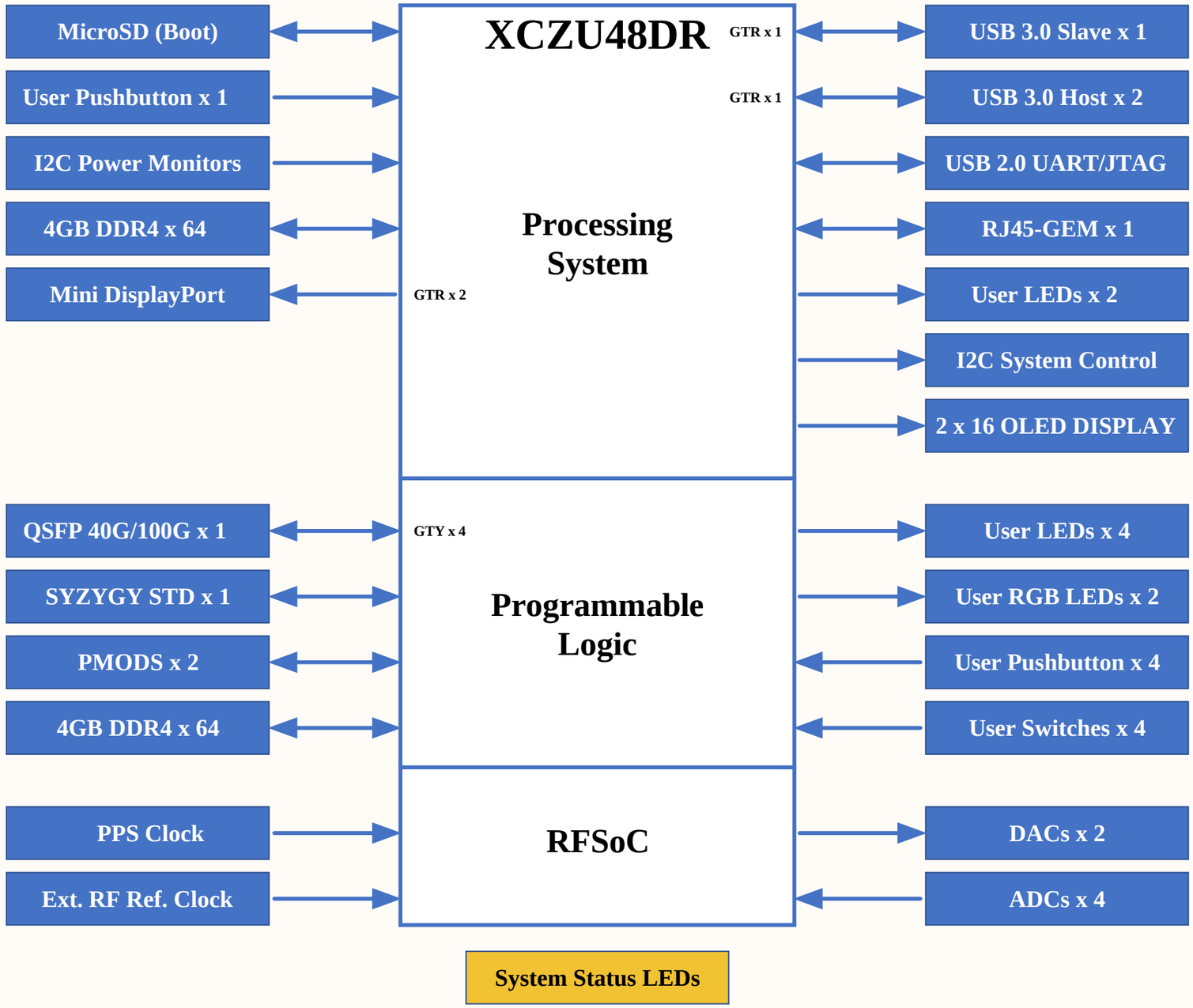
RFSoC 4X2 Gen3

(Block Diagram)



REAL DIGITAL			
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [02] - BLOCK DIAGRAM.SchDoc			
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RFSoC 4X2 Gen3

(Power Diagram)

PWR JACK 2x5.5mm → EMI FILTER → LM5069 Input Protection 12V0 @8A0

- 3V3 @3A0 TPS563240 → PWR GOOD LEDs
- EN1 0V85 @20A0 LTC7150S → VCCINT, VCCINT_IO, VCCBRAM, VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR, VPS_MGTRAVCC, VCCINT_AMS, VCCSDFEC
- EN1 0V85 @20A0 LTC7150S → VCCINT
- EN2 1V8 @6A0 / EN4 3V3 @6A0 LTC3636 → VCCAUX, VCCAUX_IO, I/O, I/O
- EN3 1V2 @3A0 / 0V6 @3A0 / 0V6 @0A01 LTM4632 → VCC_PSPLL, DDR4 VCC, DDR4 VTT, DDR4 VREF
- EN4 0V9 @6A0 / EN2 1V2 @6A0 LTC3636 → VMGTAVCC, VMGTAVTT
- EN3 1V2 @3A0 / 0V6 @3A0 / 0V6 @0A01 LTM4632 → VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VPS_MGTRAVTT, I/O
- EN3 1V2 @3A0 / 0V6 @3A0 / 0V6 @0A01 LTM4632 → DDR4 VCC, DDR4 VTT, DDR4 VREF
- EN4 1V1 @6A0 / EN4 2V5 @6A0 LTC3636 → DDR4 MEM ICs
- EN4 3V5 @6A0 / EN4 5V0 @6A0 LTC3636 → USB, 1V2 TO 3V3 @3A0 TPS563240 → SYZYGY
- EN6 0V925 @3A0 ADP1763 → VDAC AVCC
- EN6 0V925 @3A0 ADP1763 → VADC AVCC
- EN5 1V8 @2A0 ADM7172 → VDAC AVCCAUX
- EN5 1V8 @2A0 ADM7172 → VADC AVCCAUX
- EN5 1V8 @2A0 ADM7172 → VMGTVCCAUX
- 1V0 @2A0 TPSM82822SILR → ETHERNET
- EN6 2V5 @2A0 ADP7172 → VDAC AVTT
- EN4 3V3 @2A0 ADM7172 → CLK ICs

Legend

- IC
- Programmable Logic
- Connector
- Processor System
- MISC
- RF-ADC, RF-DAC, SD-FEC

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Page Contents: [03] - POWER DIAGRAM.SchDoc	
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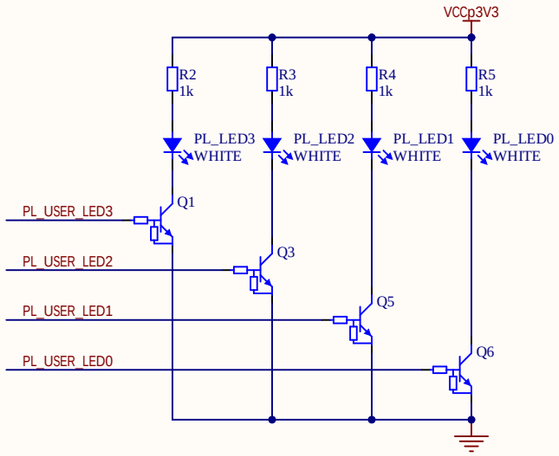
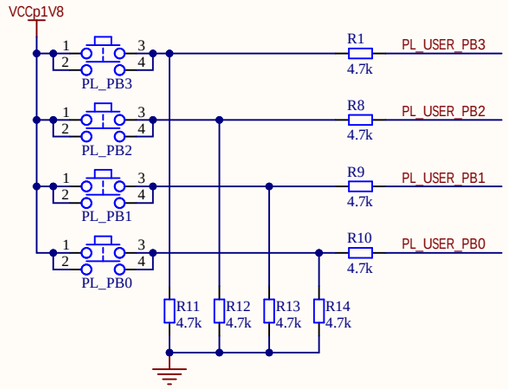
USER IO, LEDs

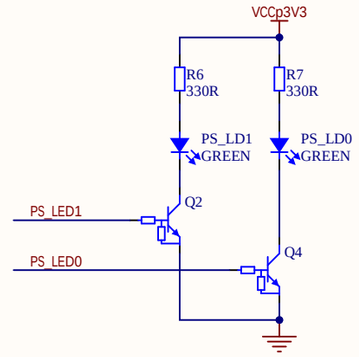
PL user-defined white LEDs



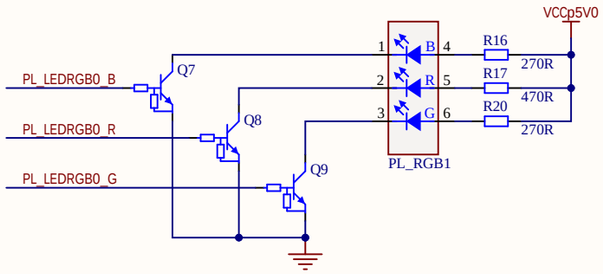
PL user-defined pushbuttons

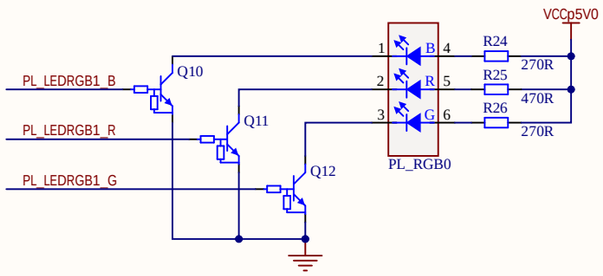


PS user-defined green LEDs

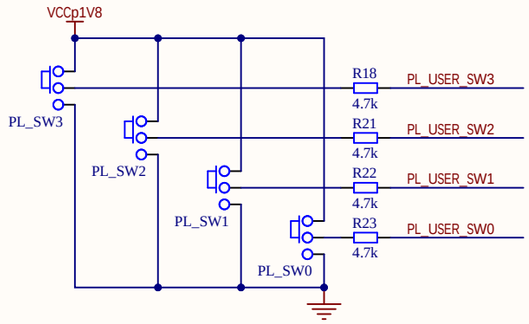


PL user-defined RGB LEDs

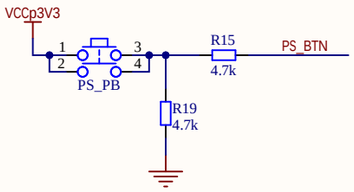




PL user-defined switches



PS user-defined pushbutton



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Title: RFSoC 4X2 Gen3		***Variant:*** Prototype
Page Contents: [04] - USER IO, LEDs.SchDoc		
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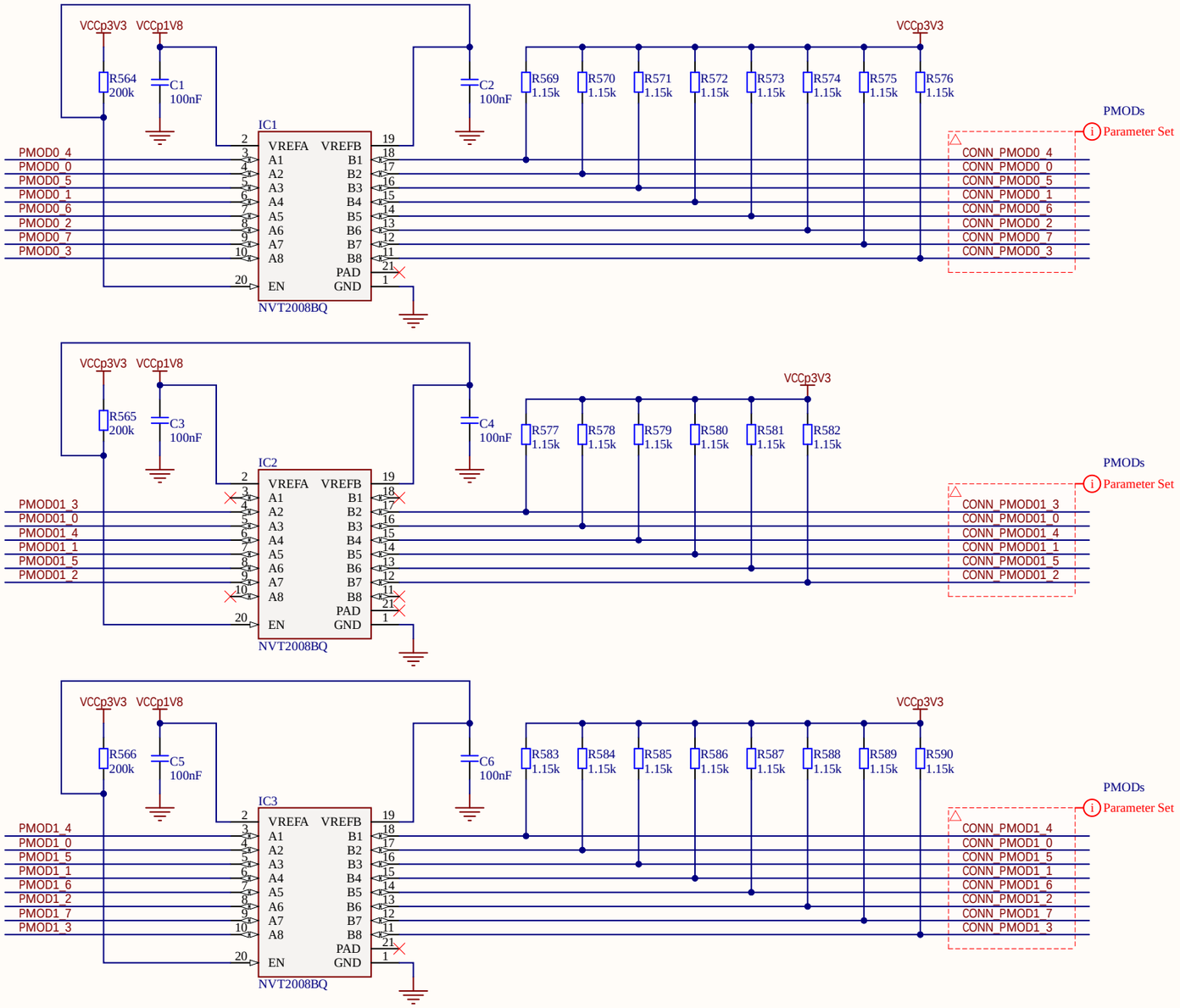
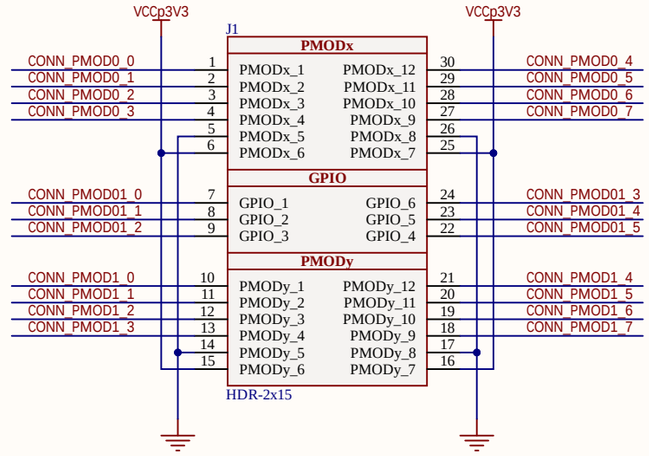
PMOD HEADERS





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Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [05] - PMOD HEADERS.SchDoc			
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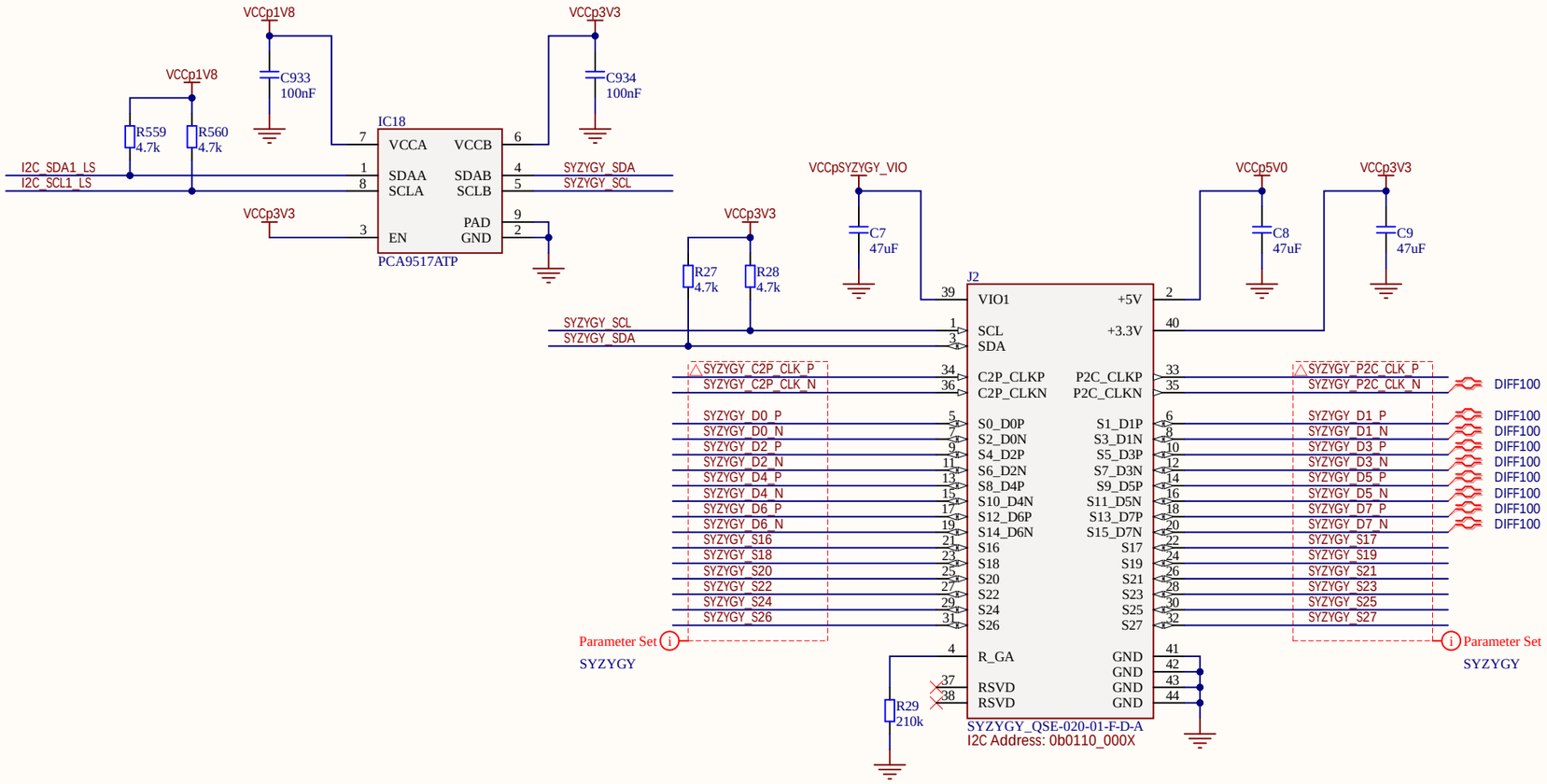
SYZYGY HEADER



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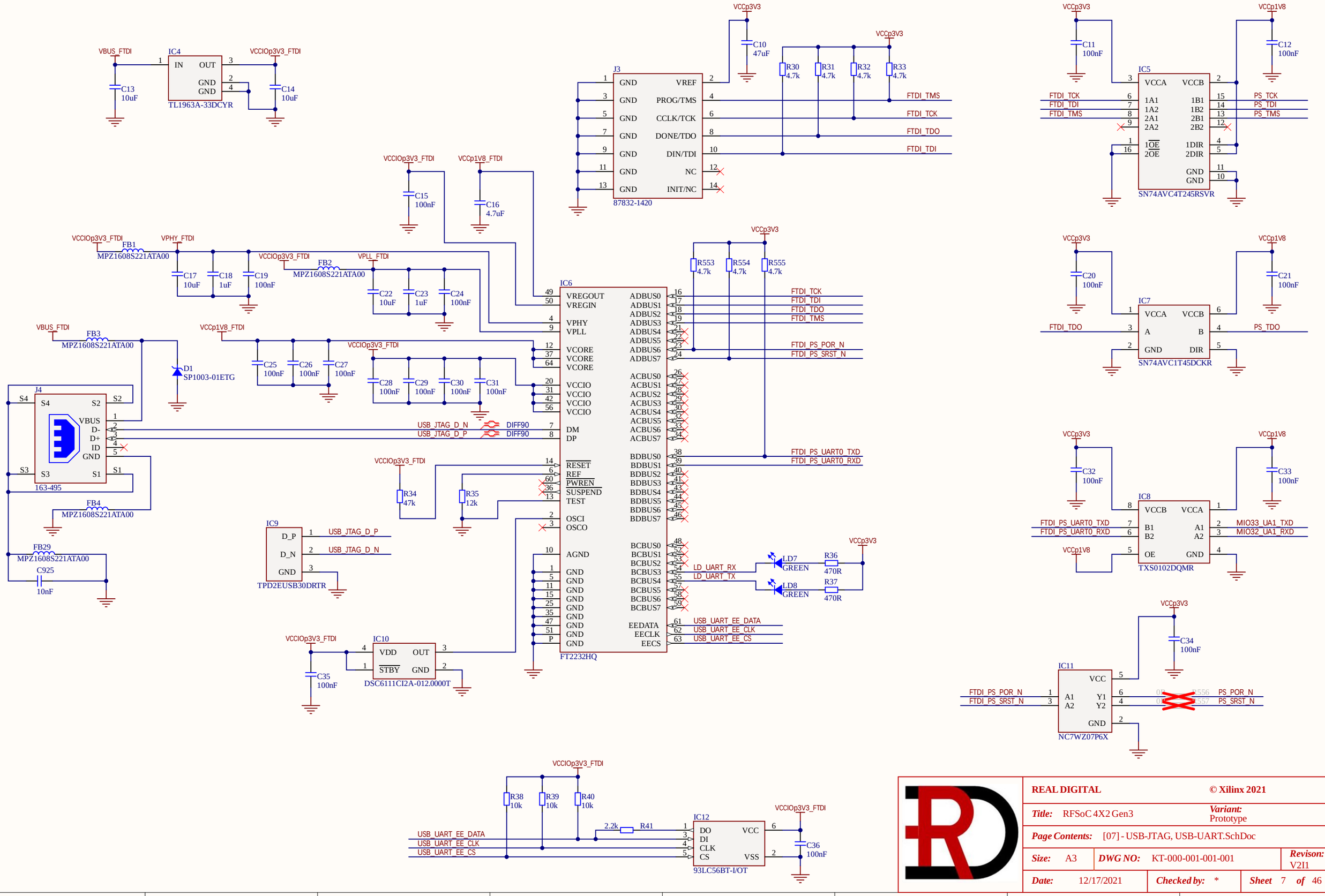
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [06] - SYZYGY HEADER.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 6 ***of*** 46	

USB-JTAG, USB-UART



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Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [07] - USB-JTAG, USB-UART.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
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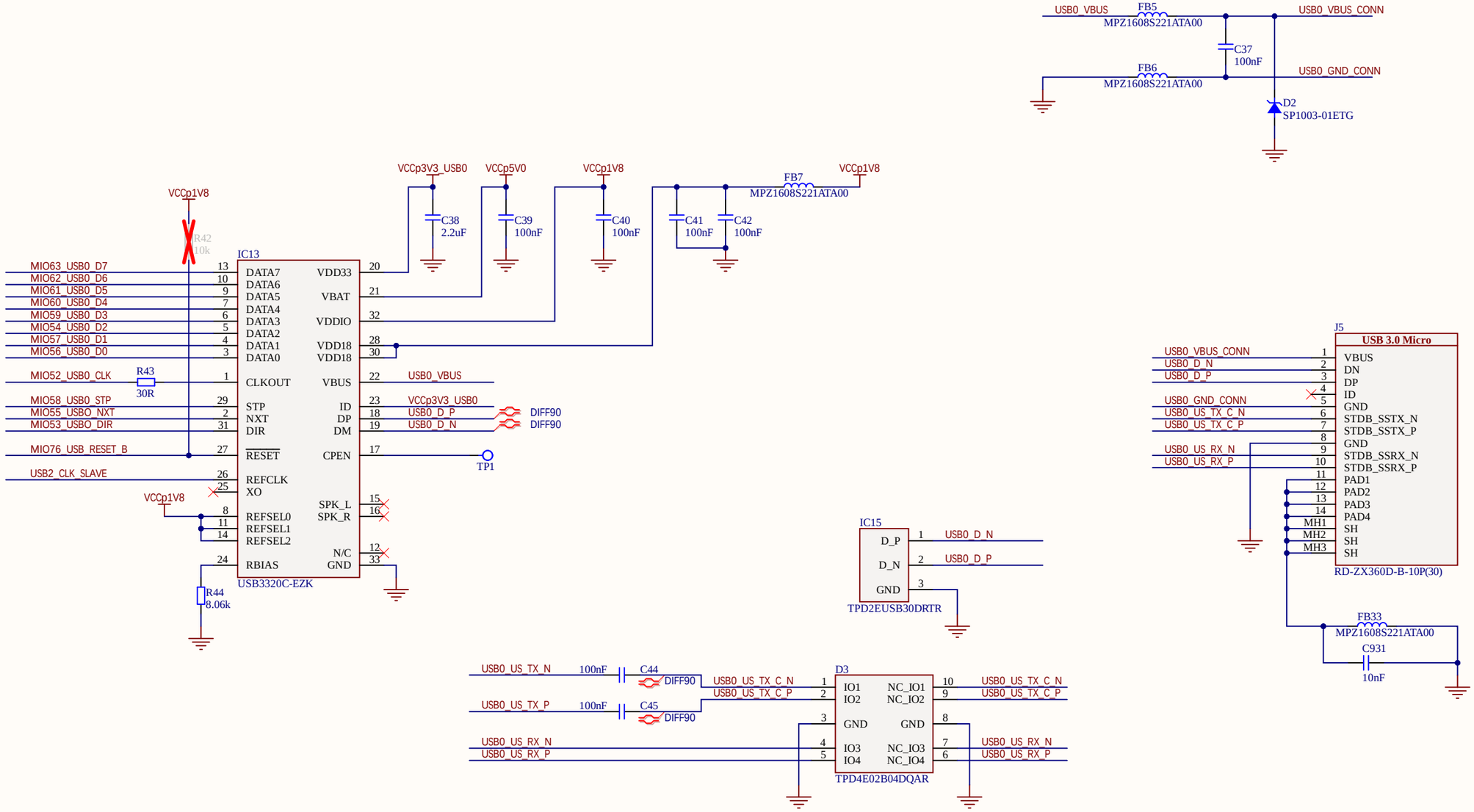
USB 3.0 SLAVE



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Page Contents: [08] - USB 3.0 SLAVE.SchDoc			
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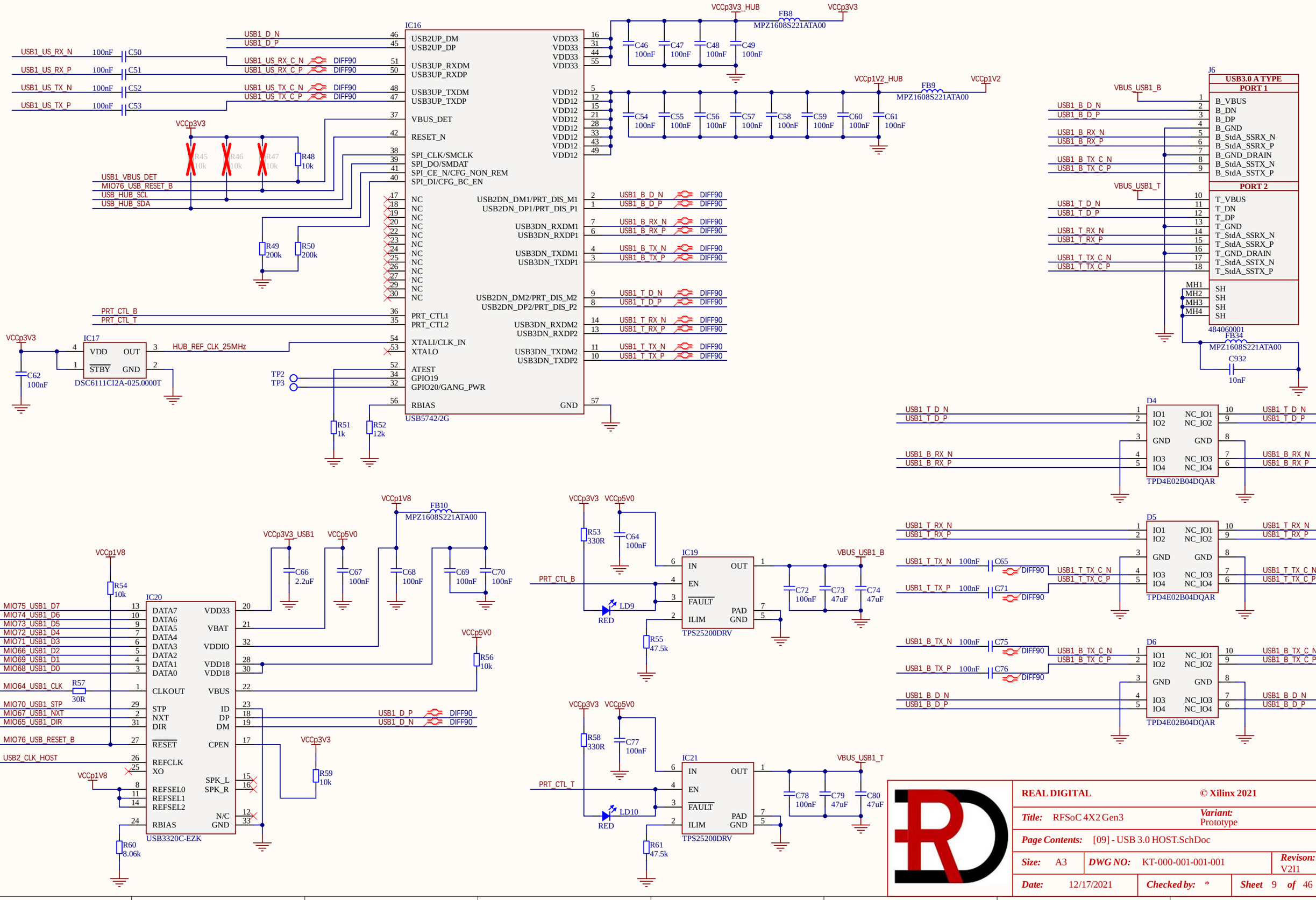
USB 3.0 HOST



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Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
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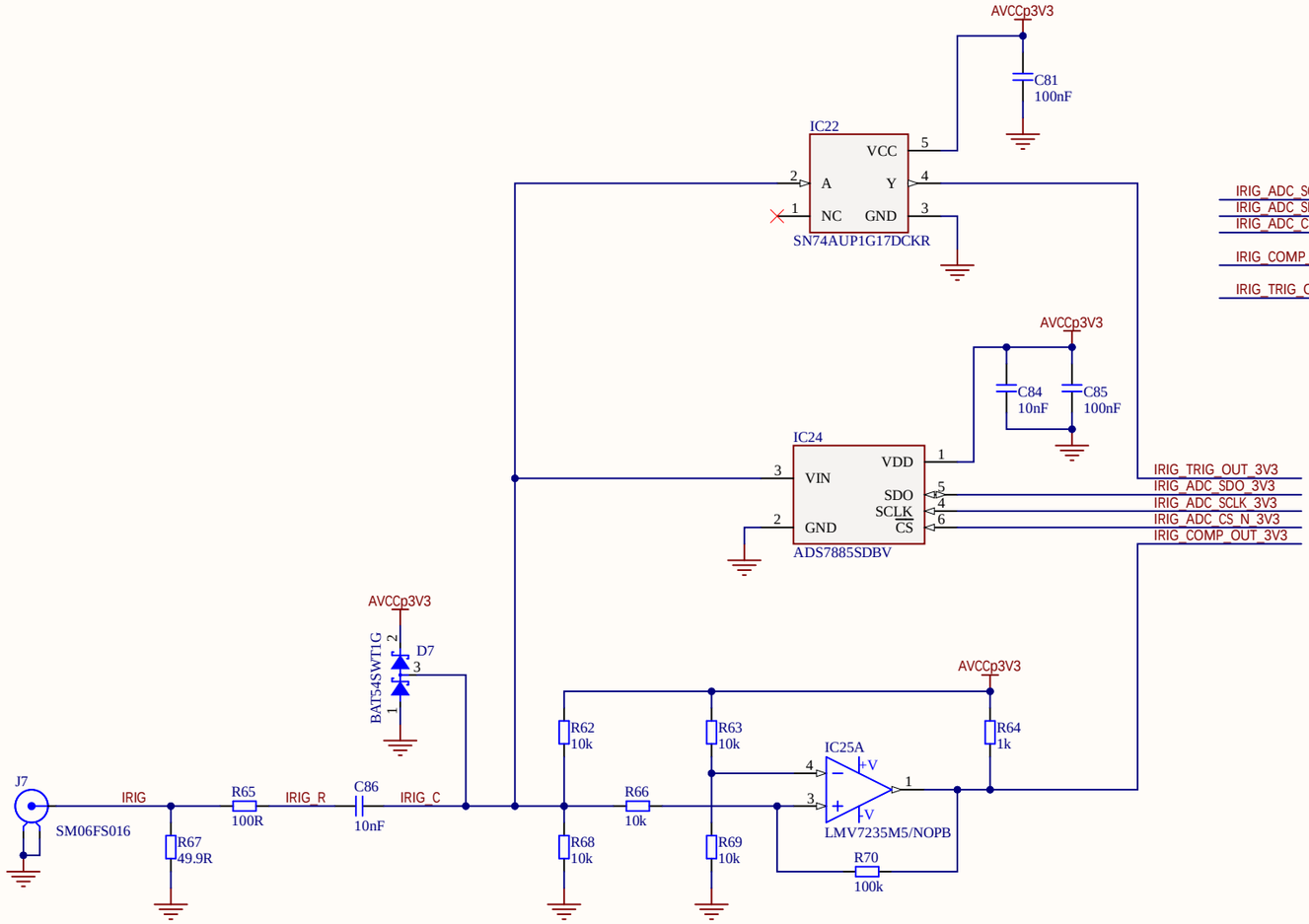
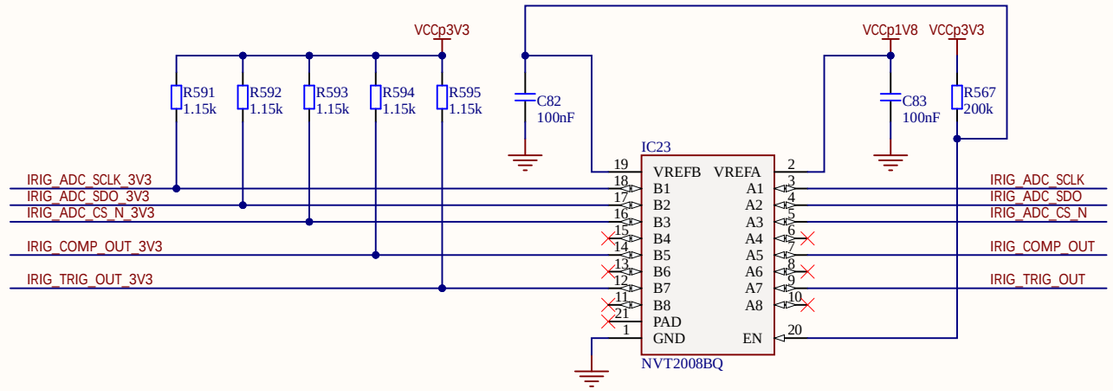
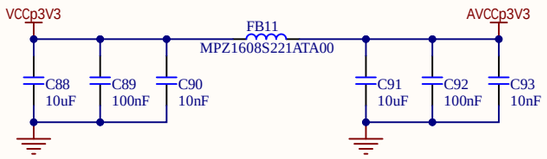
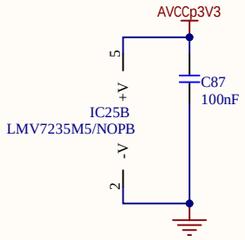
1PPS









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Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
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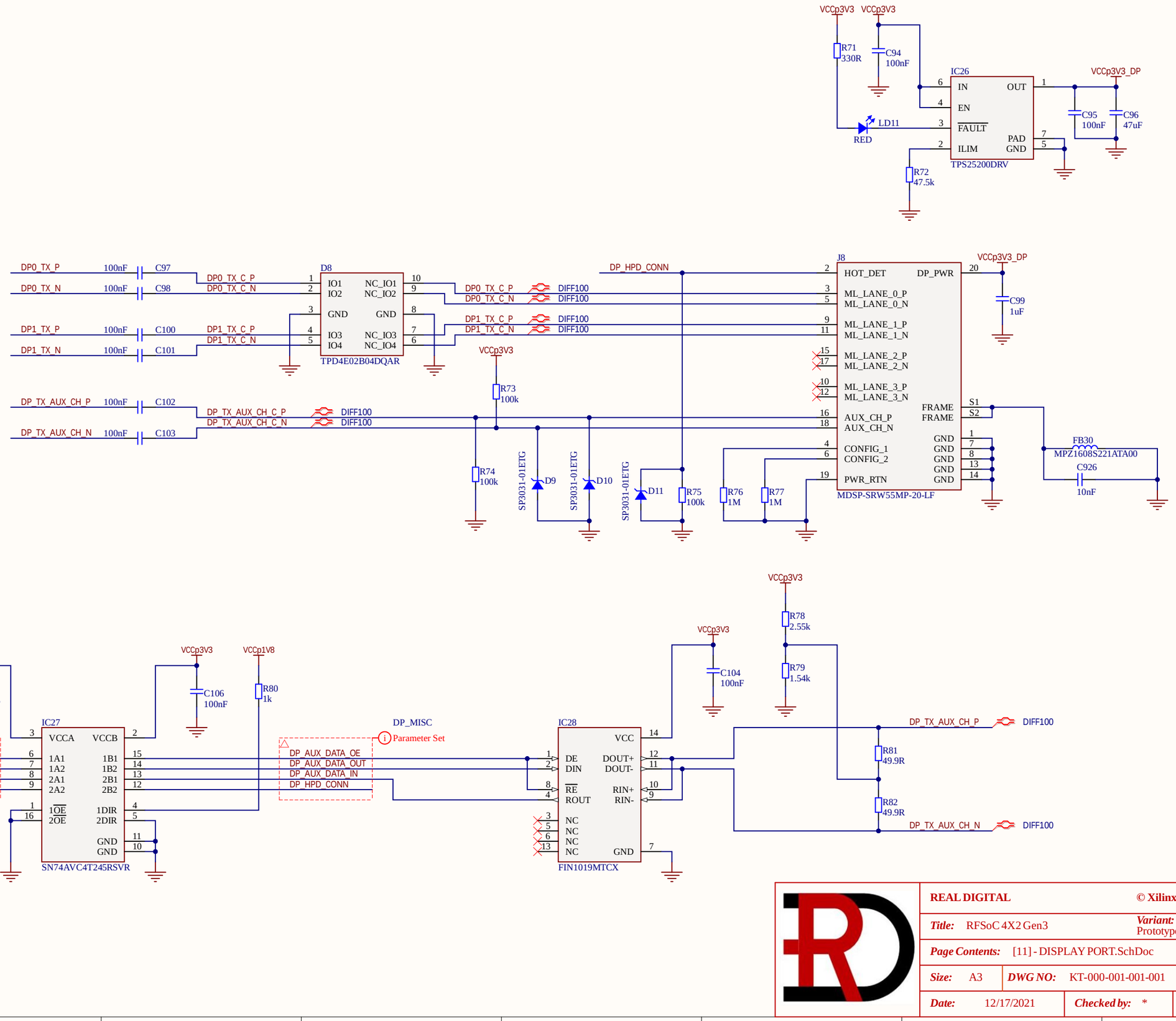
DISPLAY PORT



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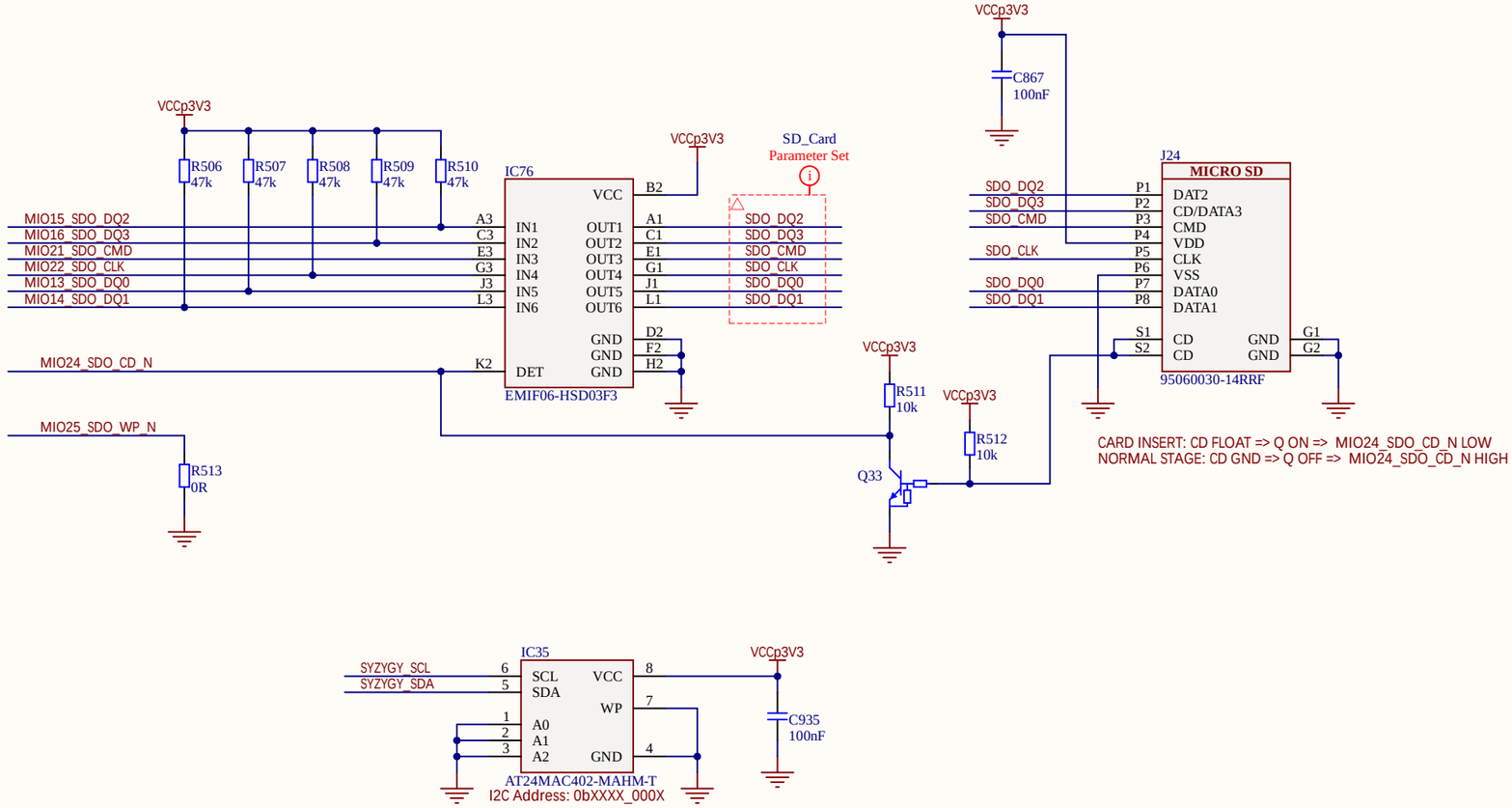
SD CARD



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Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [12] - SD CARD AND EEPROM.SchDoc			
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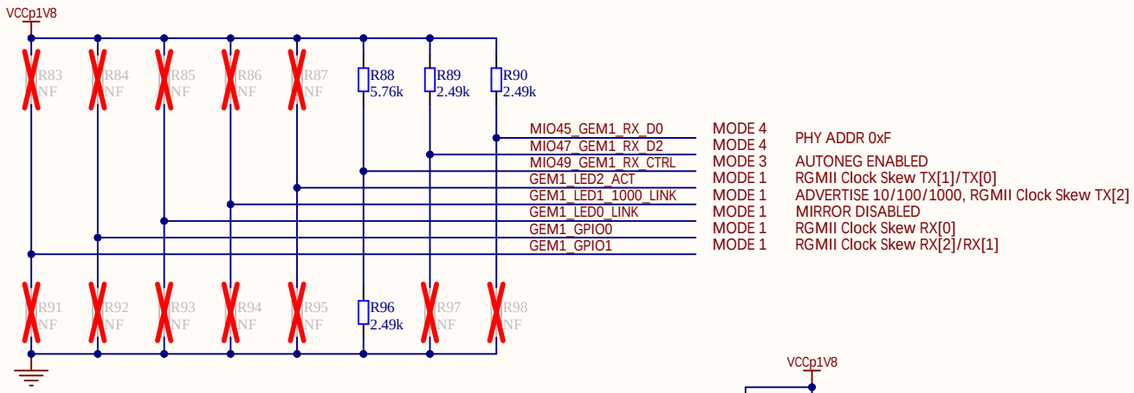
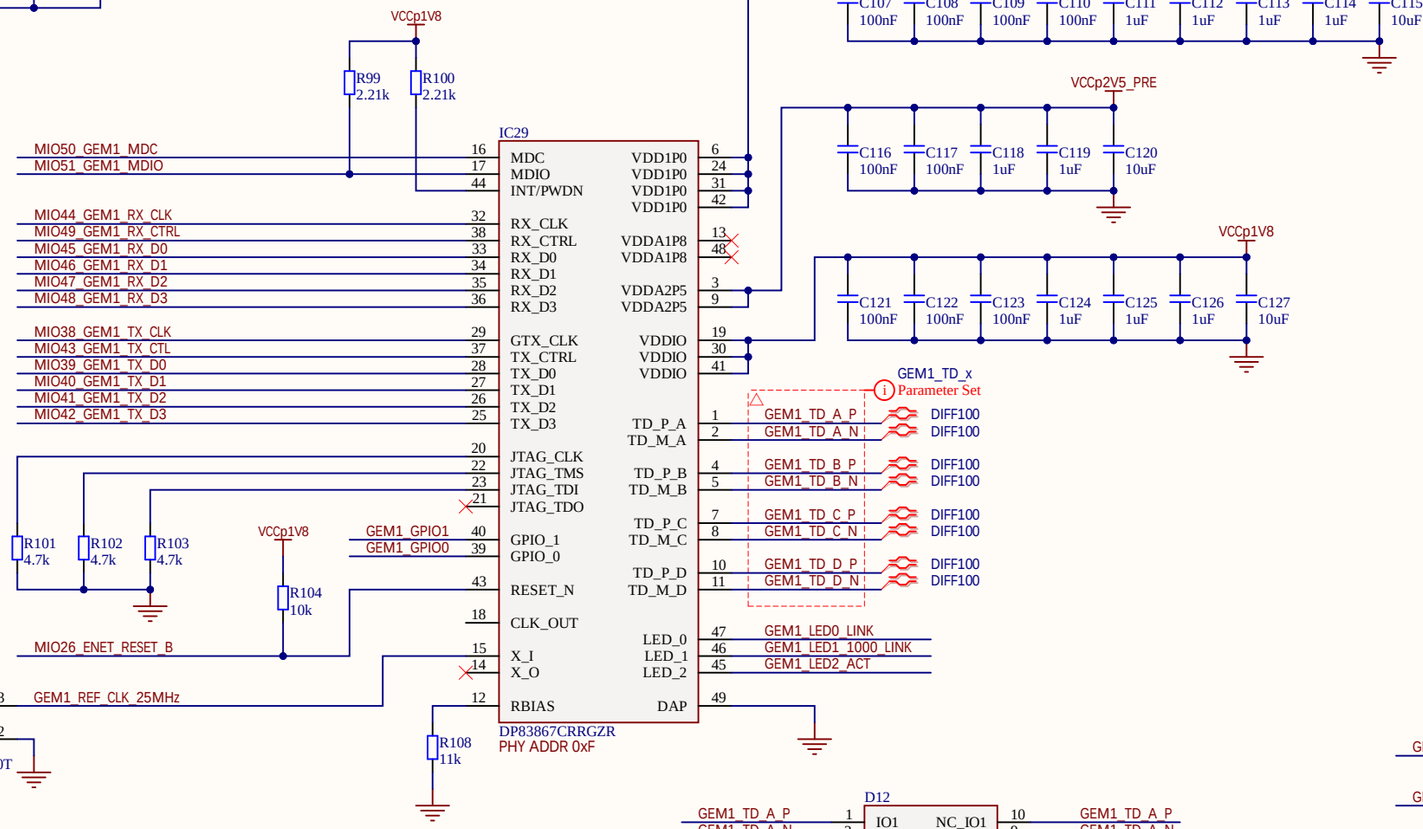
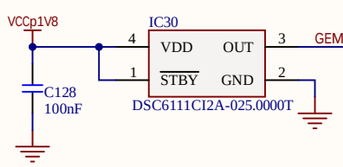
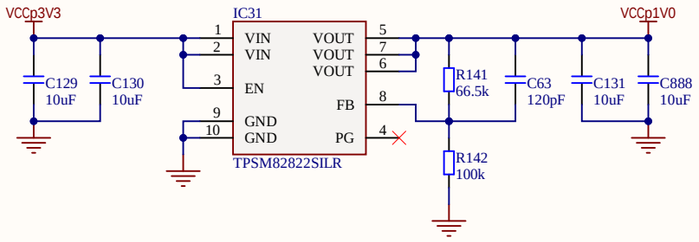
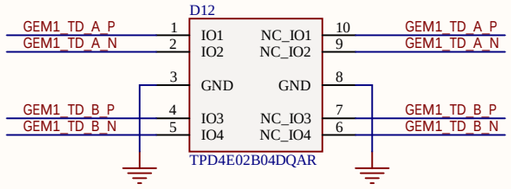
ETHERNET 1Gbit

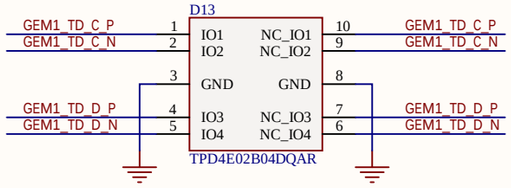


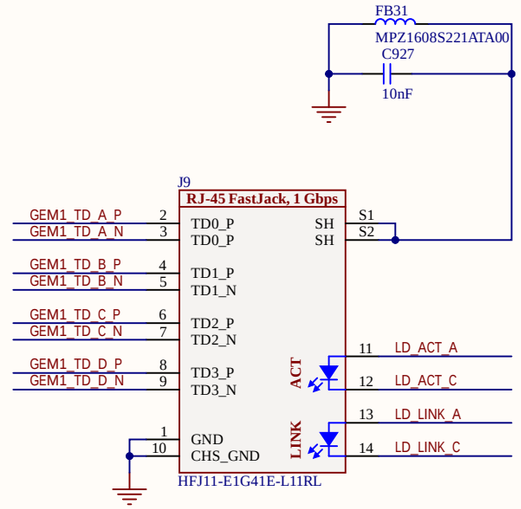


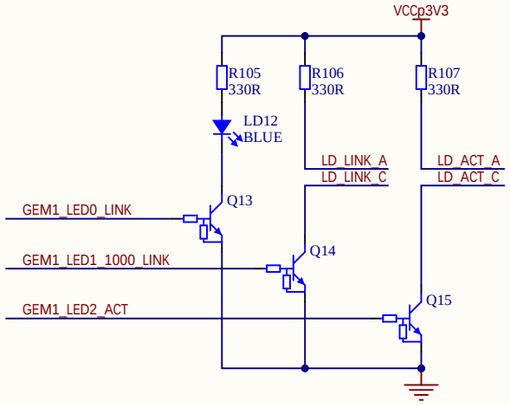












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Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
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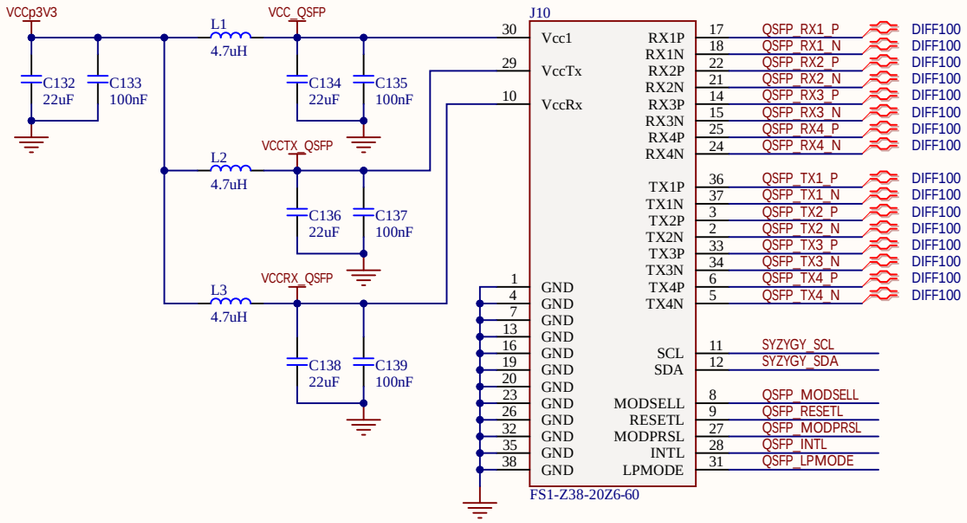
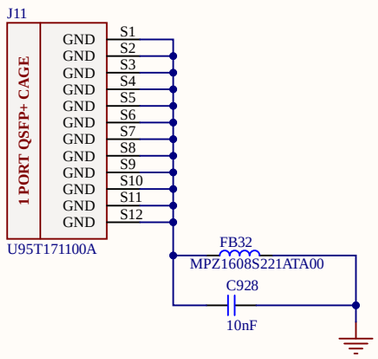
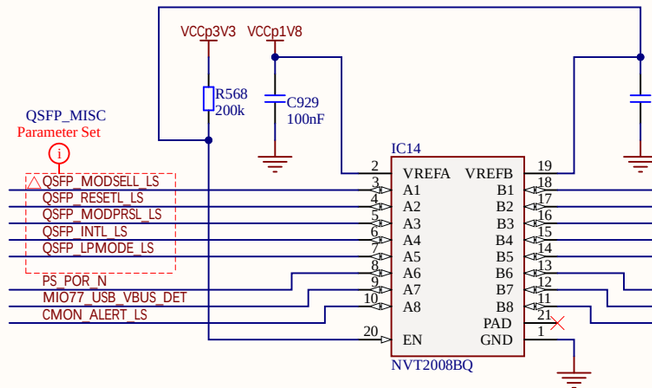
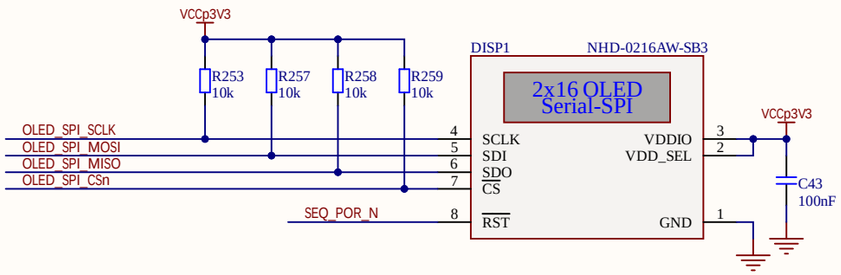
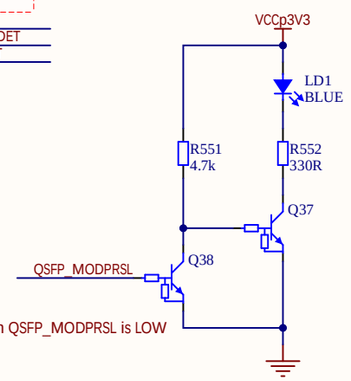
QSFP











SC1	Screw, Phillips, M2, 6mm	M2, 6mm	STDF1 SMD Standoff, M2, L:2.5mm 9774025243R
SC2	Screw, Phillips, M2, 6mm	M2, 6mm	STDF2 SMD Standoff, M2, L:2.5mm 9774025243R
SC3	Screw, Phillips, M2, 6mm	M2, 6mm	STDF3 SMD Standoff, M2, L:2.5mm 9774025243R
SC4	Screw, Phillips, M2, 6mm	M2, 6mm	STDF4 SMD Standoff, M2, L:2.5mm 9774025243R

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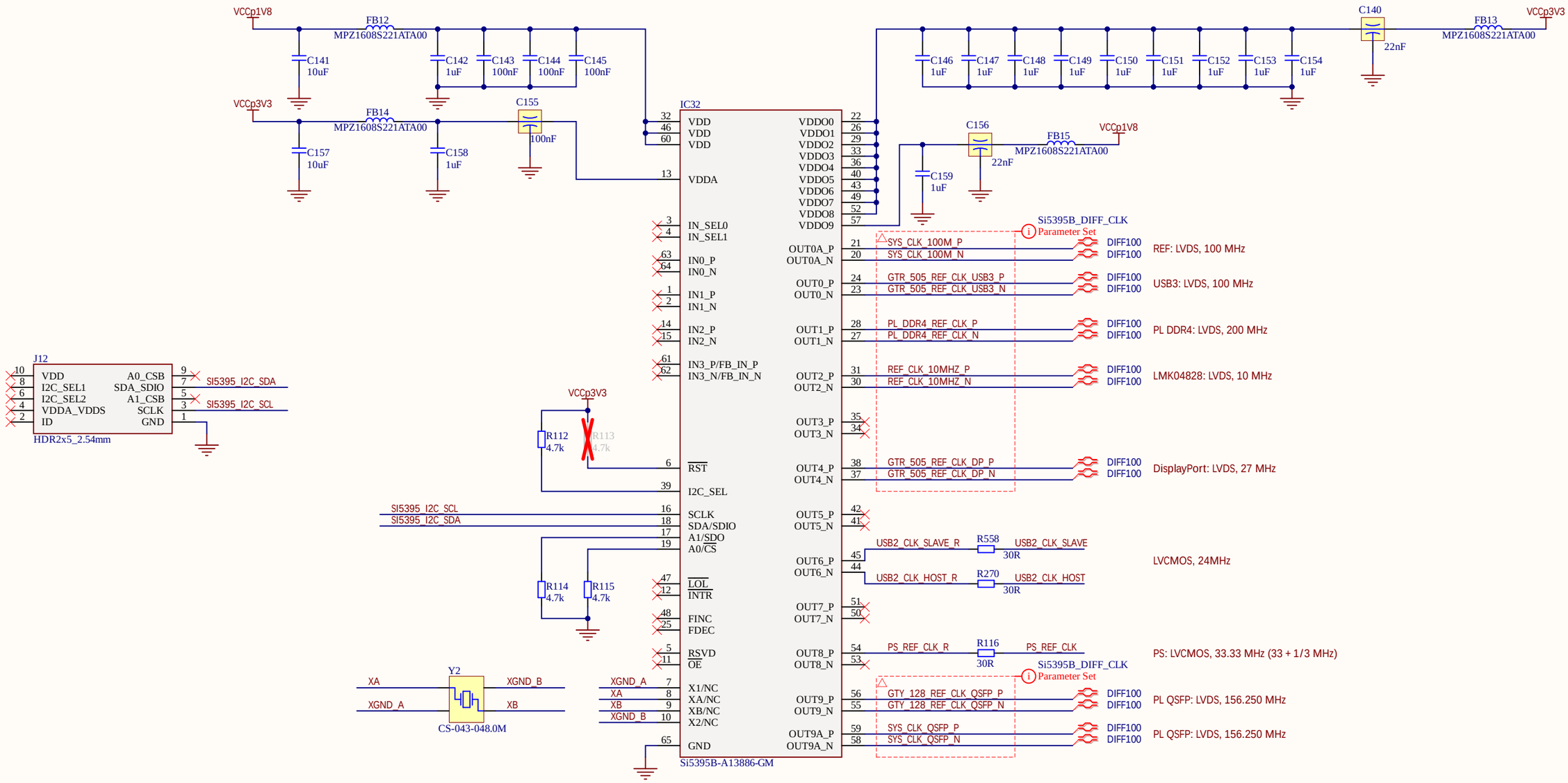
CLOCK I: SYS, DDR4, MGT, GTY AND USER



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Page Contents: [15] - CLOCK I.SchDoc	
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CLOCK II

IC33
LMK04828BISQX/NOPB

IC34
ABLJO-V-160.000MHZ

IC36
SN74LVC1G125DCKR

Locked Status
Locked Status
EXTERNAL INPUT REFERENCE
3dB Attenuator
Reference Clock of RF ADC
System Reference Clock of RF DAC
Reference Clock of RF DAC
Reference Clock I of RF-MPSoC
Reference Clock II of RF-MPSoC
Clock Out SMA

REAL DIGITAL
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Title: RFSoC 4X2 Gen3
Variant: Prototype
Page Contents: [16] - CLOCK II.SchDoc
Size: A3
DWG NO: KT-000-001-001-001
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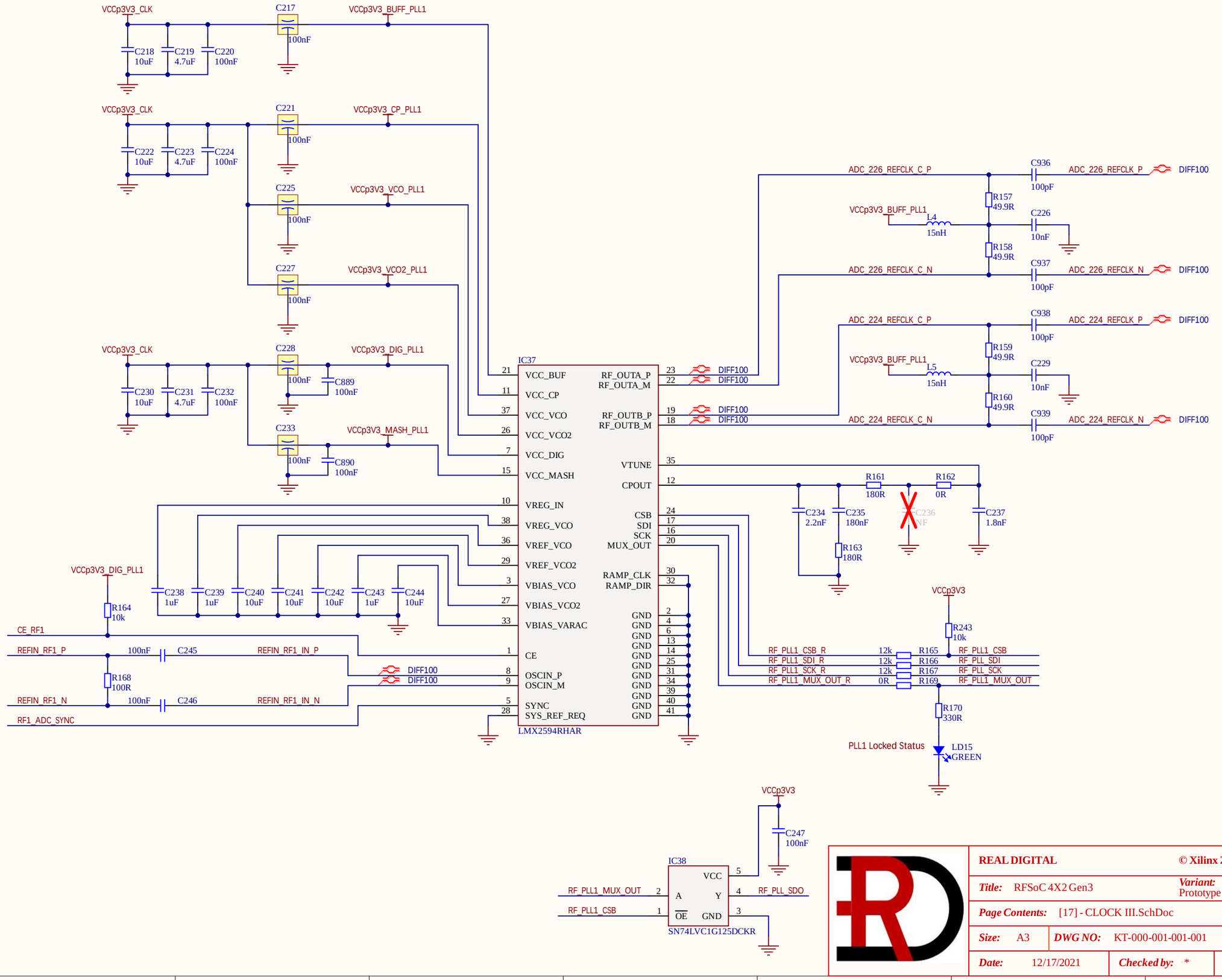
CLOCK III: RF ADC CLOCK



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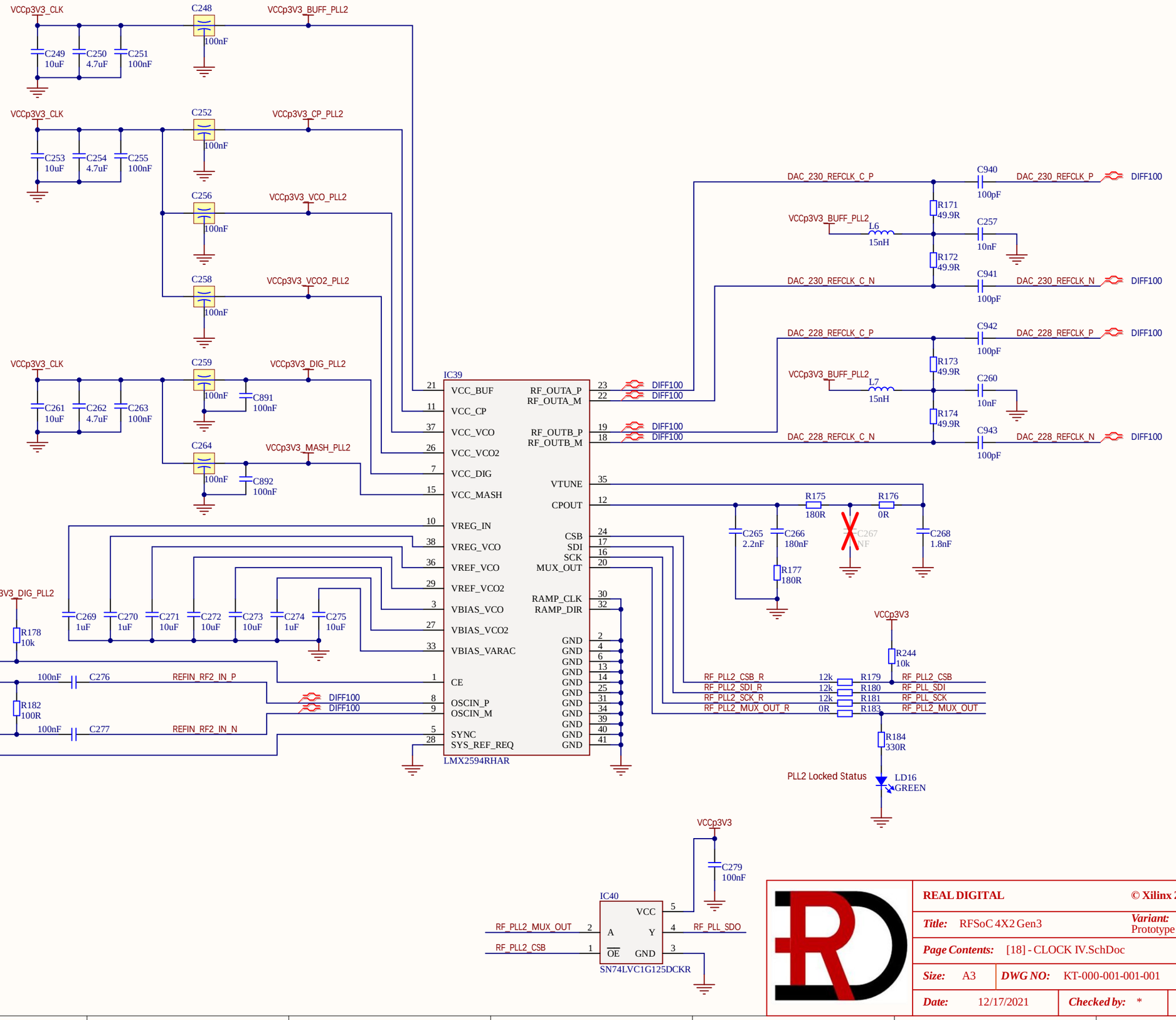
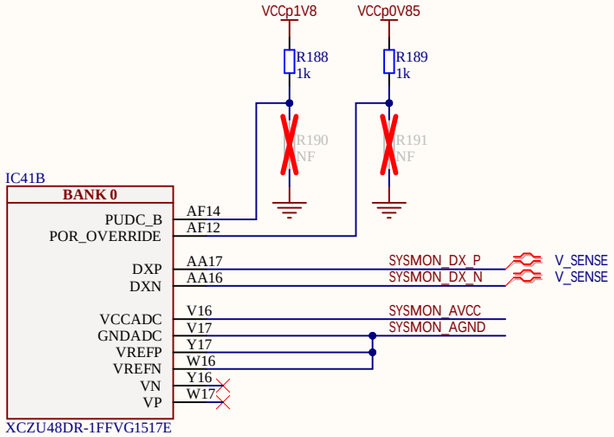
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [17] - CLOCK III.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 17 ***of*** 46	

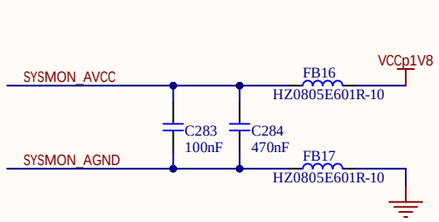
CLOCK IV: RF DAC CLOCK

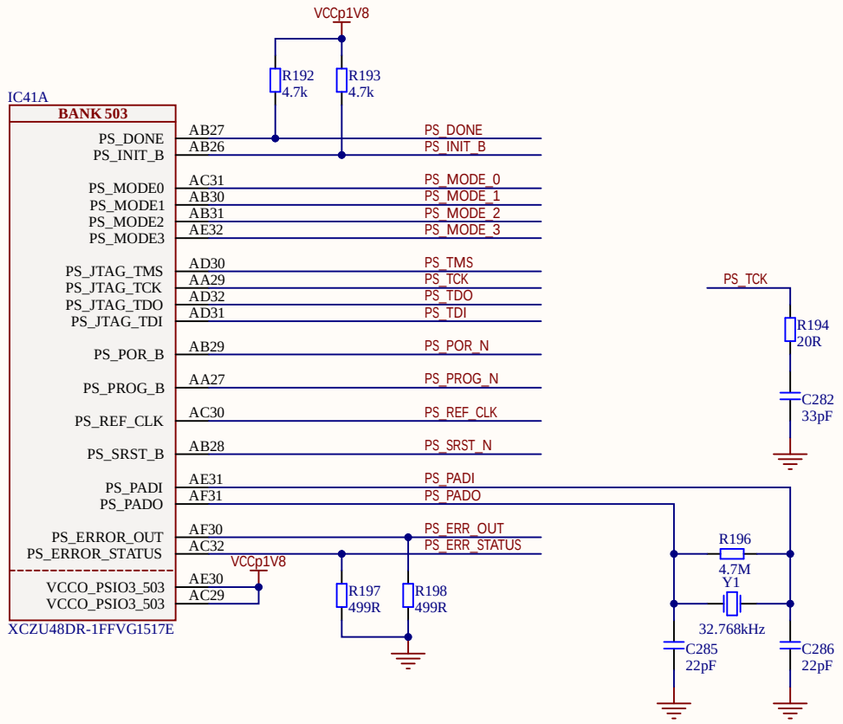


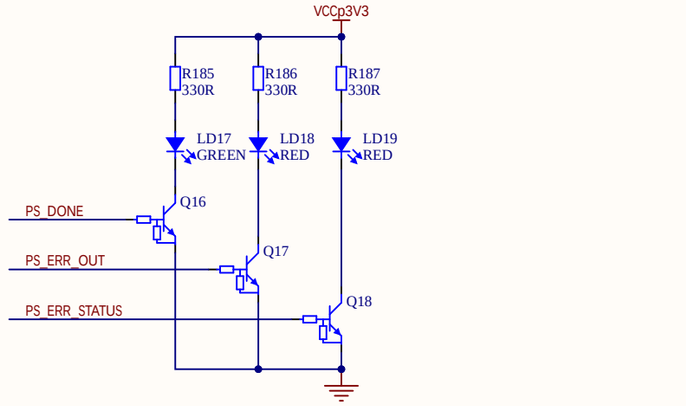
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [18] - CLOCK IV.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 18 ***of*** 46	

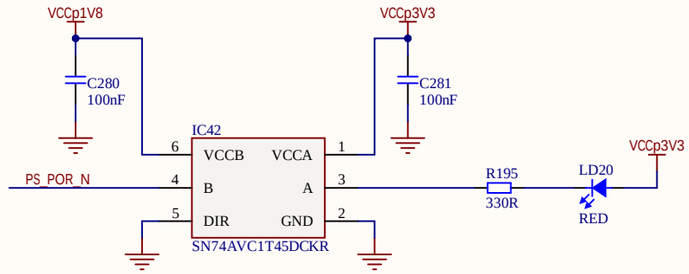
RFSoC CONFIG

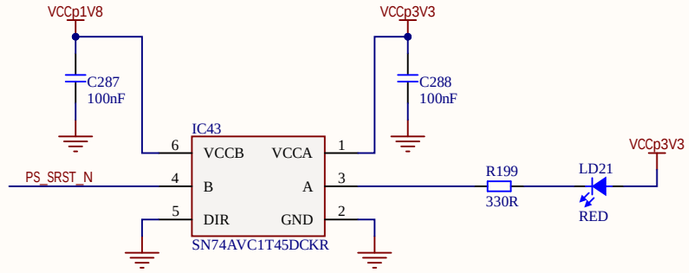


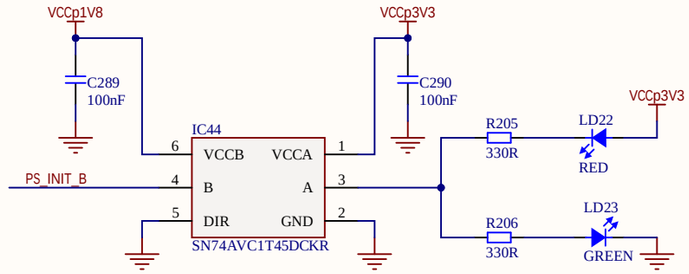


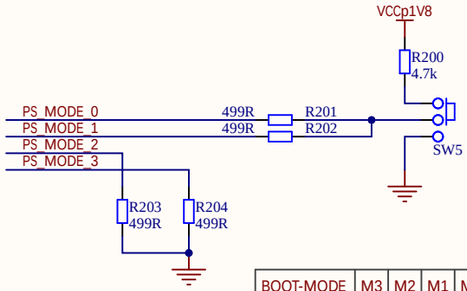




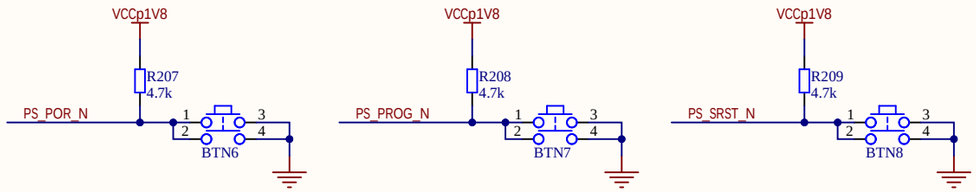








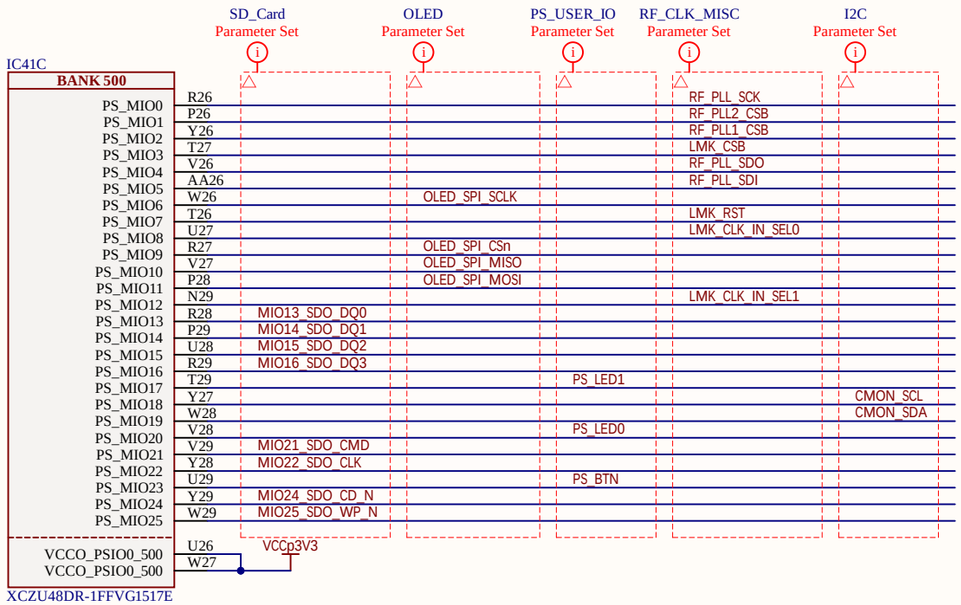
BOOT-MODE	M3	M2	M1	M0
JTAG	L	L	L	L
SD Card	L	L	H	H

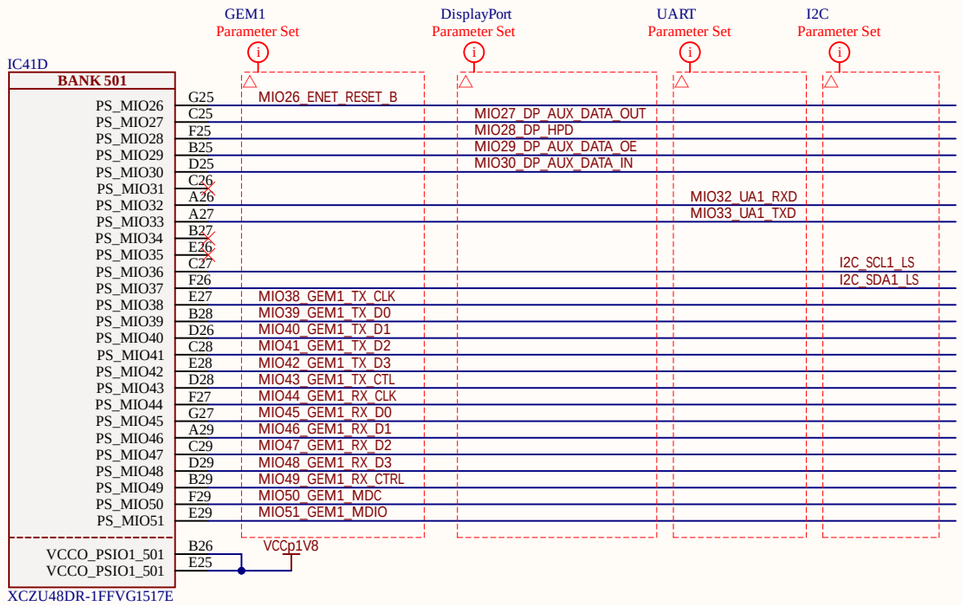


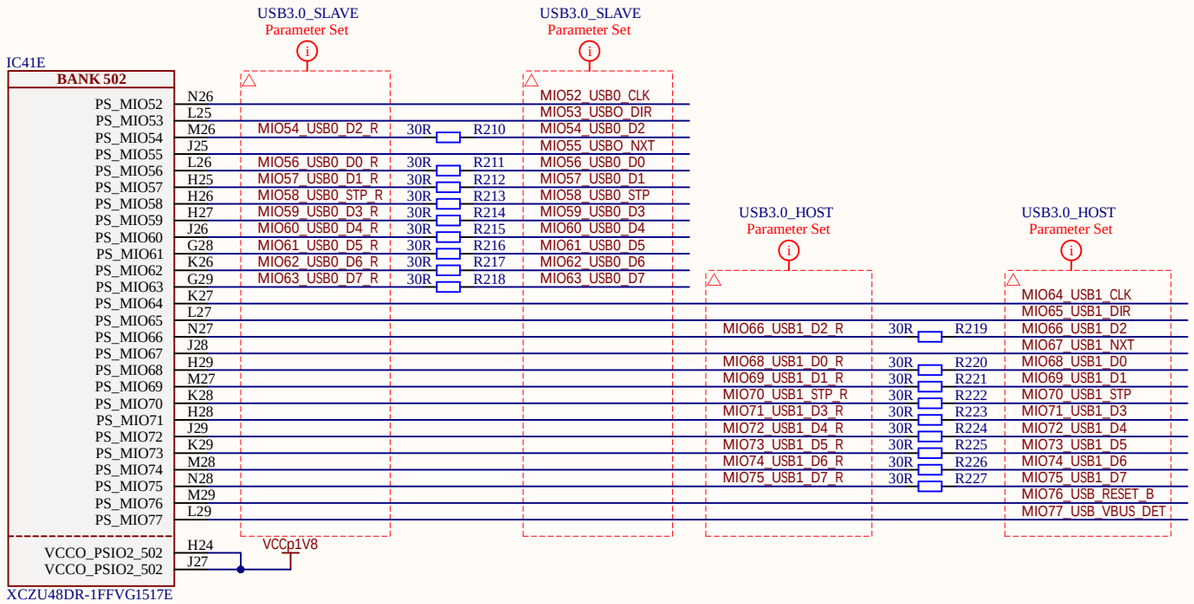
REAL DIGITAL © Xilinx 2021

Title: RFSoC 4X2 Gen3		*Variant:* Prototype
Page Contents: [19] - RFSoC CONFIG.SchDoc		
Size: A3	*DWG NO:* KT-000-001-001-001	*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 19 *of* 46

PS: BANKS 500-502

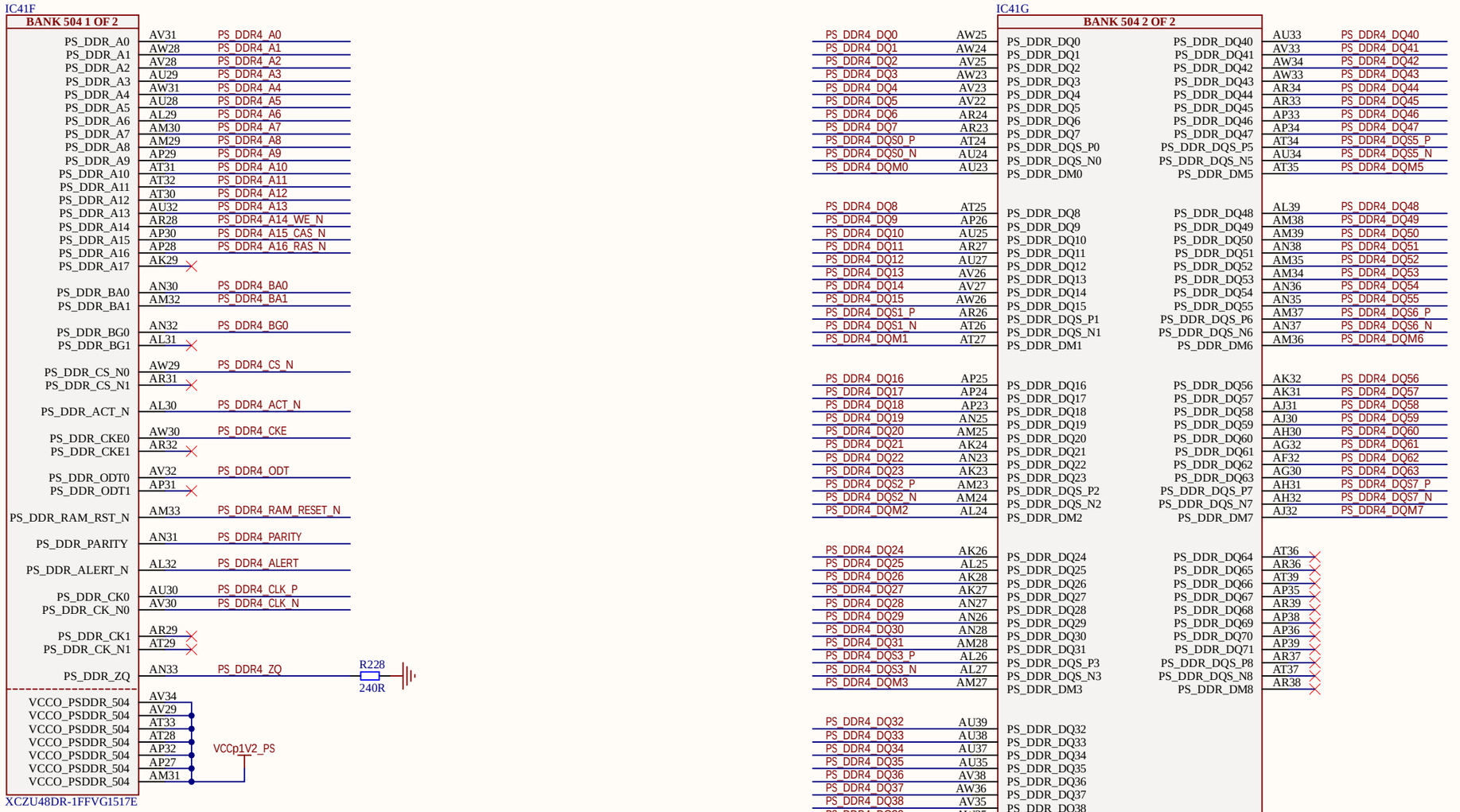






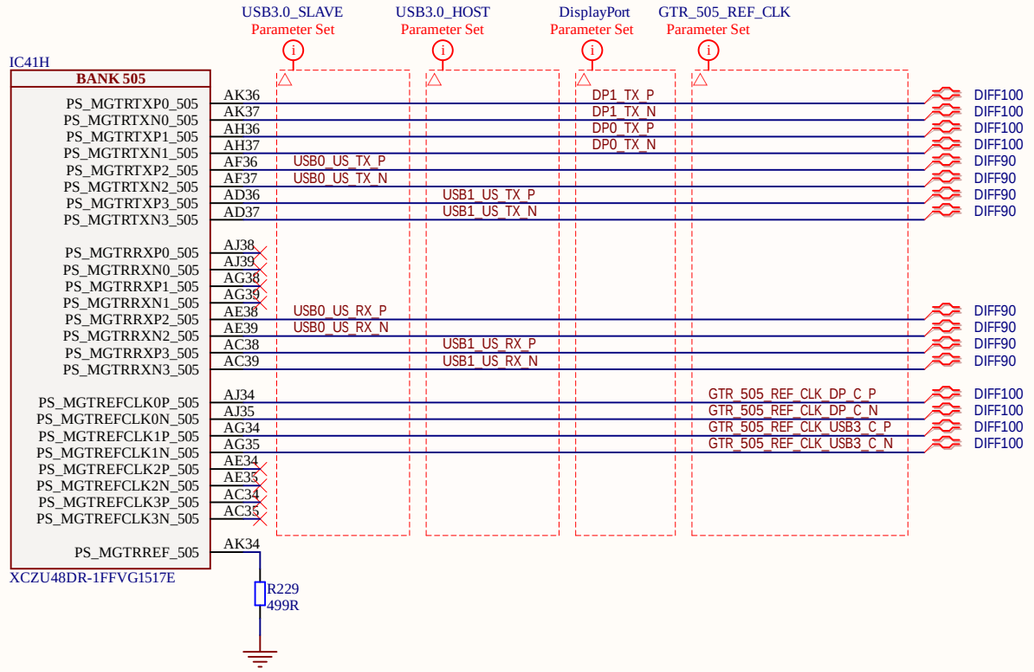
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [20] - PS BANKS 500-502.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 20 *of* 46	

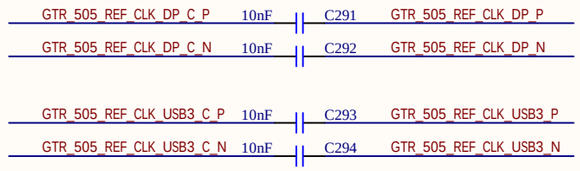
PS: BANK 504



REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [21] - PS BANK 504.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 21 ***of*** 46	

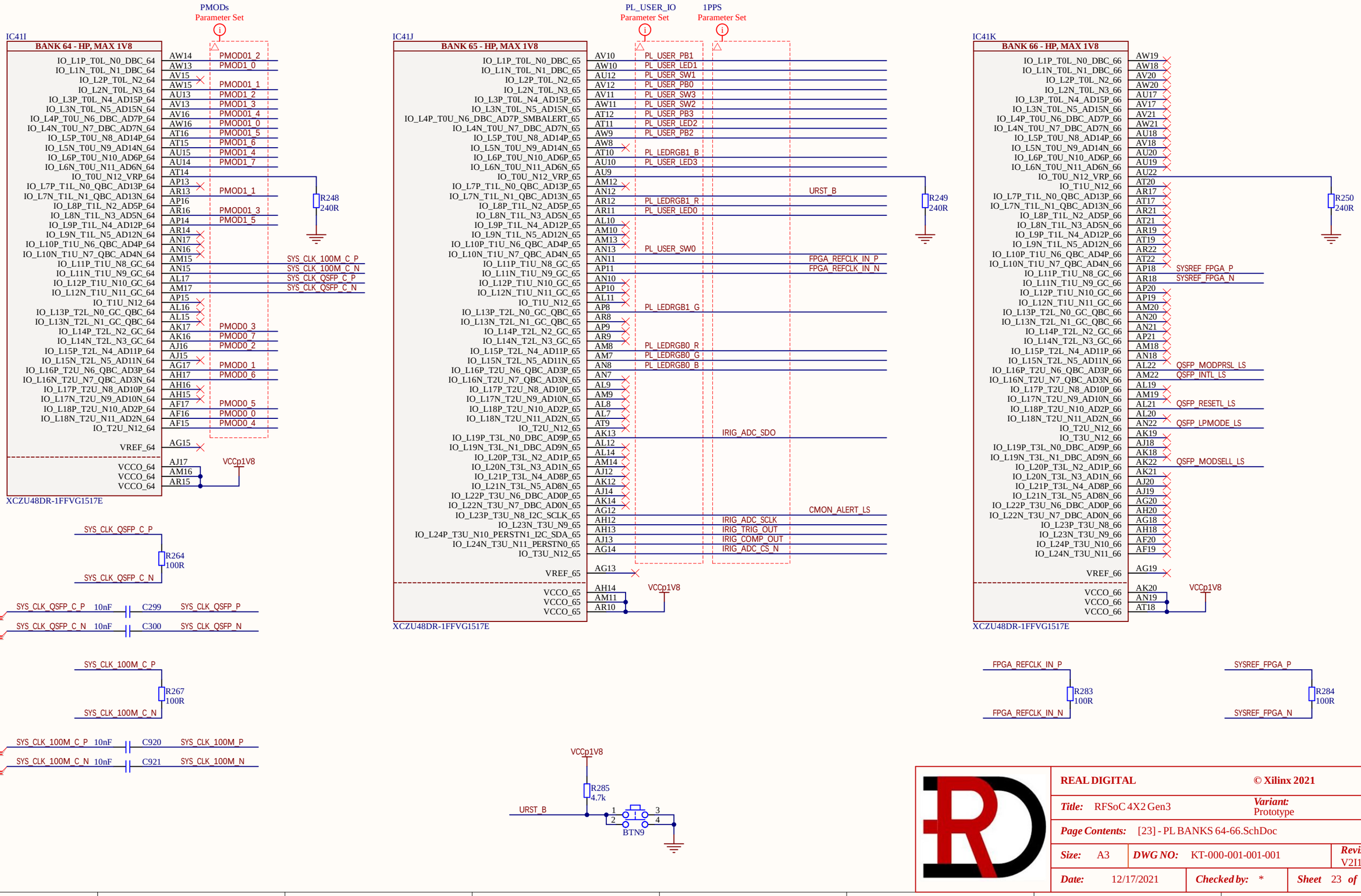
PS: MGT





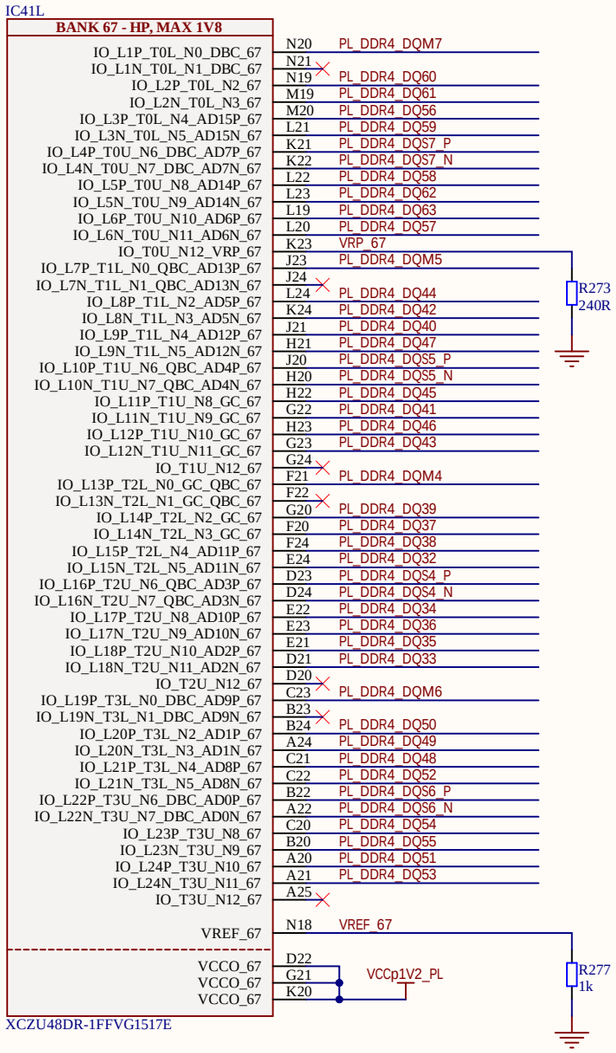
REAL DIGITAL			**© Xilinx 2021**
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [22] - PS MGT.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 22 ***of*** 46	

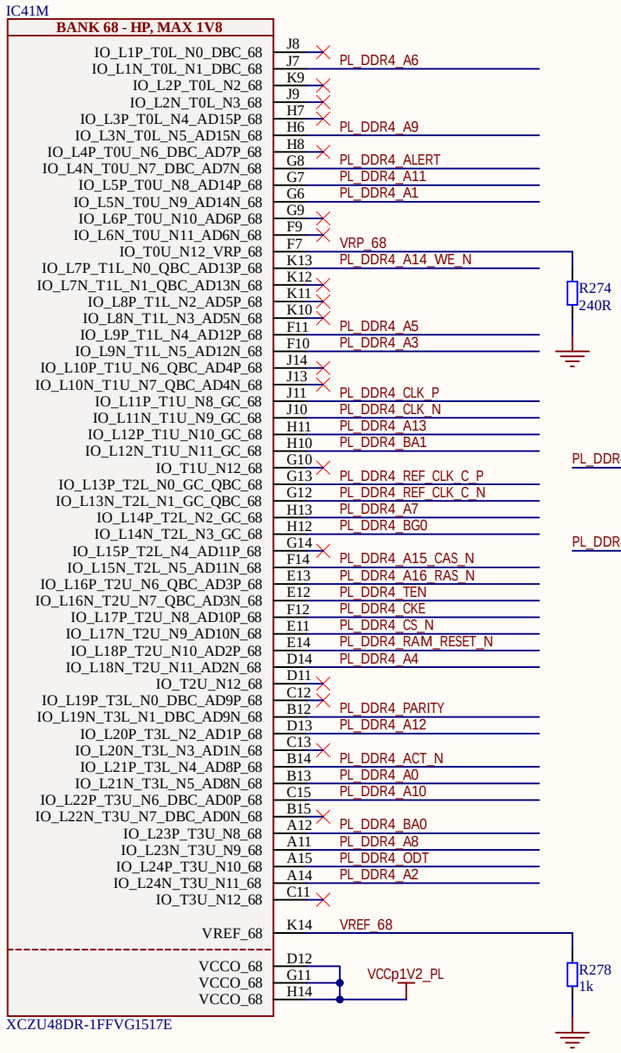
PL: BANKS 64-66

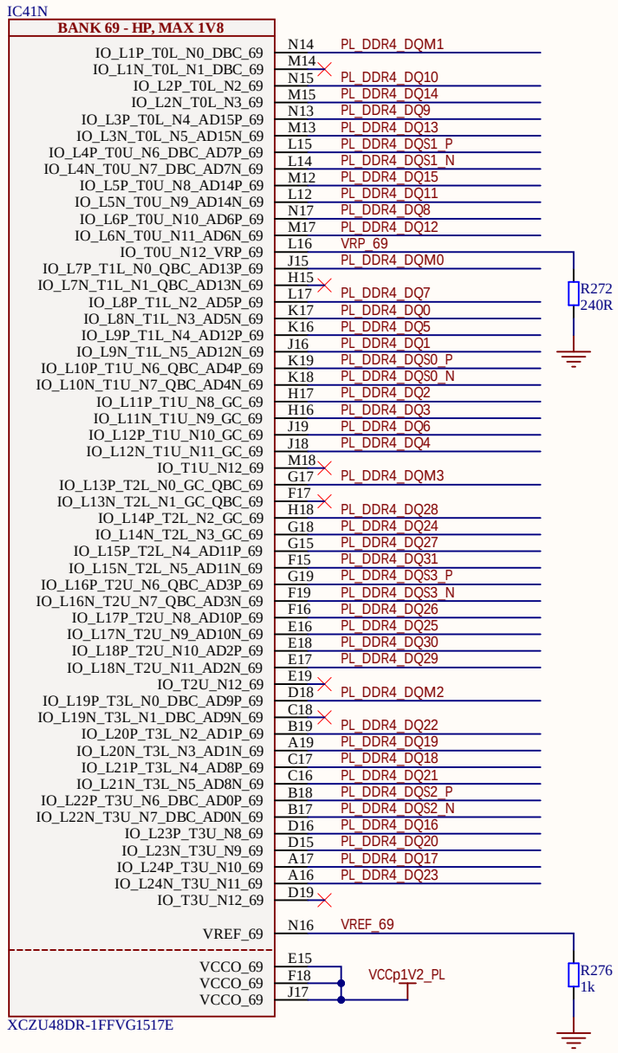


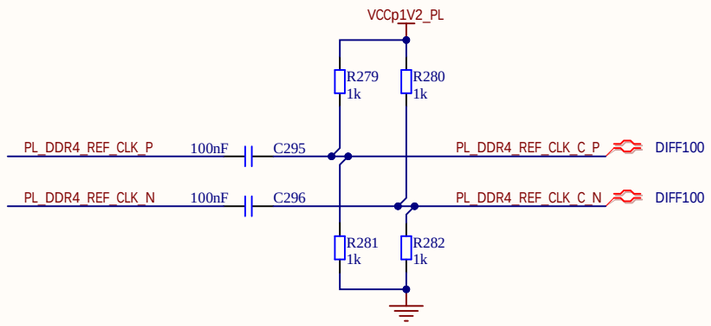
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [23] - PL BANKS 64-66.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 23 ***of*** 46	

PL: BANKS 67-69



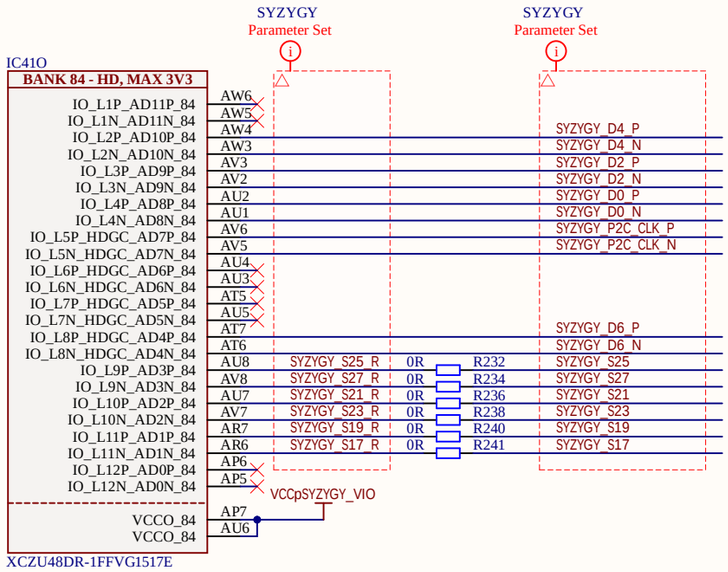


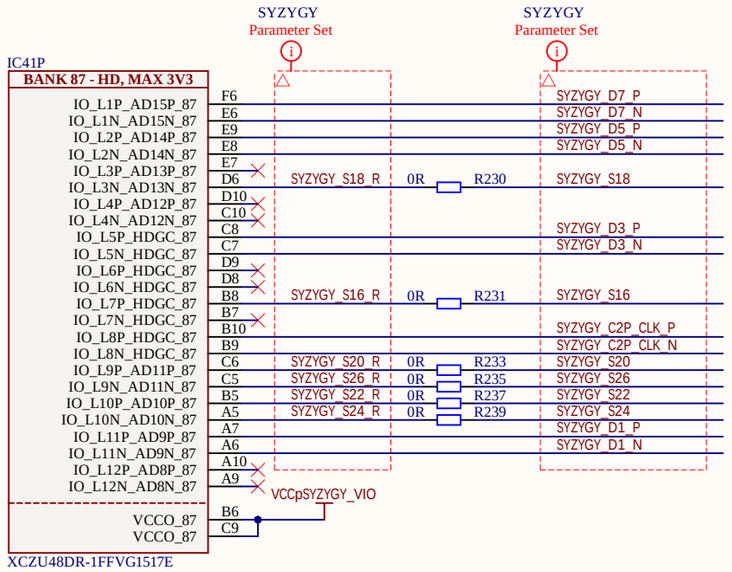


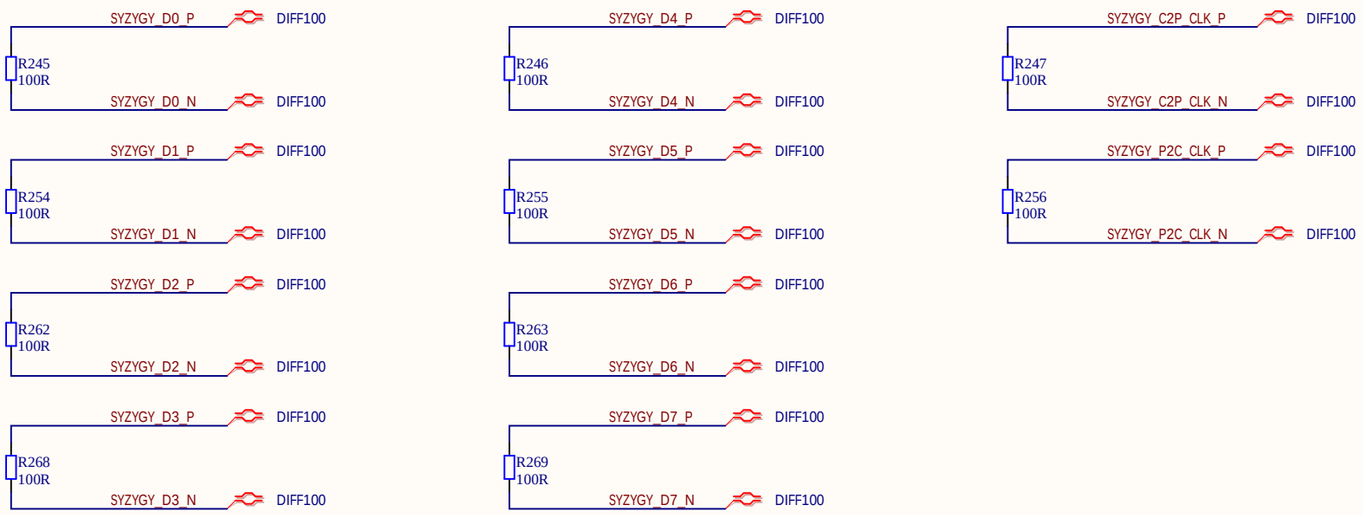


REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [24] - PL BANKS 67-69.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 24 ***of*** 46	

PL: BANKS 84, 87

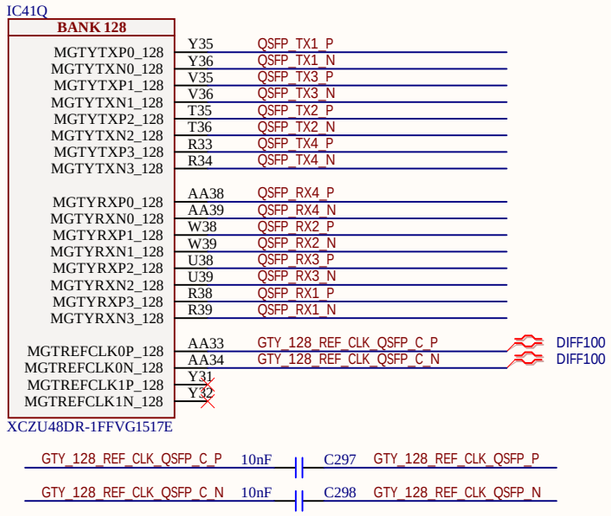


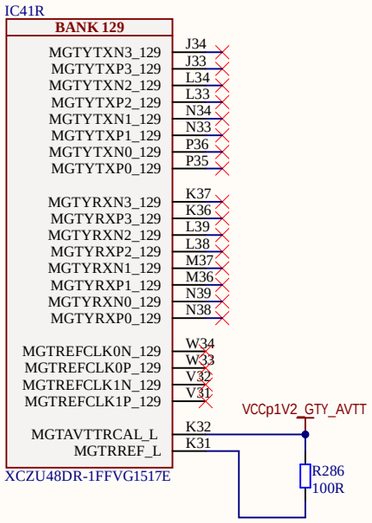


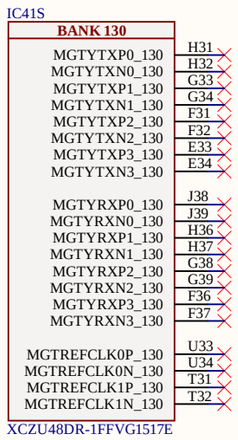


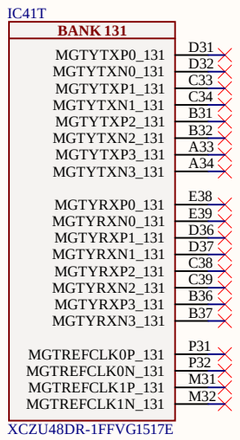
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [25] - PL BANKS 84, 87.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 25 ***of*** 46	

PL: GTY









REAL DIGITAL © Xilinx 2021

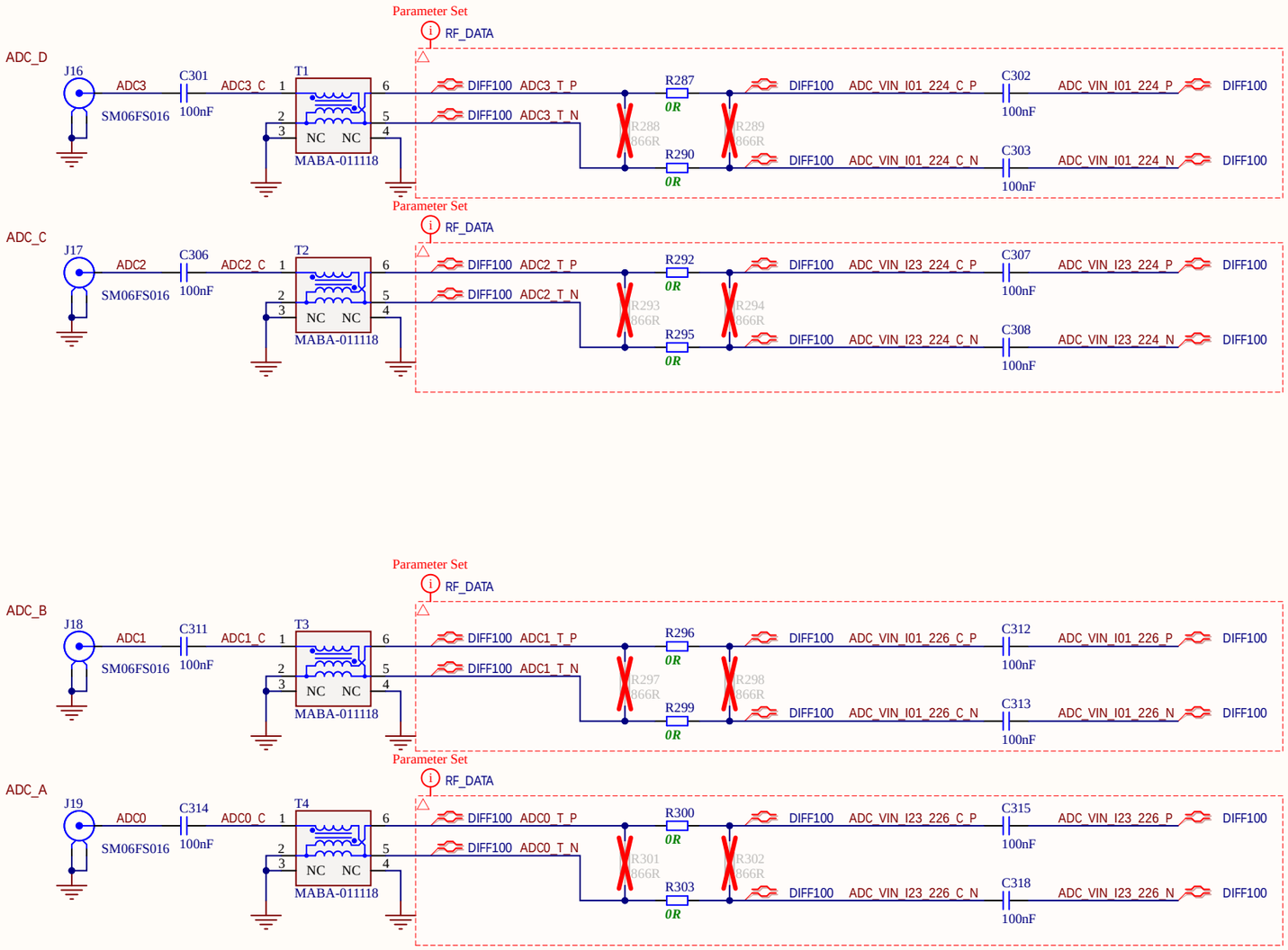
Title: RFSoC 4X2 Gen3 *Variant:* Prototype

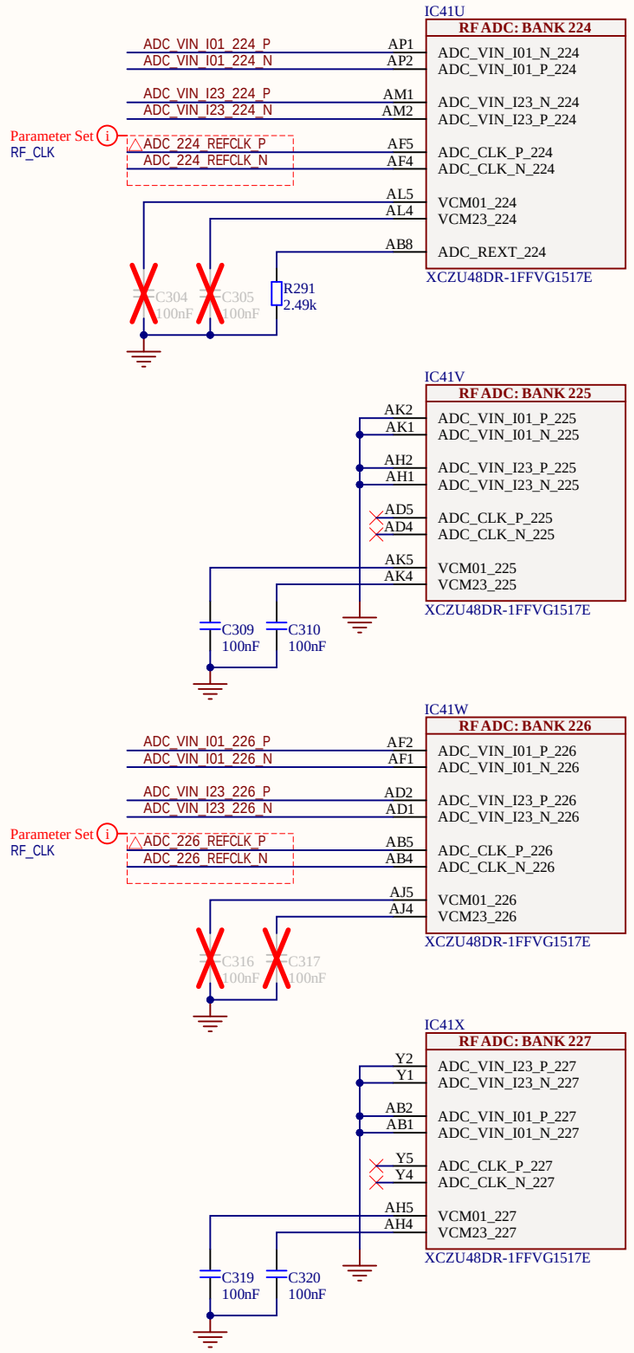
Page Contents: [26] - PL GTY.SchDoc

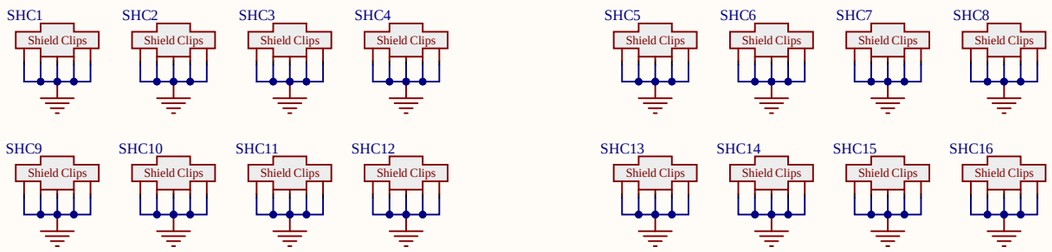
Size: A3 *DWG NO:* KT-000-001-001-001 *Revison:* V2I1

Date: 12/17/2021 *Checked by:* * *Sheet* 26 *of* 46

RF ADC

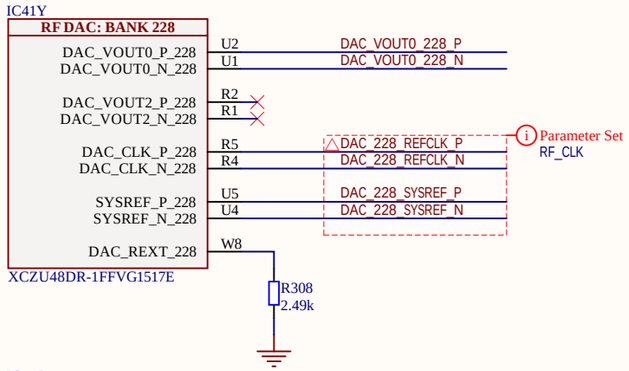


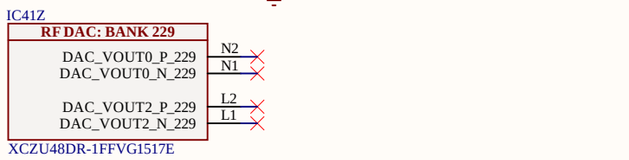


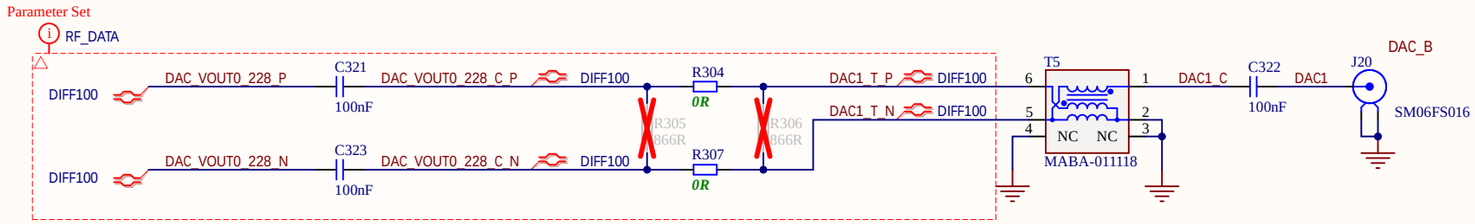


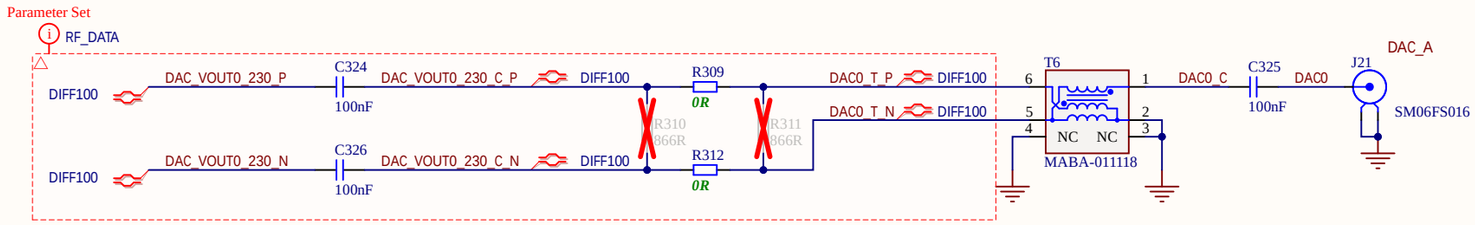
REAL DIGITAL			© Xilinx 2021
Title: RFSoC 4X2 Gen3			*Variant:* Prototype
Page Contents: [27] - RF ADC.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 27 *of* 46	

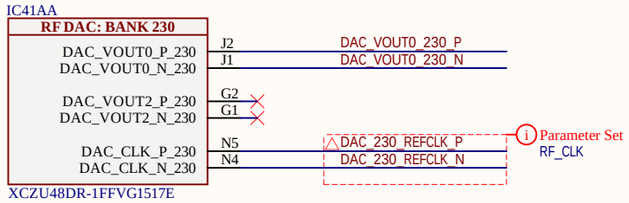
RF DAC

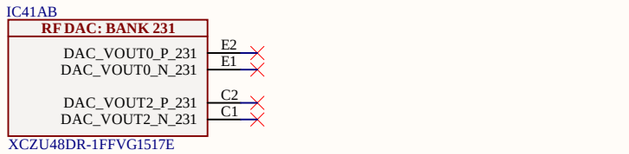


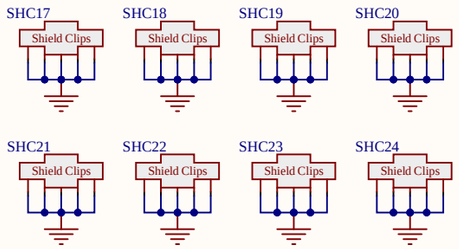






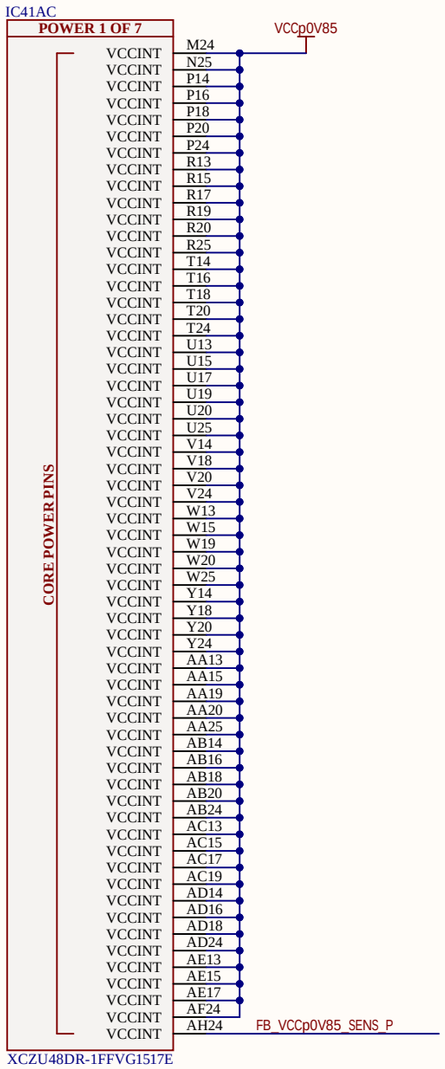


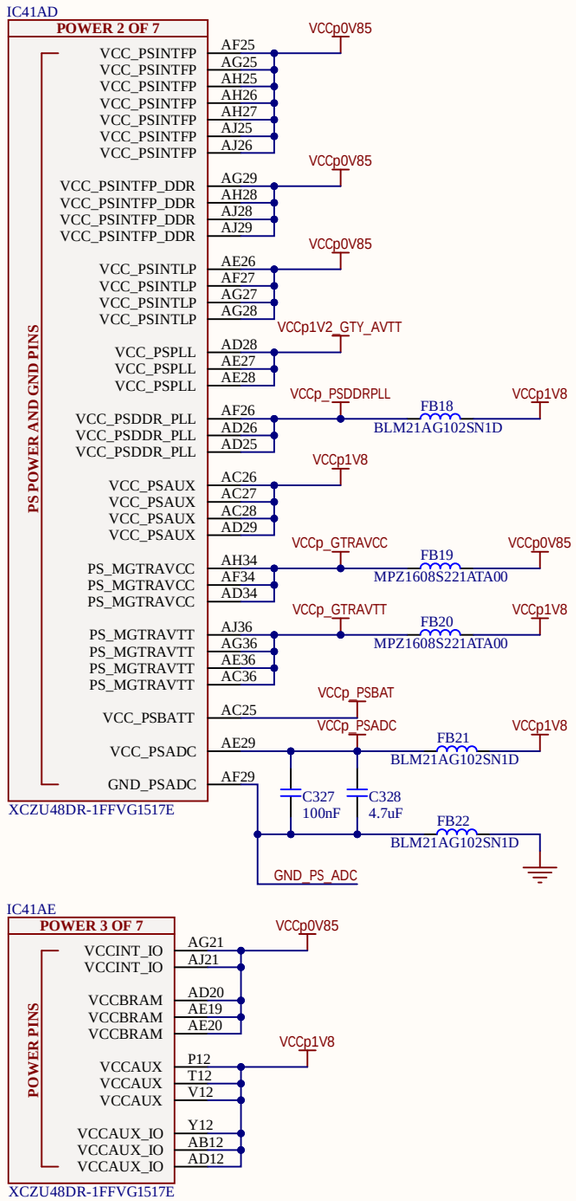


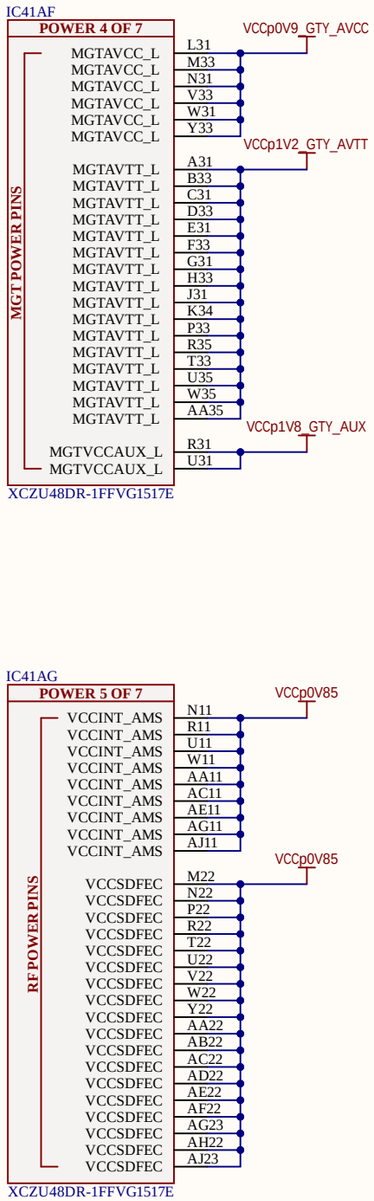


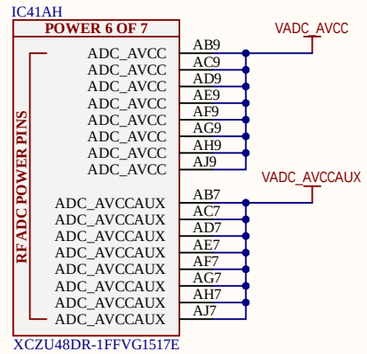
REAL DIGITAL	**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3	***Variant:*** Prototype	
Page Contents: [28] - RF DAC.SchDoc		
Size: A3	***DWG NO:*** KT-000-001-001-001	***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 28 ***of*** 46

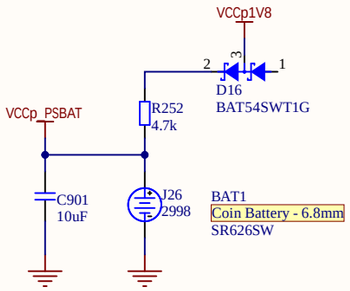
RFSoC POWER Pins







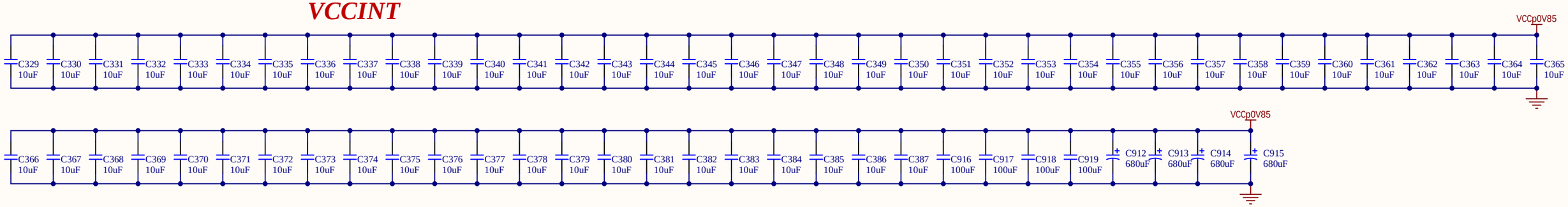




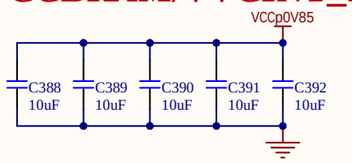
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [29] - RFSoC POWER Pins.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 29 ***of*** 46	

DECOUPLING

VCCINT



VCCBRAM/VVCINT_IO



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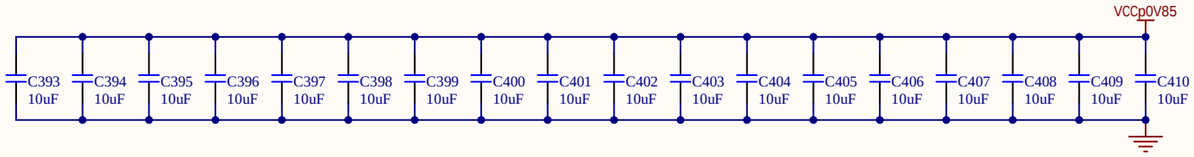
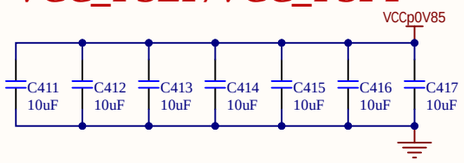
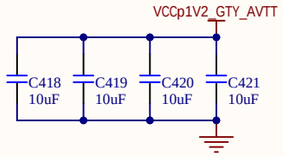


VCC_PSLP/VCC_PSFP



GTY AVTT



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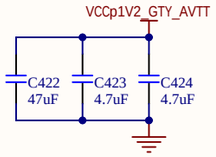

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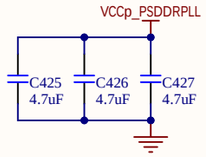

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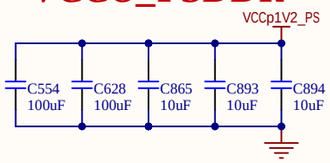
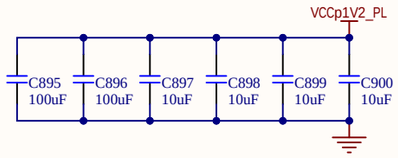
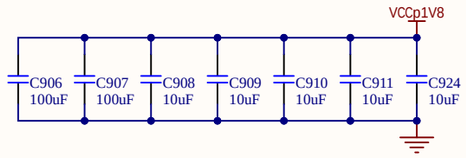


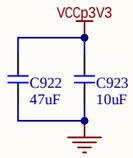
VCCO PLDDR



VCCO 1V8



VCCO 3V3



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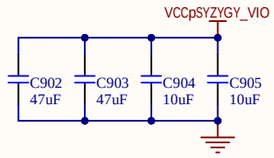
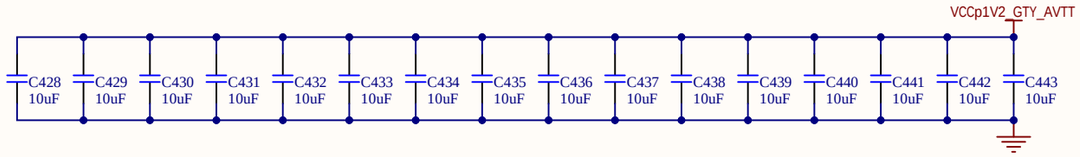


MGTAVTT



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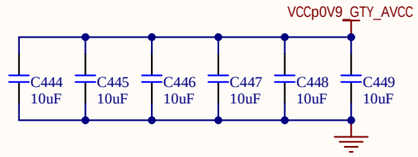
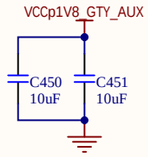
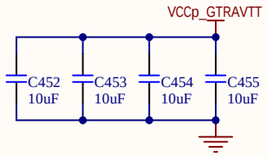


MGTVAUX



MGTRAVTT



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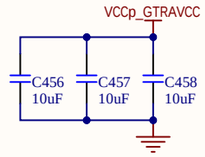
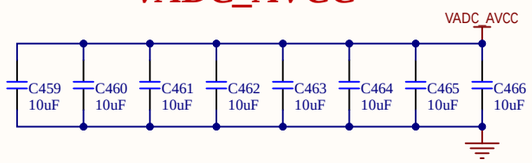
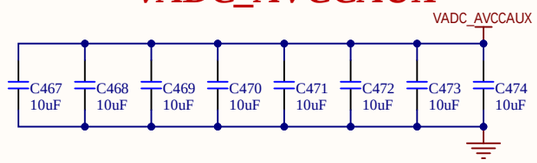


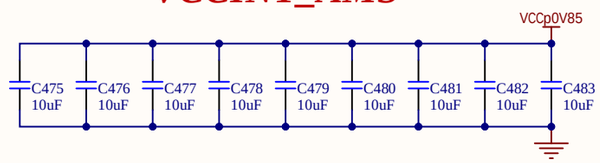
VADC_AVCC



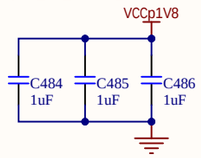
VADC_AVCCAUX



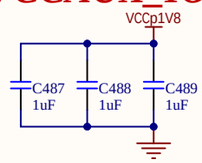
VCCINT_AMS



VCCAUX



VCCAUX_IO



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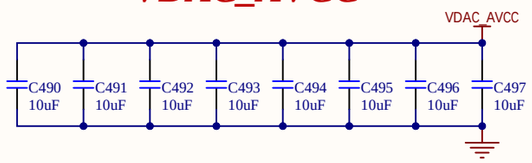

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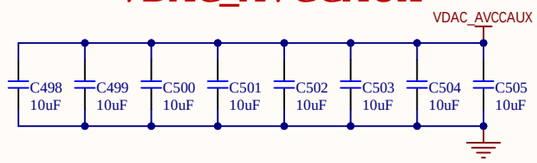

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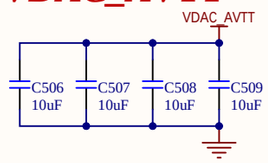
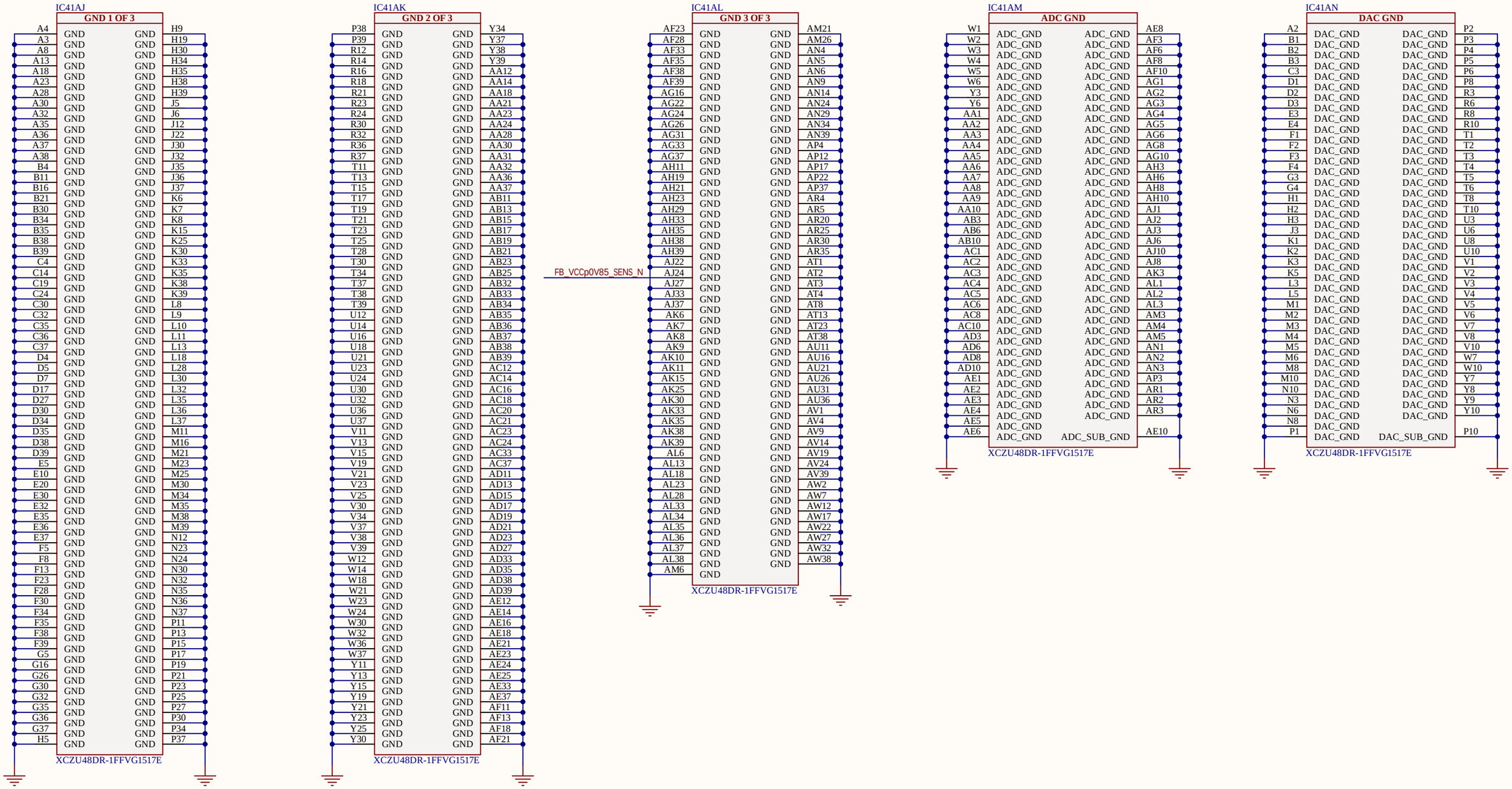


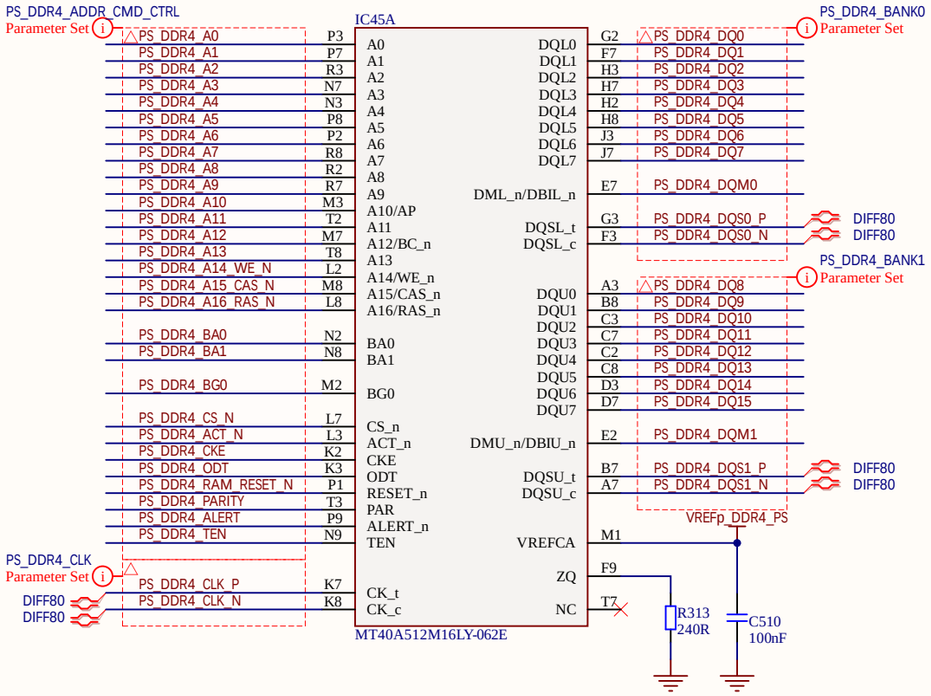
REAL DIGITAL		**© Xilinx 2021**
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype
Page Contents: [30] - RFSoC DECOUPLING.SchDoc		
Size: A3	***DWG NO:*** KT-000-001-001-001	***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 30 ***of*** 46

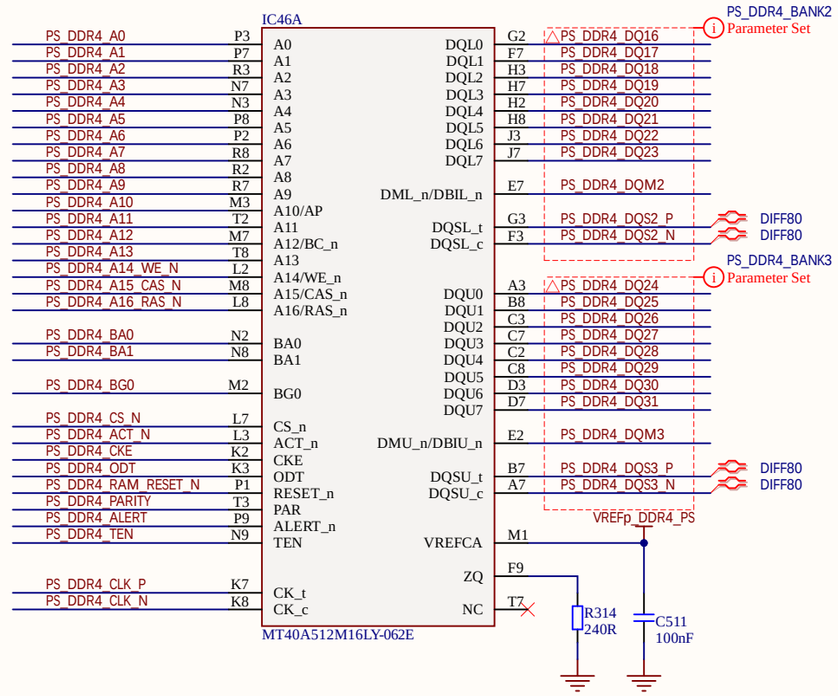
RFSoC GND Pins

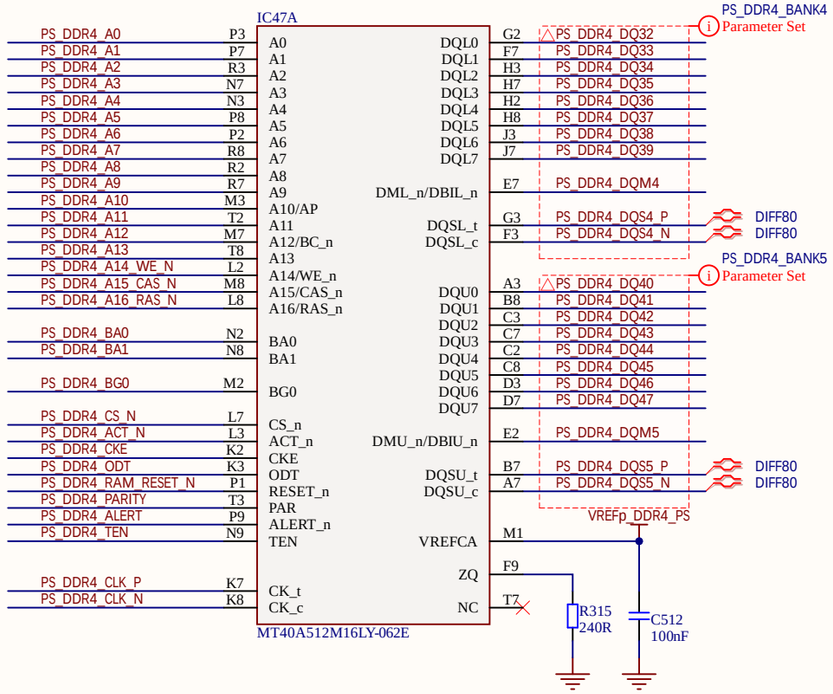


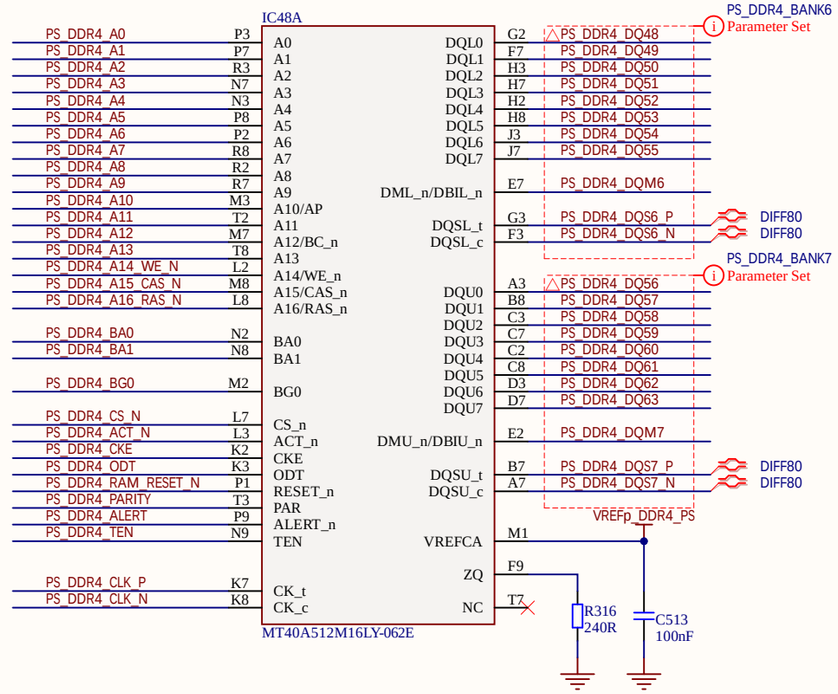
REAL DIGITAL		© Xilinx 2021	
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [31] - RFSoC GND Pins.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 31 *of* 46	

DDR4 MEMORY PS I



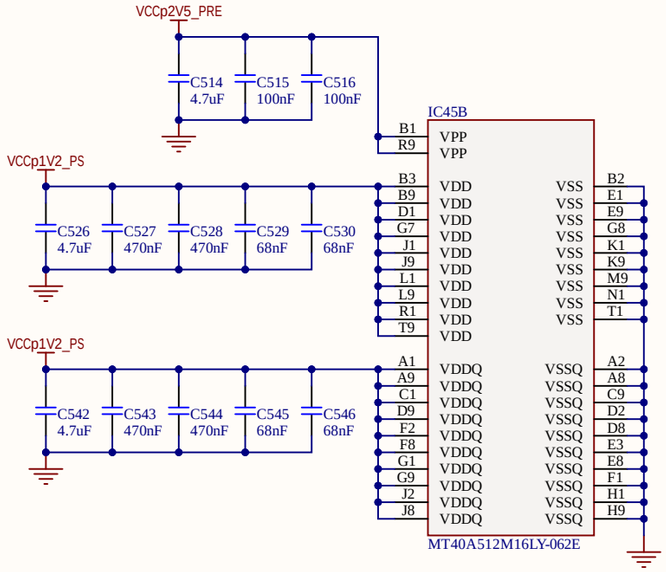


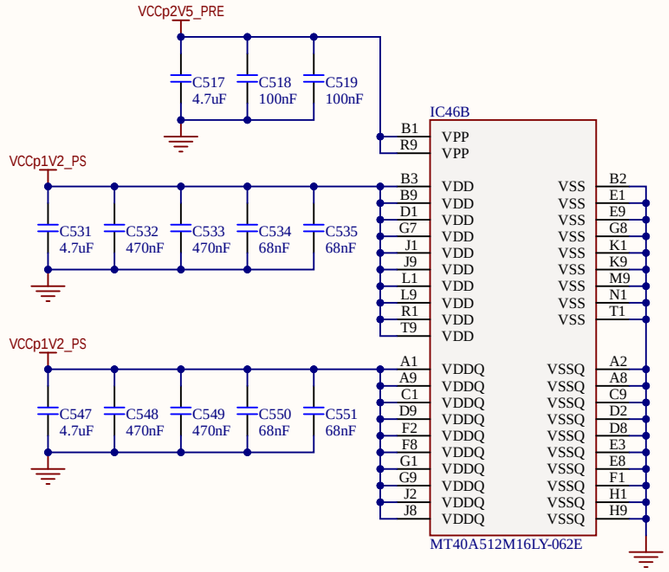


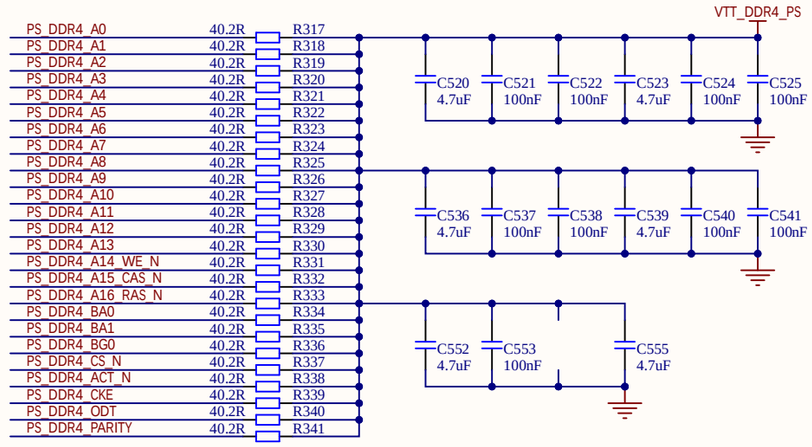


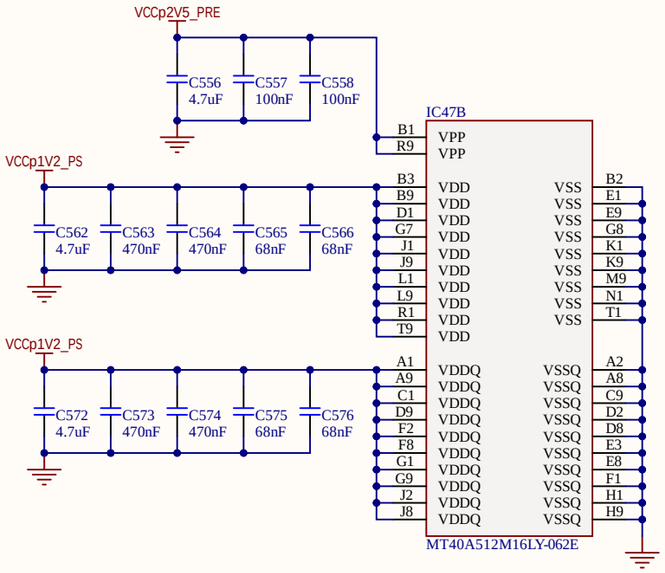
REAL DIGITAL			**© Xilinx 2021**
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [32] - DDR4 MEMORY PS I.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 32 ***of*** 46	

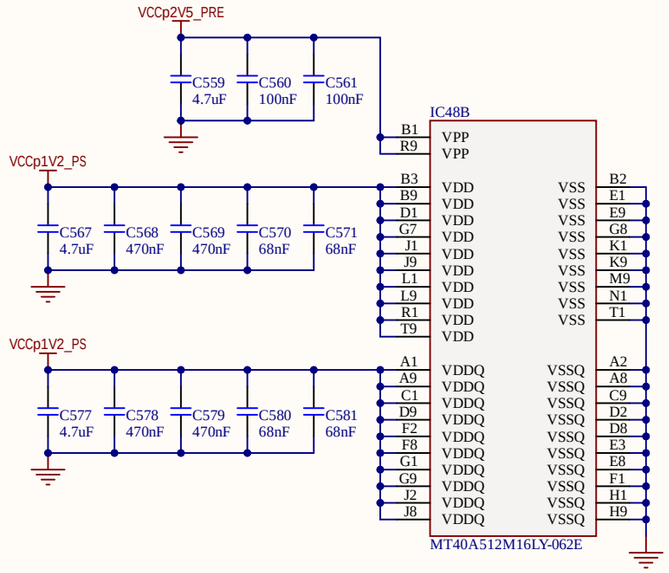
DDR4 MEMORY PS II

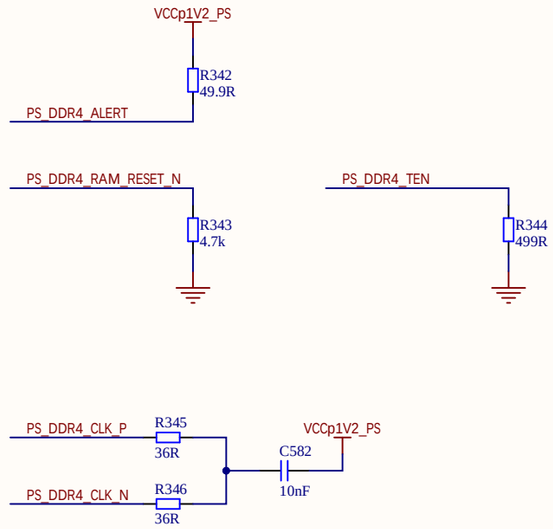






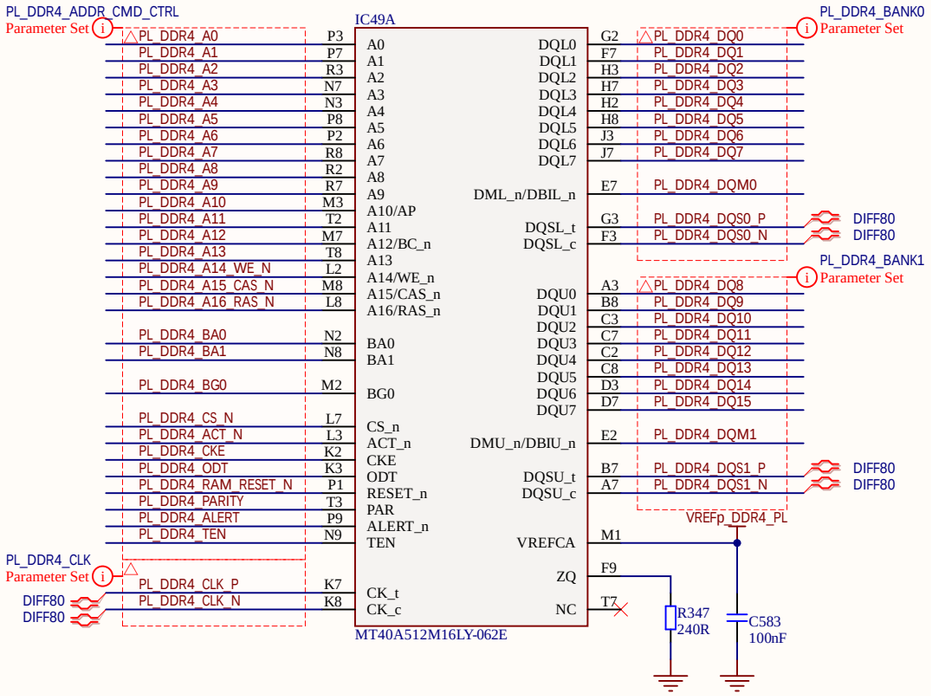


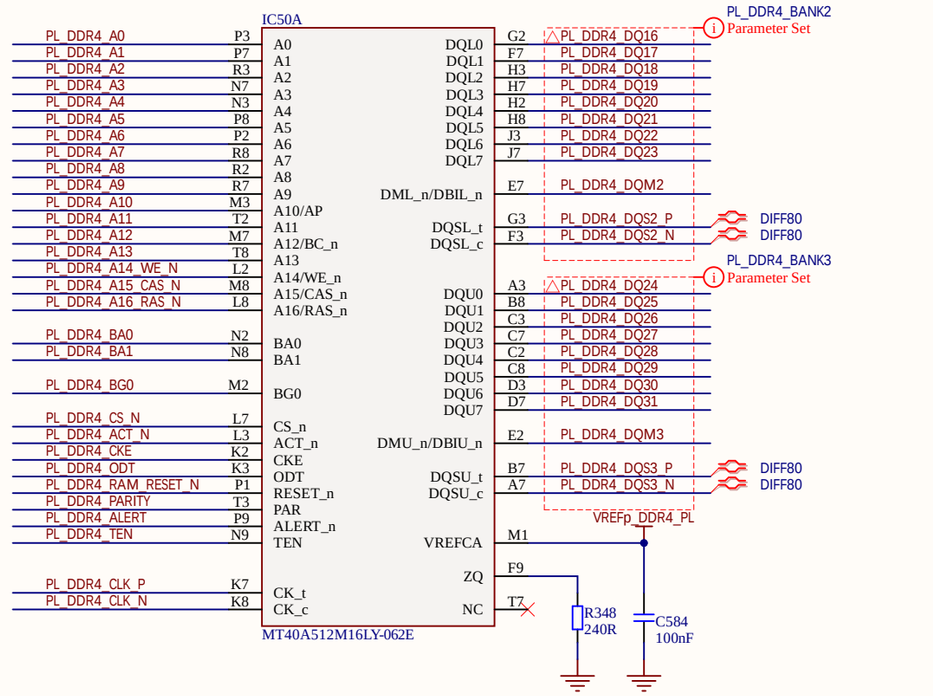


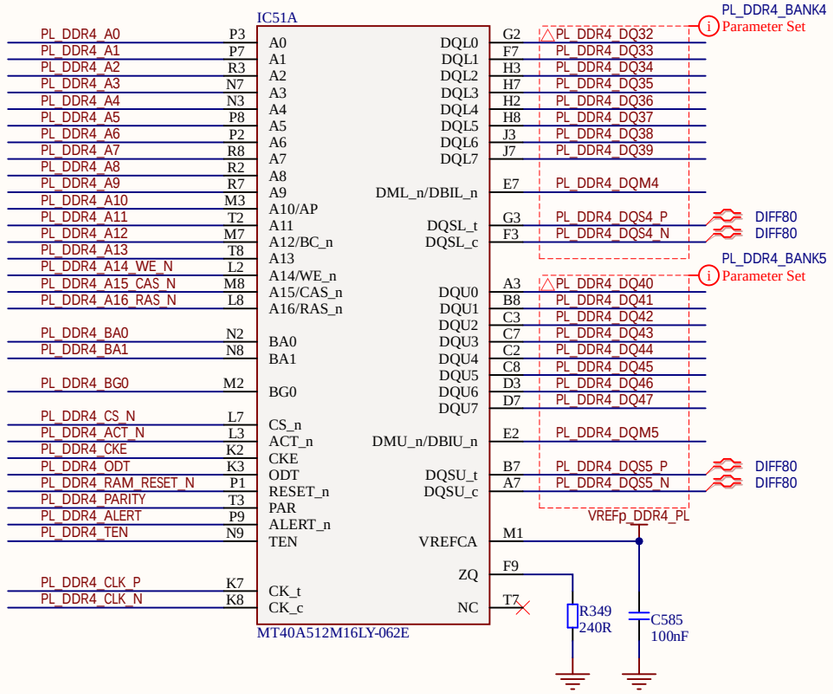


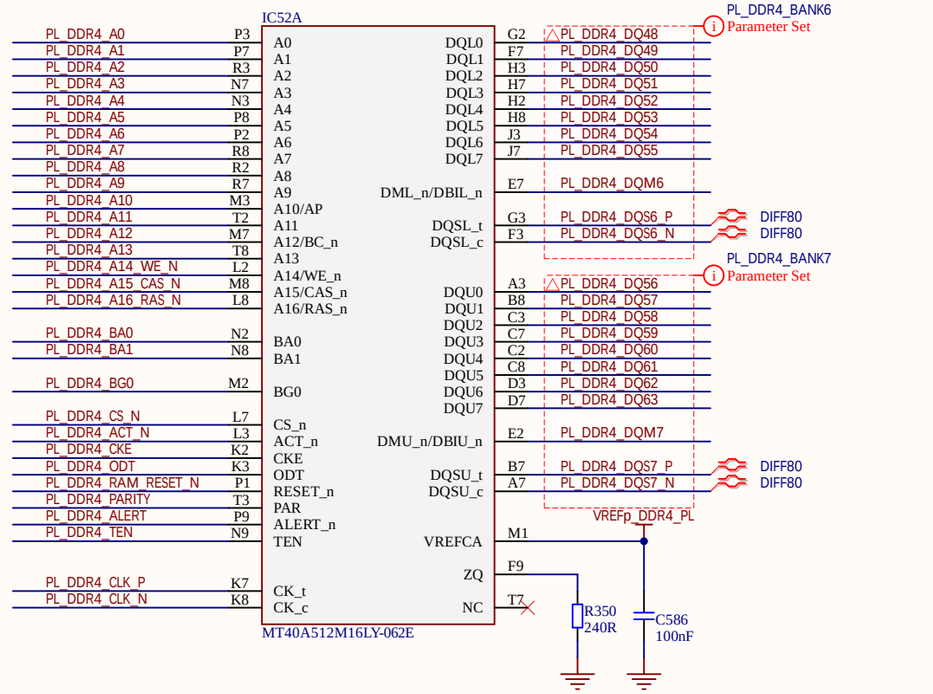
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [33] - DDR4 MEMORY PS II.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 33 ***of*** 46	

DDR4 MEMORY PL I



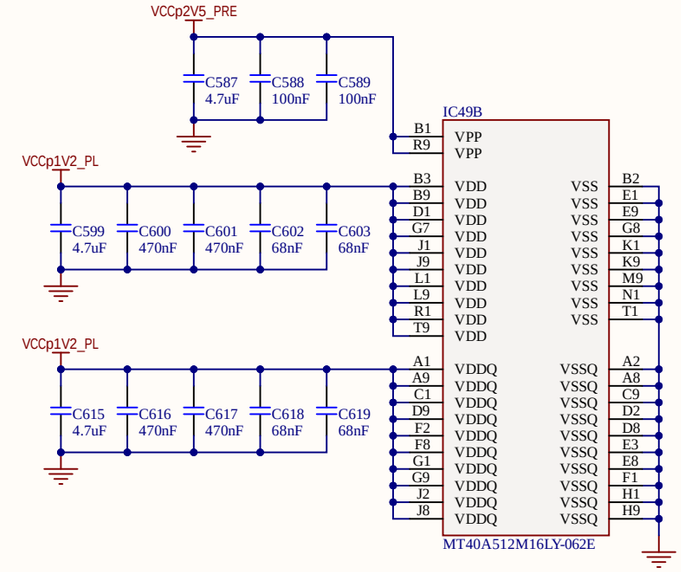


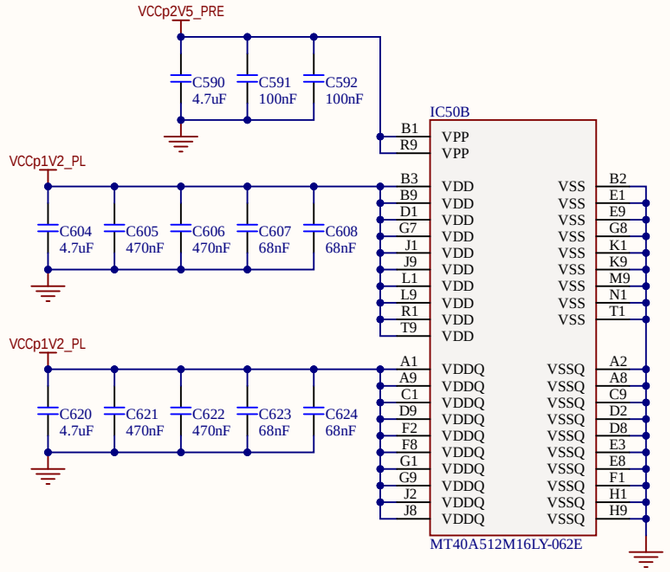


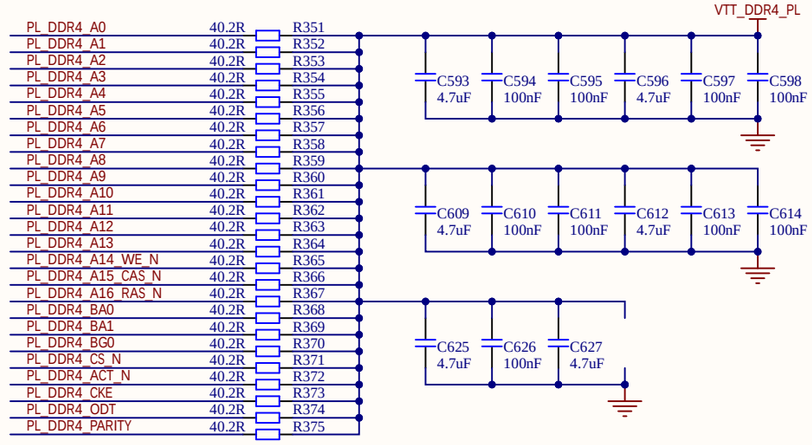


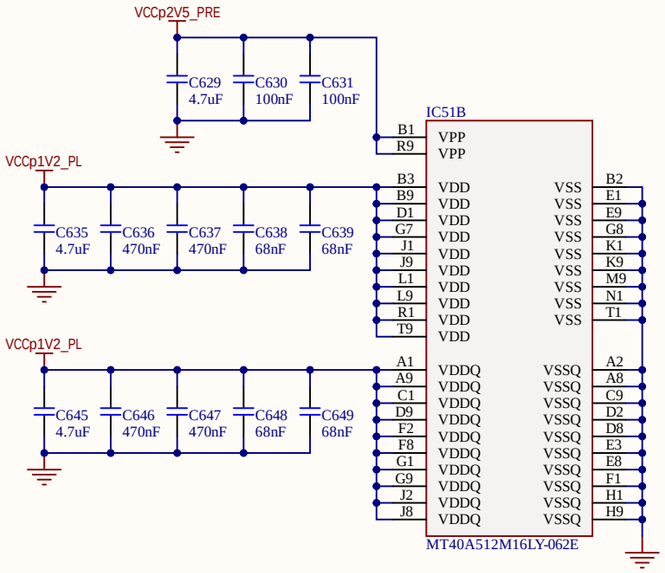
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [34] - DDR4 MEMORY PL I.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 34 ***of*** 46	

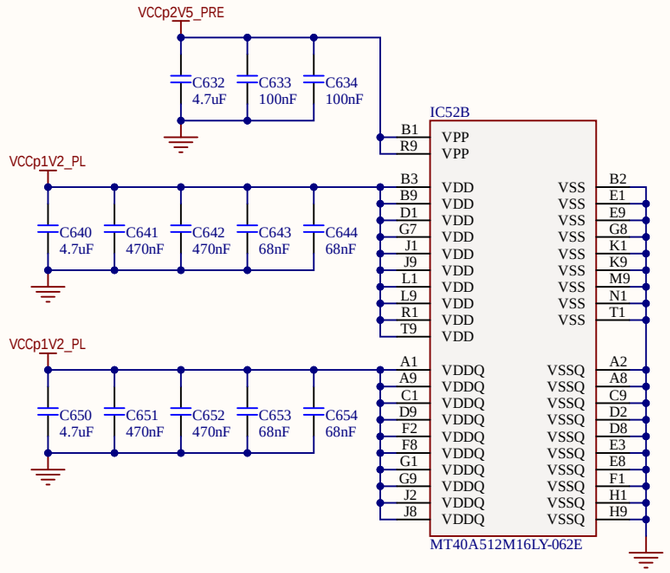
DDR4 MEMORY PL II

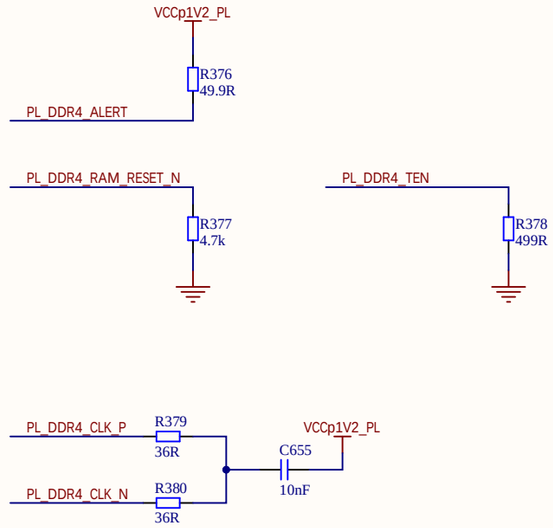








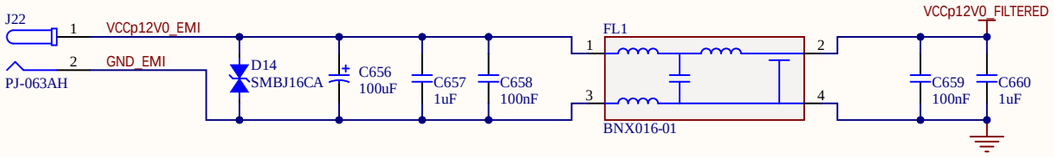




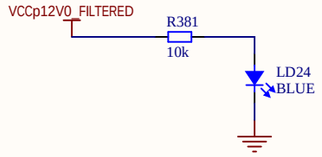
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [35} - DDR4 MEMORY PL II.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 35 ***of*** 46	

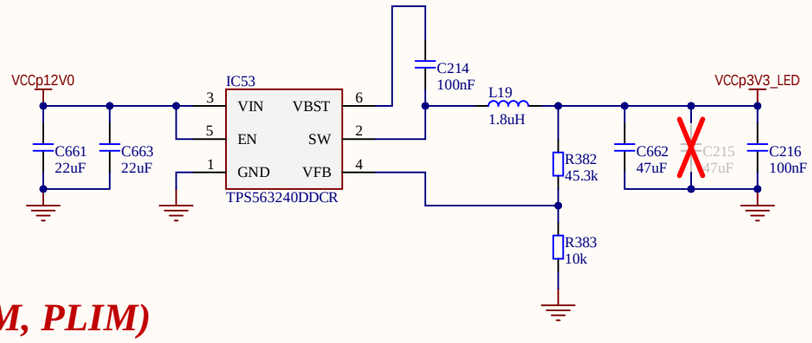
POWER INPUT AND FAN CONTROLLER

EMI Filter



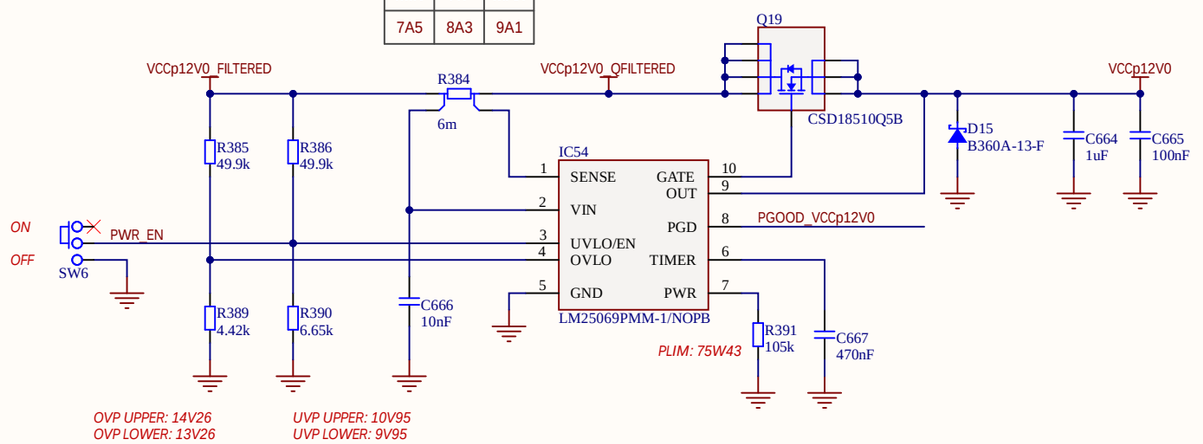
12V0 LED

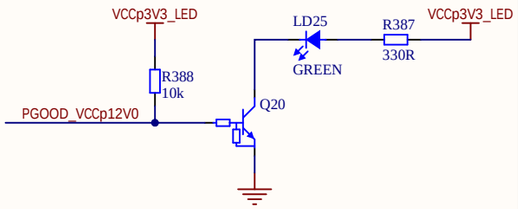


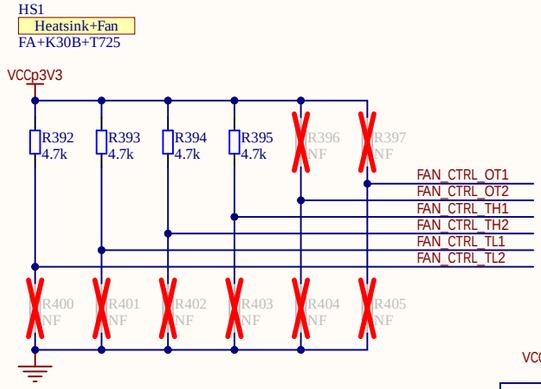


Input Protection (OVP, UVP, ILIM, PLIM)

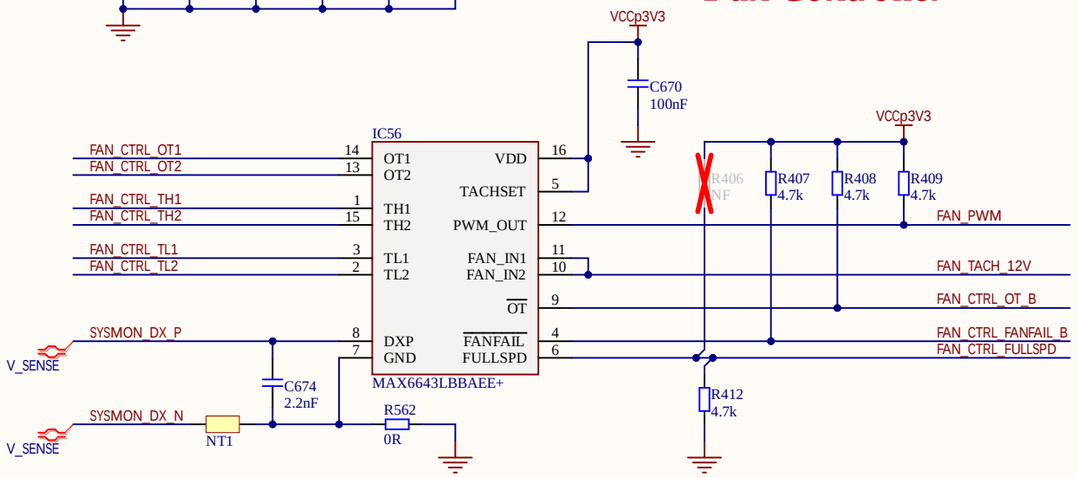
Current Limit		
MIN	TYP	MAX
7A5	8A3	9A1

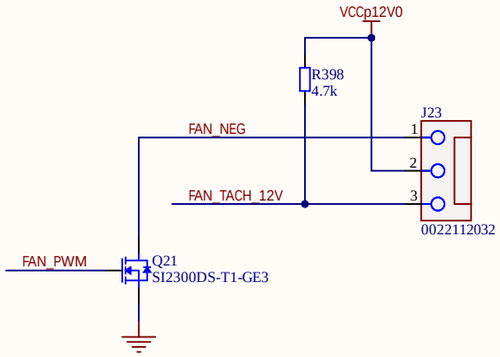


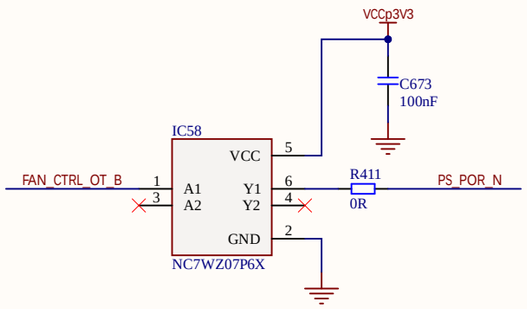


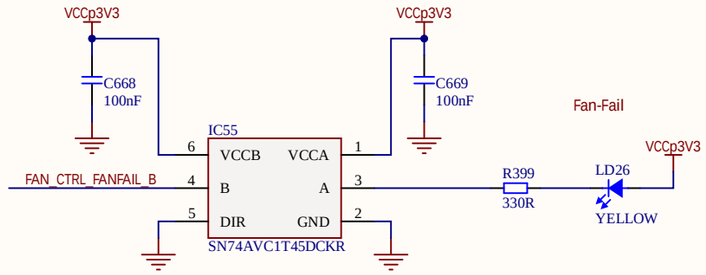


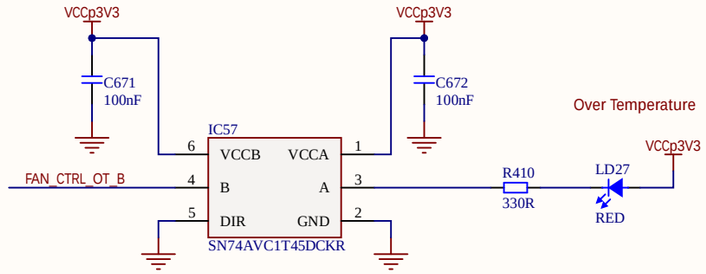
Fan Controller





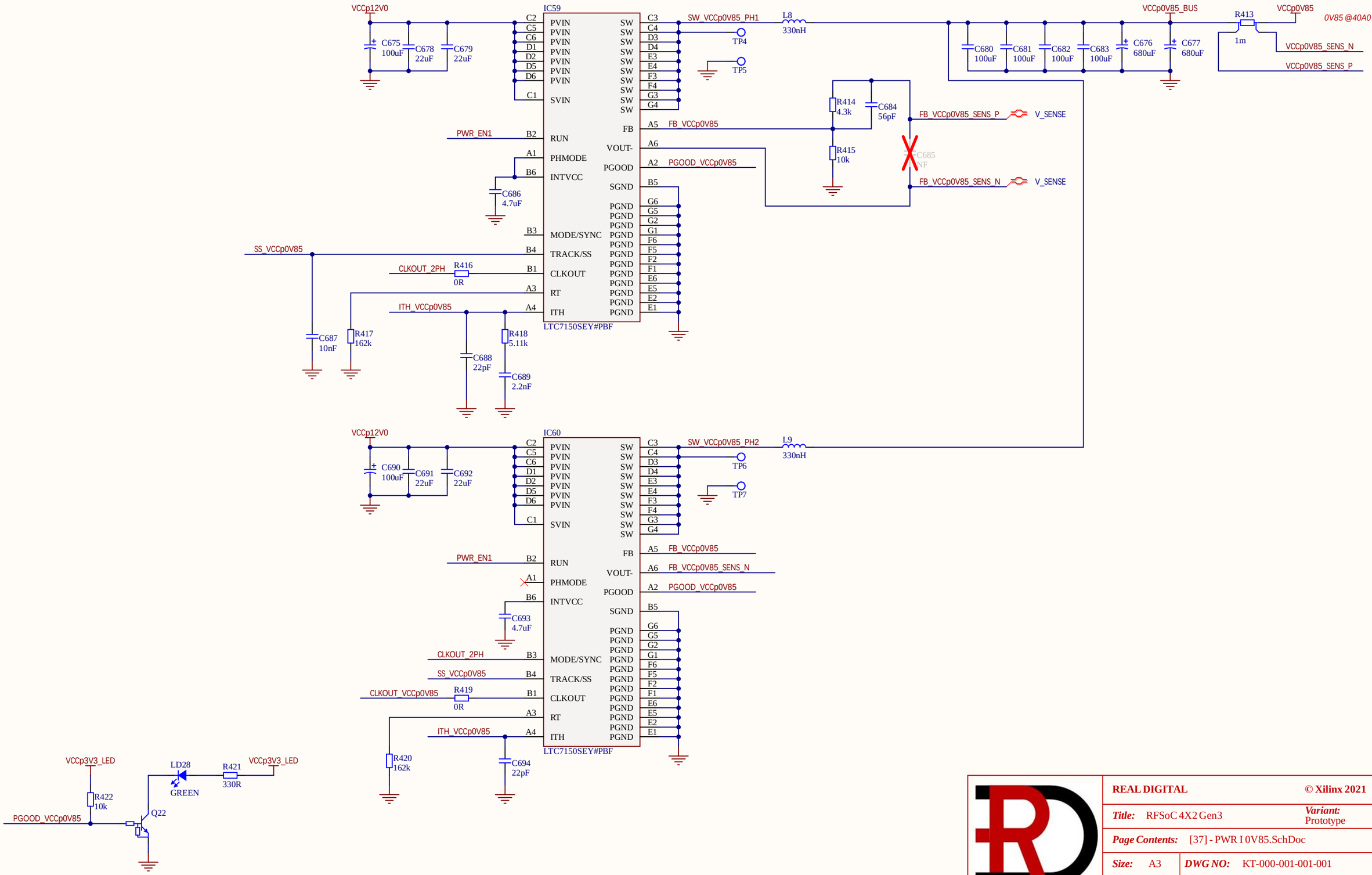






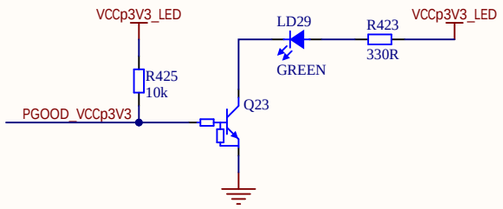
REAL DIGITAL			
Title: RFSoC 4X2 Gen3		Variant: Prototype	
Page Contents: [36] - PWR INPUT AND FAN CONTROLLER.SchDoc			
Size: A3	DWG NO: KT-000-001-001-001		Revison: V2I1
Date: 12/17/2021	Checked by: *	Sheet 36 of 46	

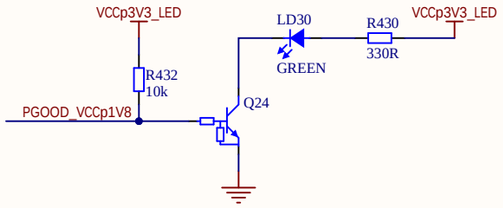
POWER I: VCCp0V85

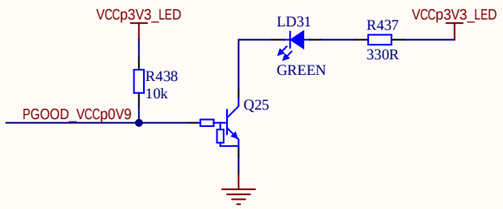


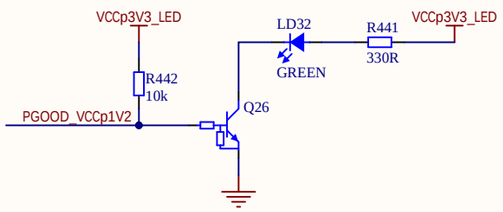
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [37] - PWR I 0V85.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 37 ***of*** 46	

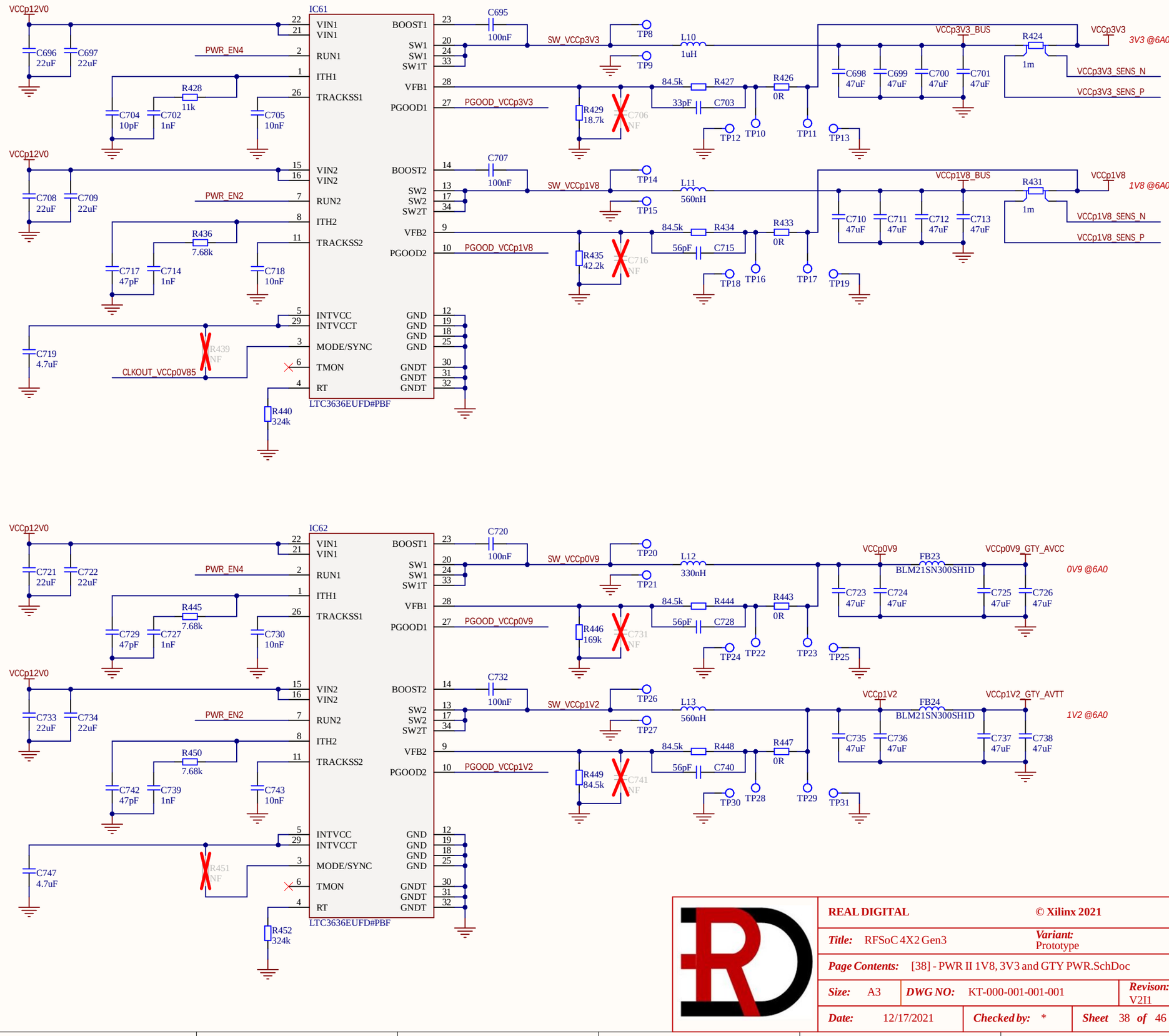
POWER II: VCCp1V8, VCCp3V3 and GTY PWR





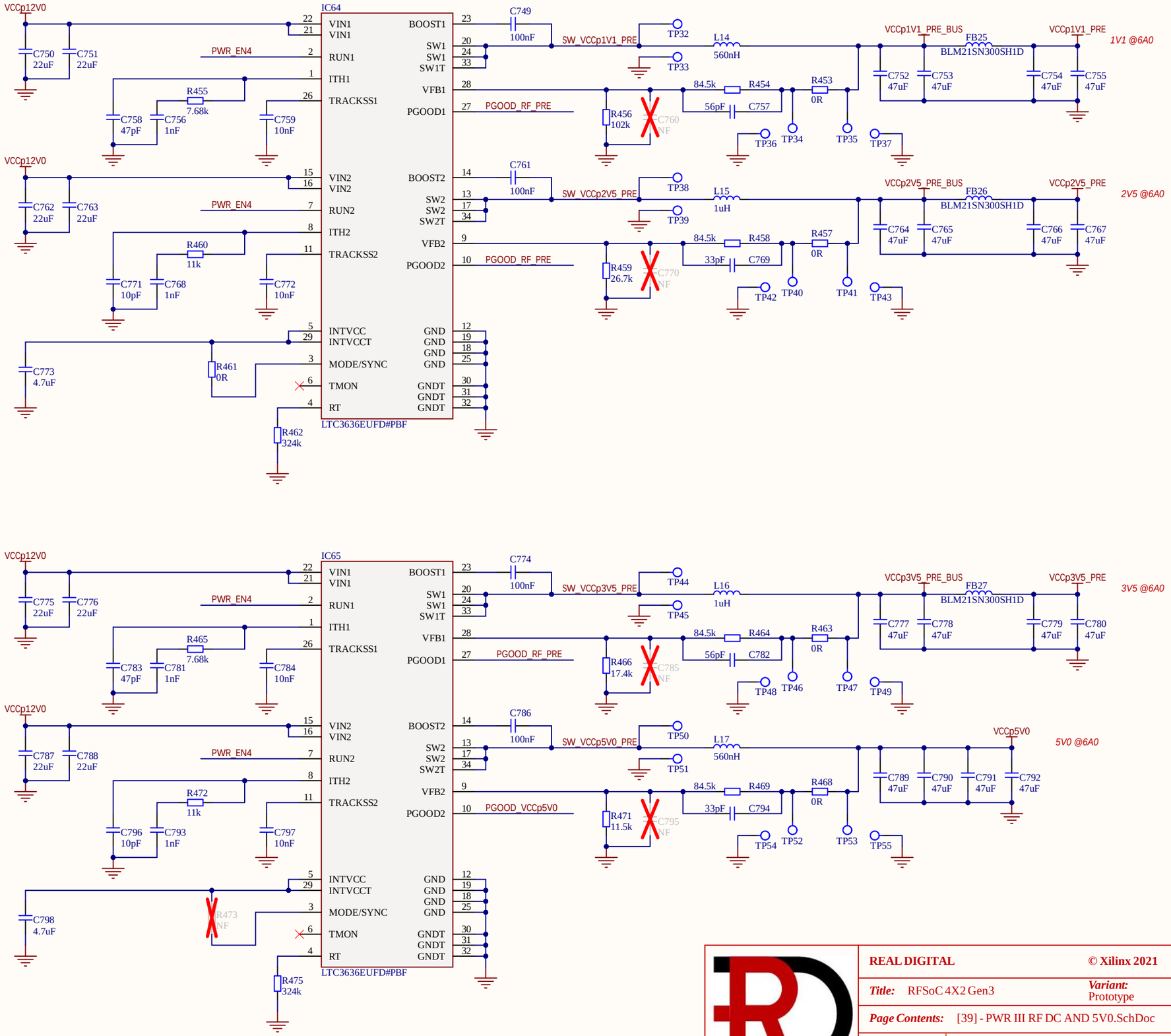






REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [38] - PWR II 1V8, 3V3 and GTY PWR.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 38 ***of*** 46	

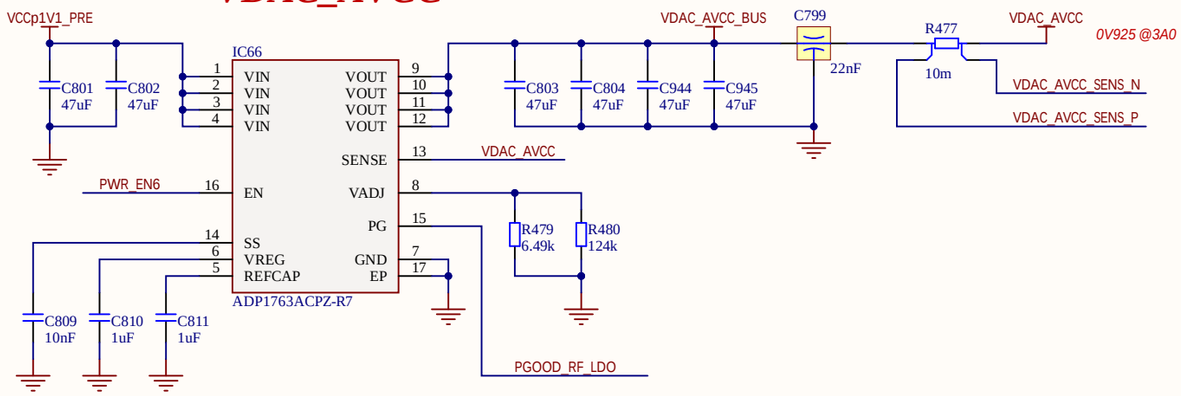
POWER III: RF DC/DC AND 5V0



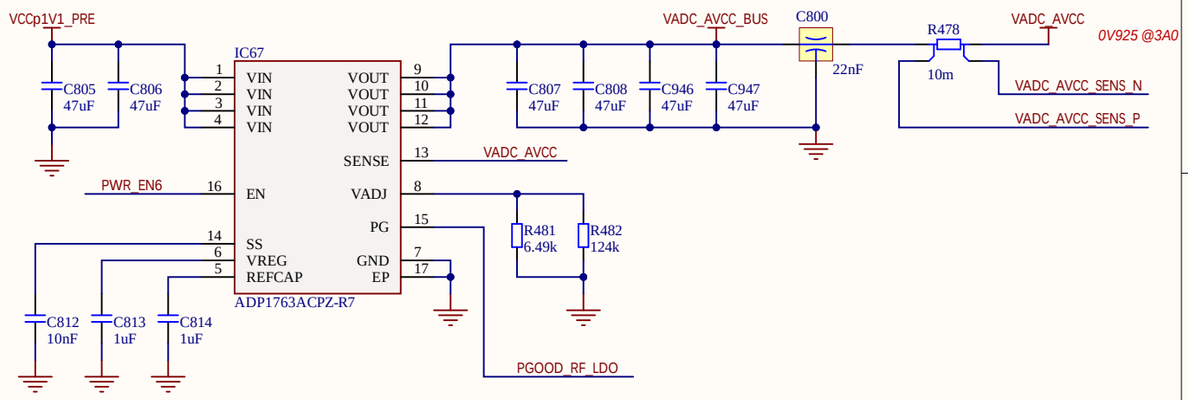
REAL DIGITAL	**© Xilinx 2021**
Title: RFSoC 4X2 Gen3	***Variant:*** Prototype
Page Contents: [39] - PWR III RF DC AND 5V0.SchDoc	
Size: A3	***DWG NO:*** KT-000-001-001-001 ***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** * ***Sheet*** 39 ***of*** 46

POWER IV: RF LDO

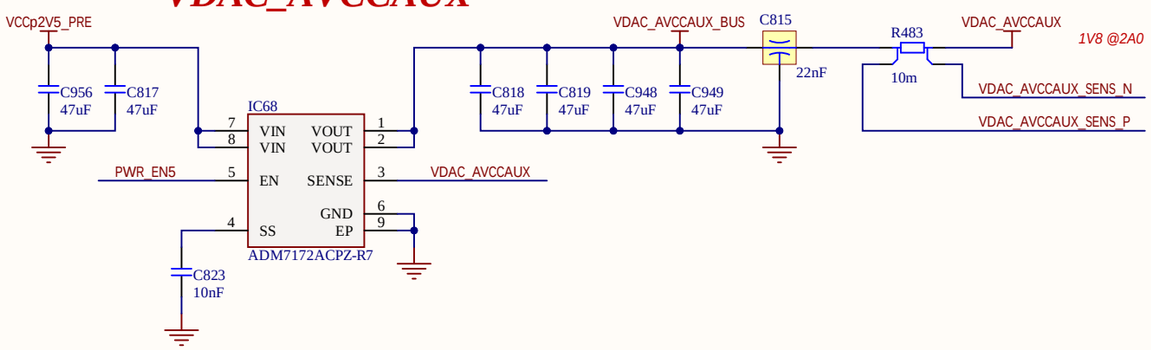
VDAC_AVCC



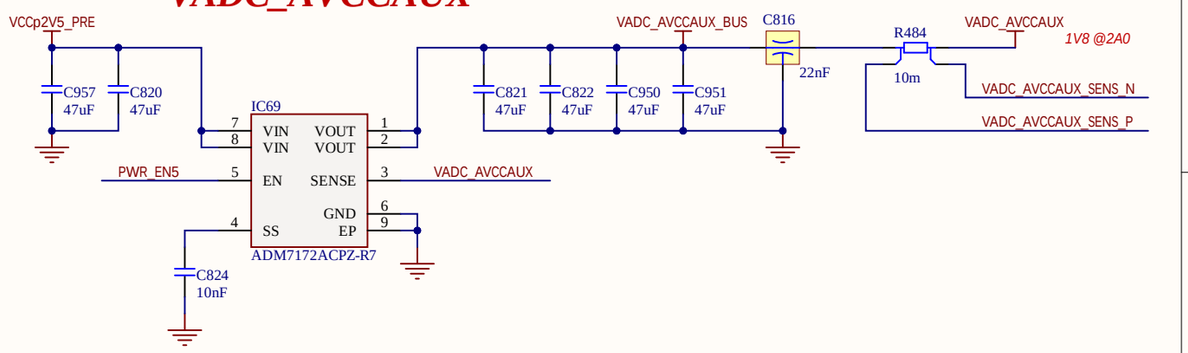
VADC_AVCC



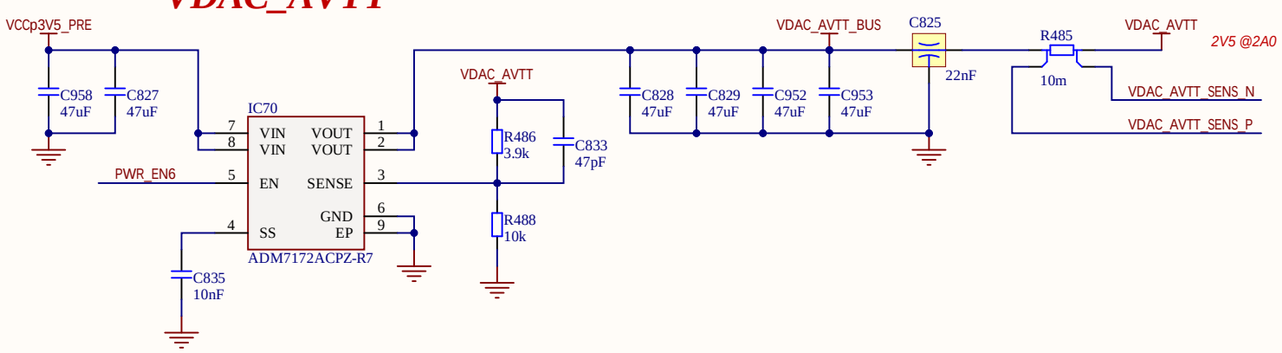
VDAC_AVCCAUX



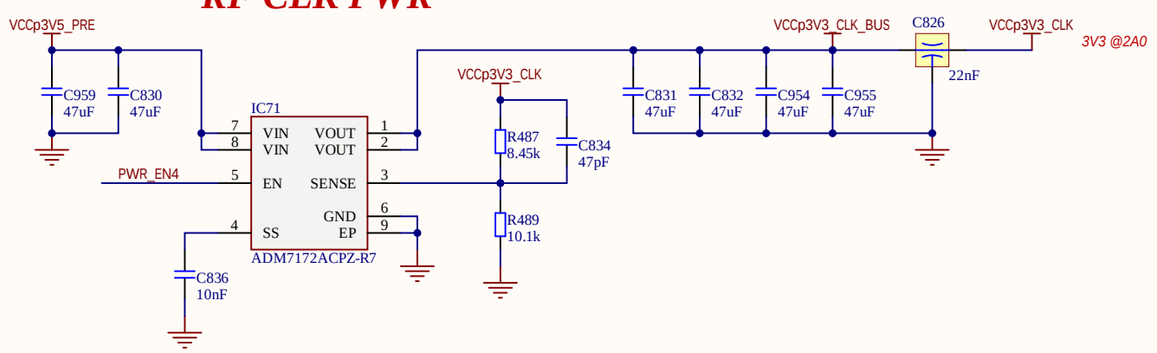
VADC_AVCCAUX

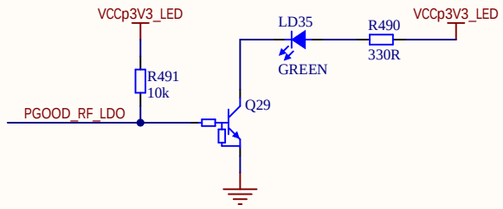


VDAC_AVTT



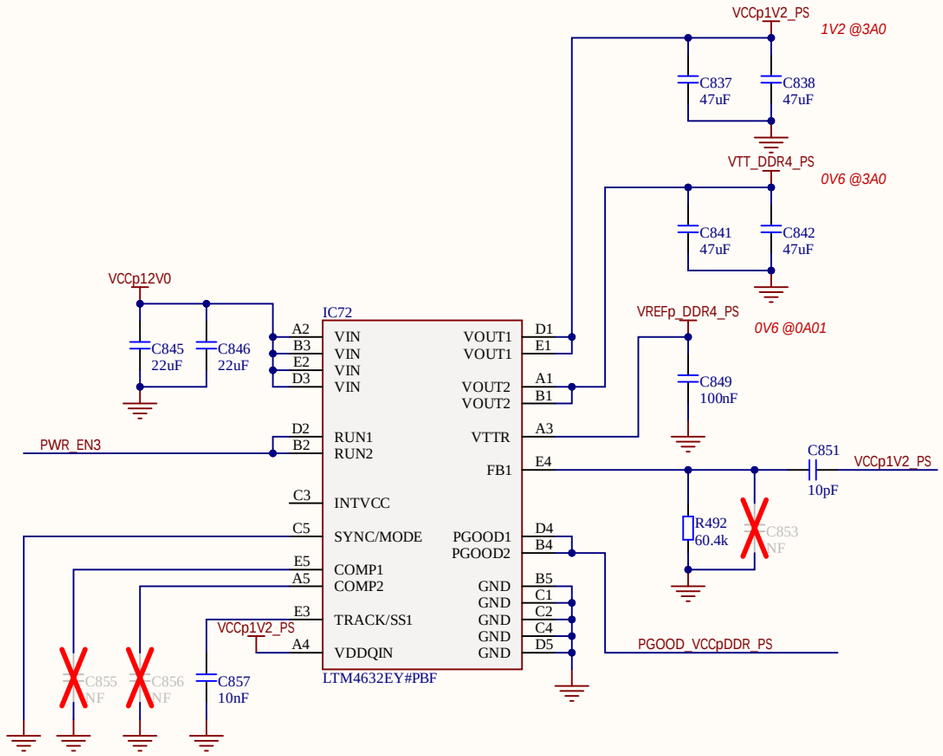
RF CLK PWR

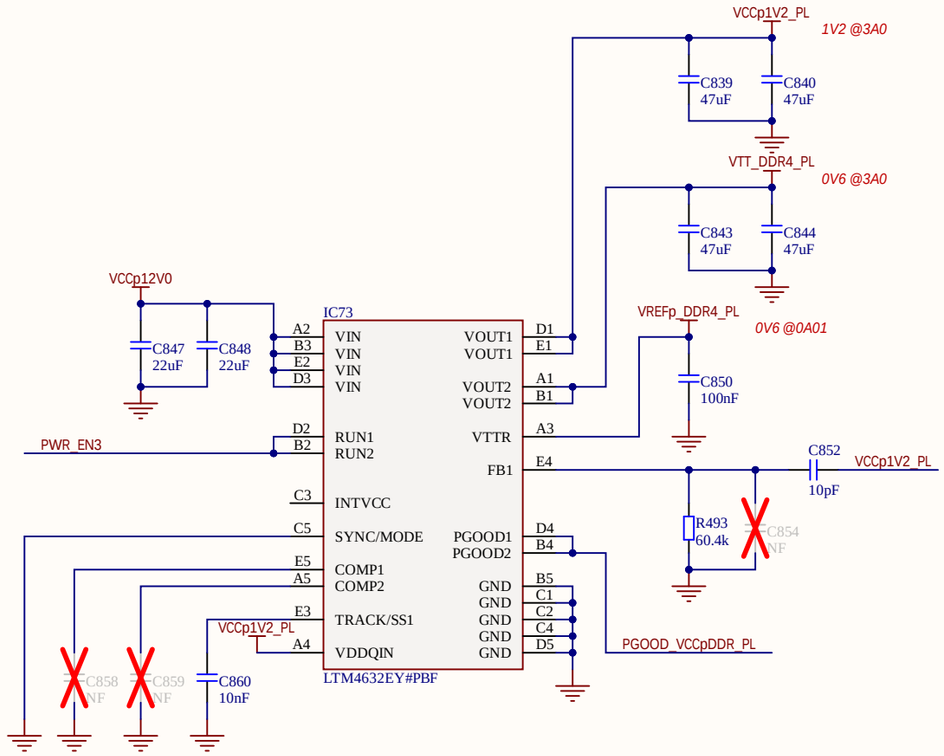


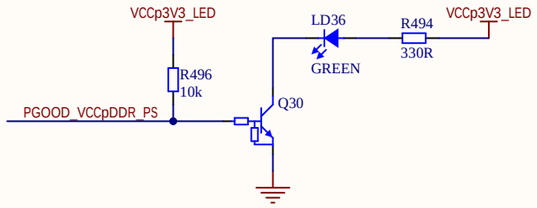


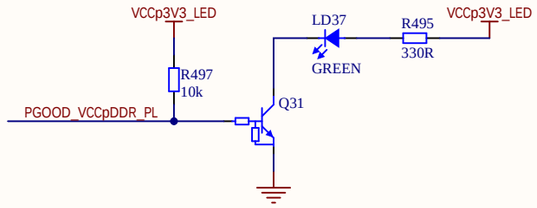
REAL DIGITAL		**© Xilinx 2021**	
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [40] - PWR IV RF LDO.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 40 ***of*** 46	

POWER V: DDR4



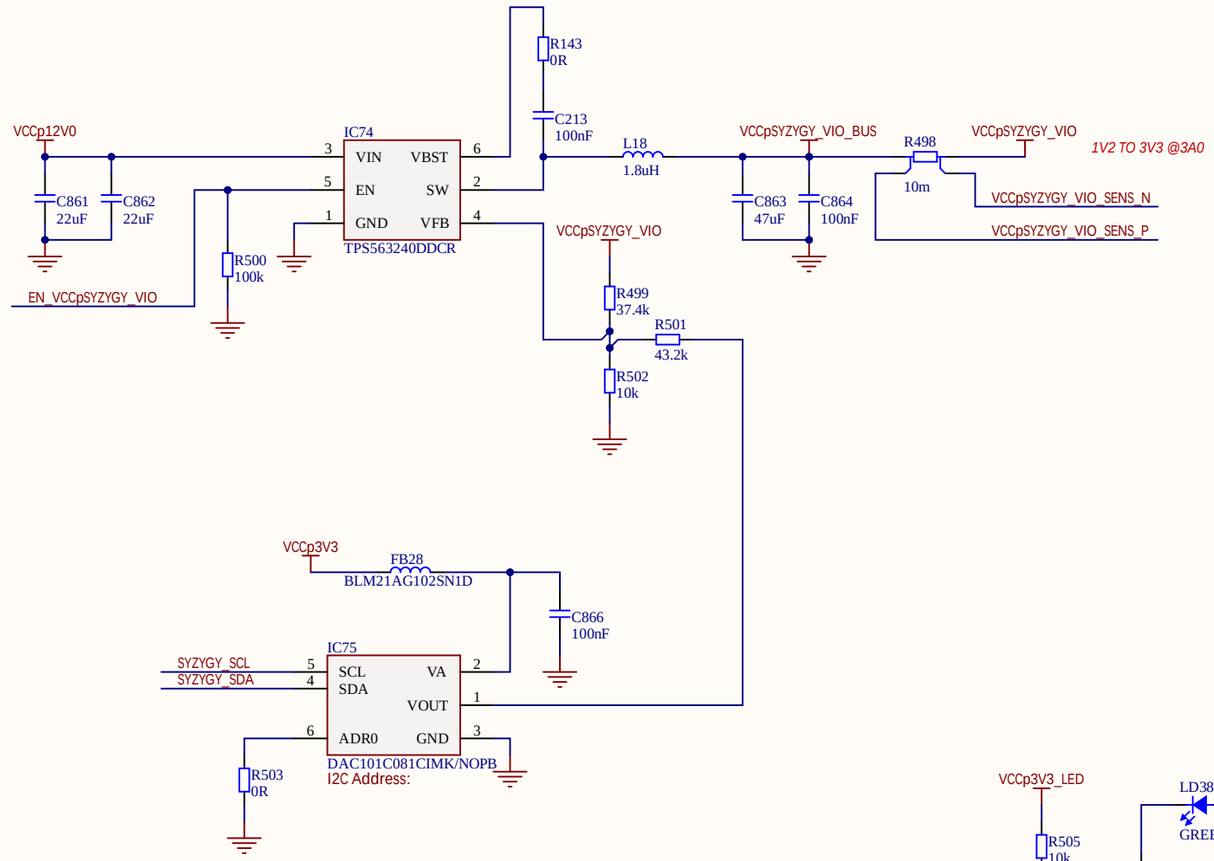






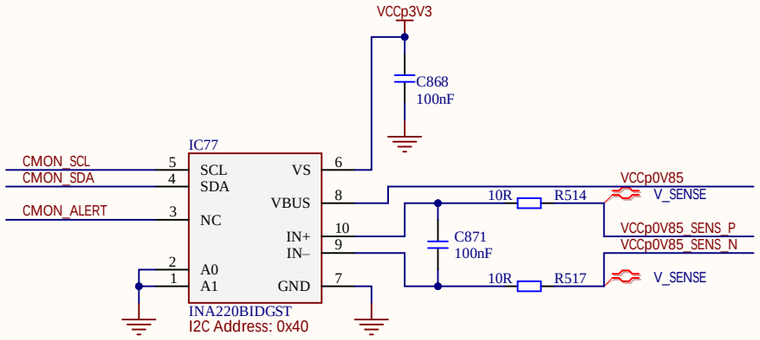
REAL DIGITAL			© Xilinx 2021
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [41] - PWR V DDR4.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 41 *of* 46	

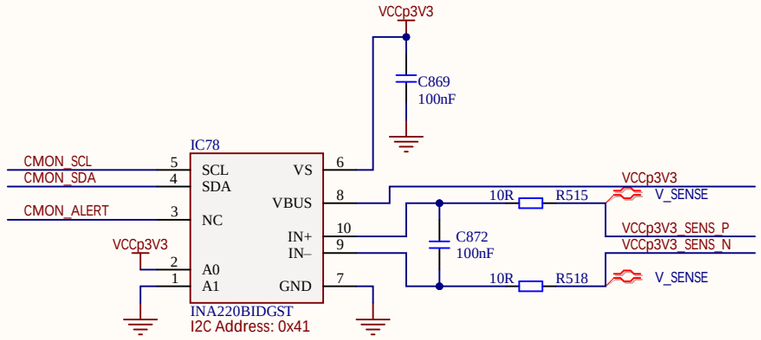
POWER VI: SYZYGY

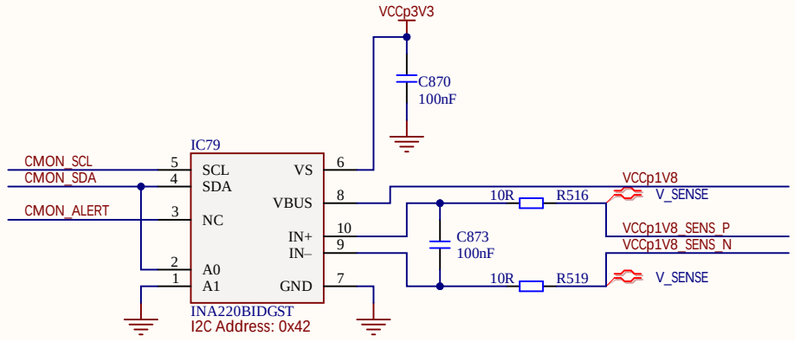


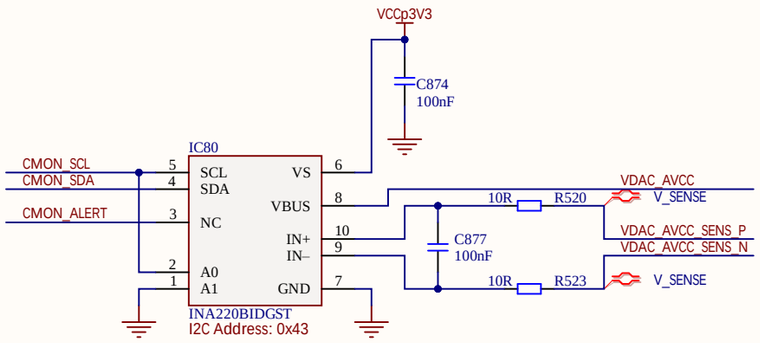
REAL DIGITAL			**© Xilinx 2021**
Title: RFSoC 4X2 Gen3		***Variant:*** Prototype	
Page Contents: [42] - PWR VII SYZYGY.SchDoc			
Size: A3	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 12/17/2021	***Checked by:*** *	***Sheet*** 42 ***of*** 46	

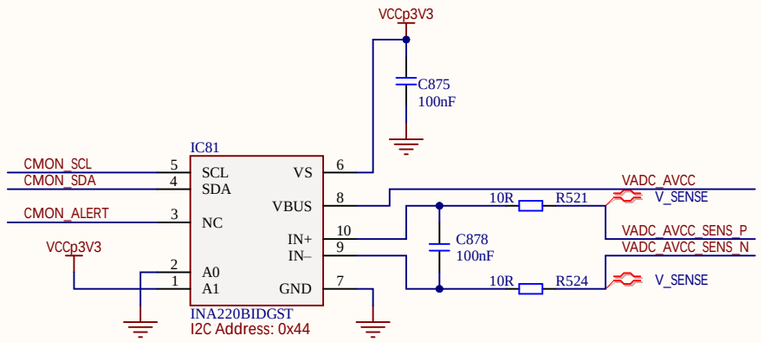
CURRENT MONITOR

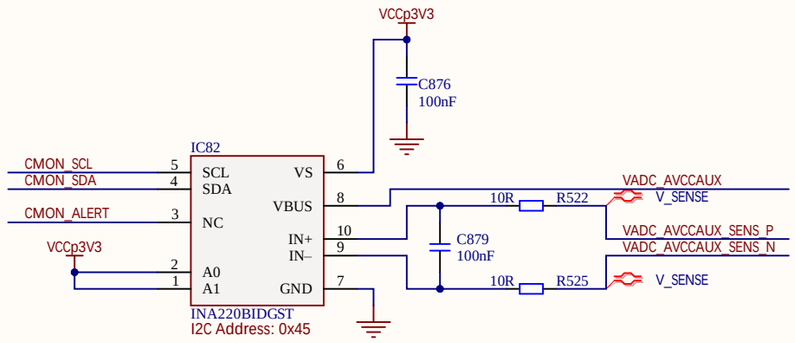


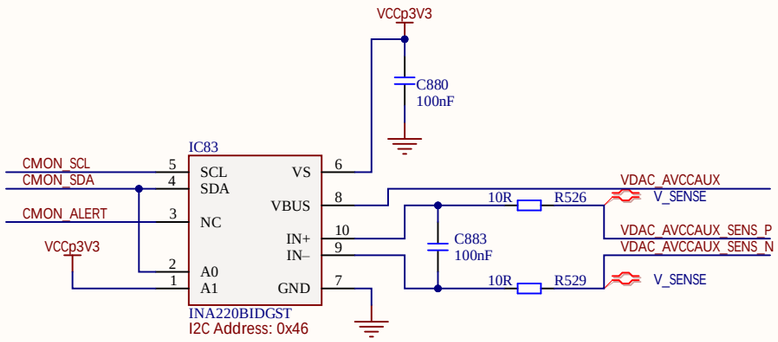


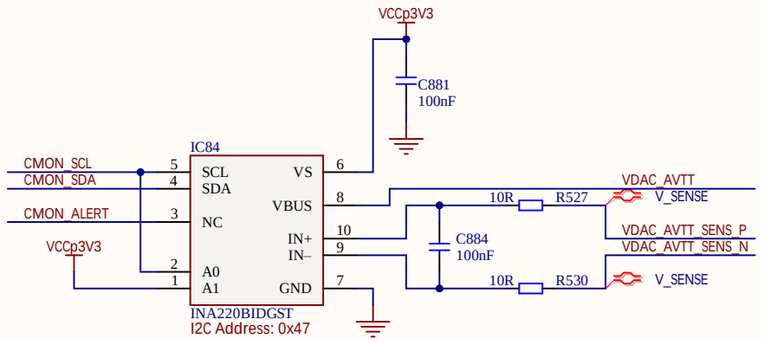


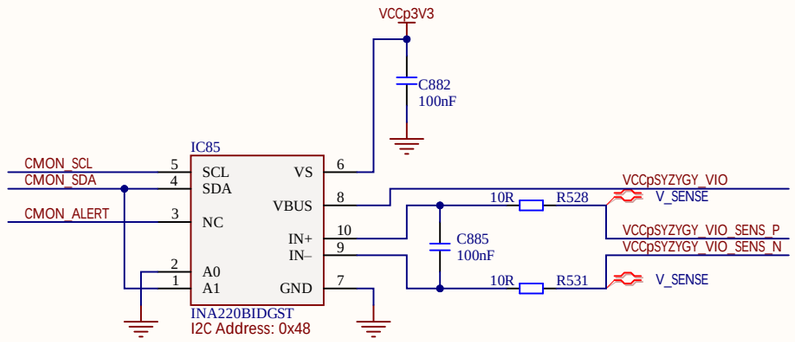


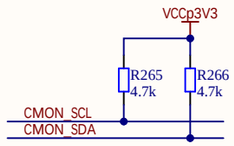






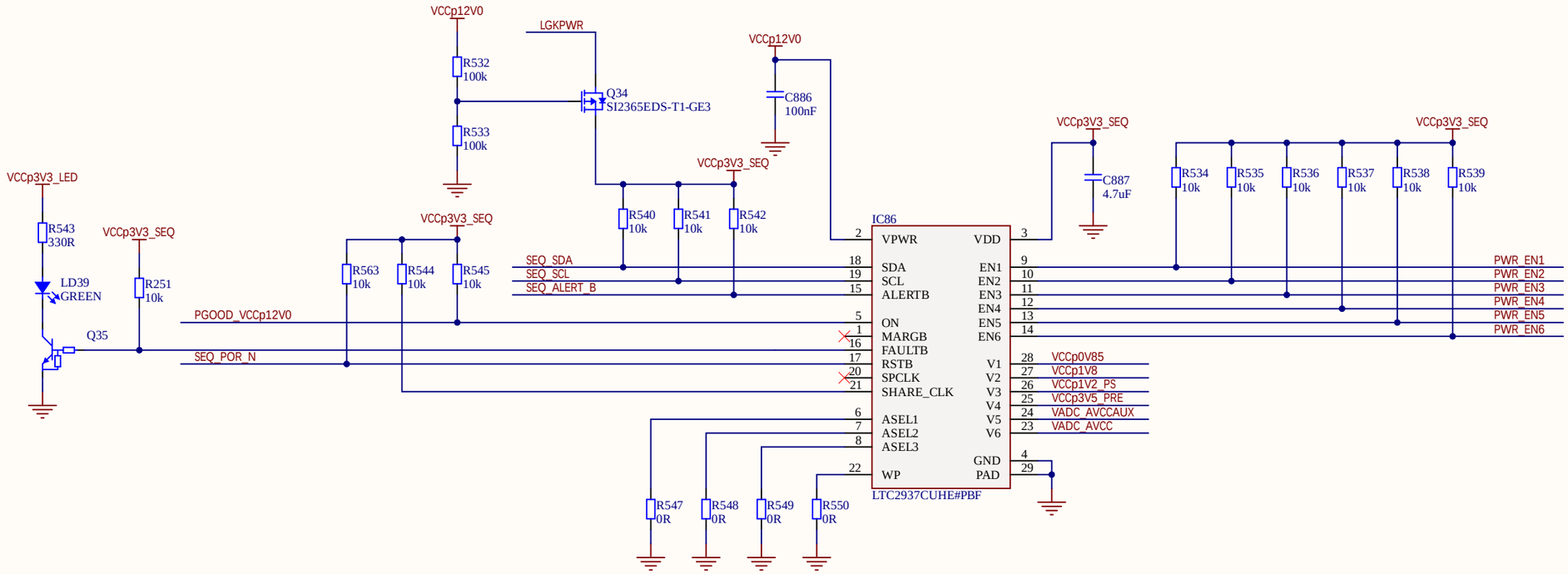


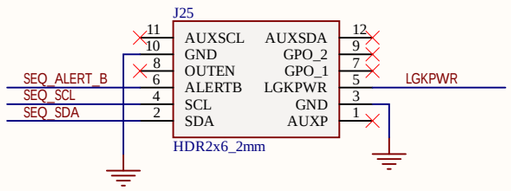




REAL DIGITAL		© Xilinx 2021	
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [43] - CURRENT MONITOR.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *		*Sheet* 43 *of* 46

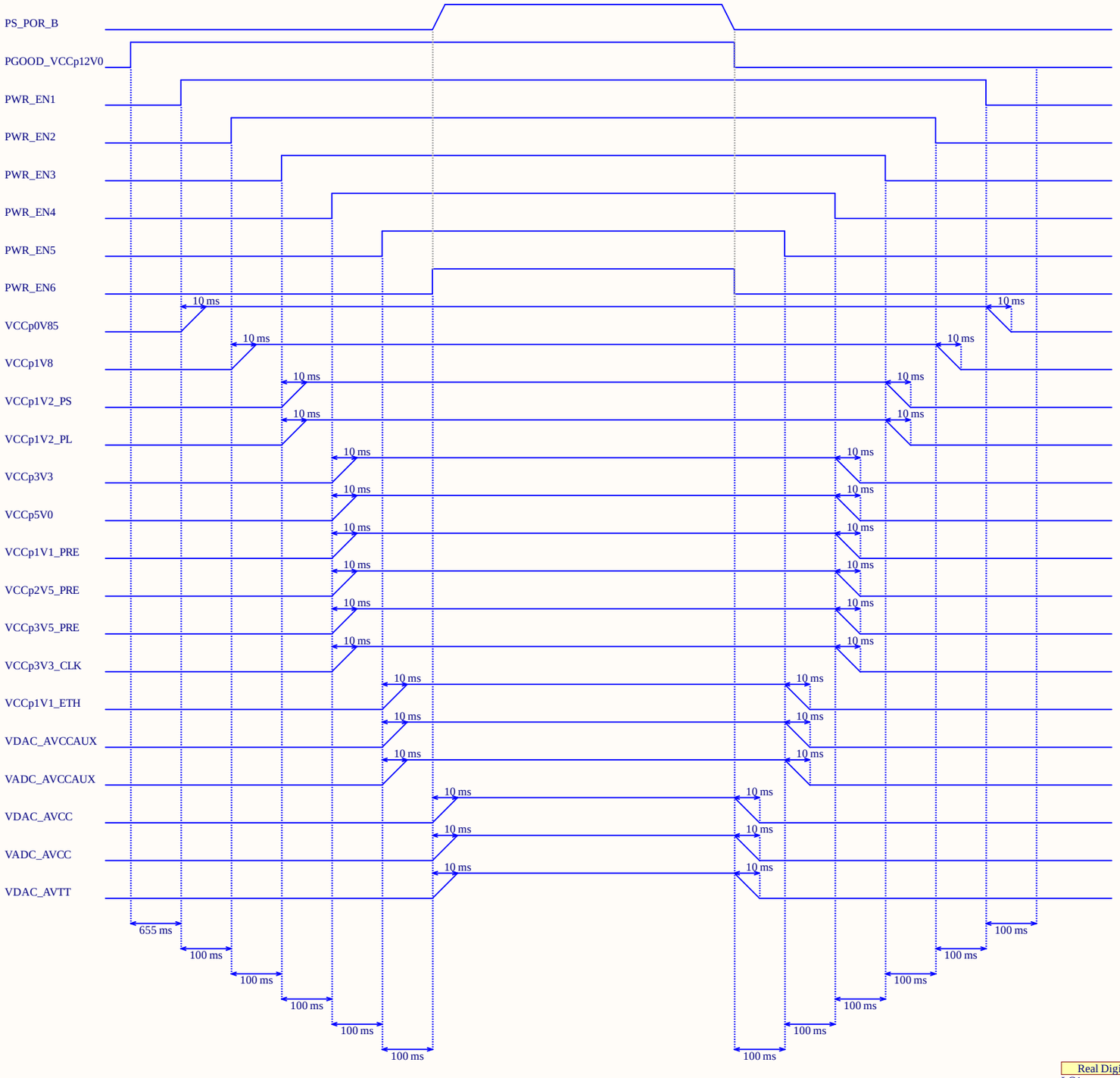
SEQUENCER





REAL DIGITAL		© Xilinx 2021	
Title: RFSoC 4X2 Gen3		*Variant:* Prototype	
Page Contents: [44] - SEQUENCER.SchDoc			
Size: A3	*DWG NO:* KT-000-001-001-001		*Revison:* V2I1
Date: 12/17/2021	*Checked by:* *	*Sheet* 44 *of* 46	

MECHANICAL AND POWER SEQUENCING



DAC SHIELD

CAN1
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

CAN2
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

VCXO SHIELD

SH1
RF Shield Shield
GND 1-Piece
26.3x19.8x8.1mm
MS263-20S

ADC SHIELD

CAN3
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

CAN4
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

CAN5
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

CAN6
RF Shield Shield
CAN
10.0x15.8x3.0mm
S03-15100300R

LMK SHIELD

SH3
GND
RF Shield Shield
FRAME: 36103205S
20.0x20.0x3.0mm
COVER: 36003200S
20.9x20.9x3.0mm
36103205S AND 36003200S

LMX SHIELD

SH4
GND
RF Shield Shield
FRAME: 36103205S
20.0x20.0x3.0mm
COVER: 36003200S
20.9x20.9x3.0mm
36103205S AND 36003200S

LMX SHIELD

SH5
GND
RF Shield Shield
FRAME: 36103205S
20.0x20.0x3.0mm
COVER: 36003200S
20.9x20.9x3.0mm
36103205S AND 36003200S

MH1 MH2 MH3 MH4
MH5 MH6 MH7

SC5 Screw, Phillips, M3, 6mm — M3, 6mm — STDF5 — Standoff, M3, L:5.0mm — 970050351
SC6 Screw, Phillips, M3, 6mm — M3, 6mm — STDF6 — Standoff, M3, L:5.0mm — 970050351
SC7 Screw, Phillips, M3, 6mm — M3, 6mm — STDF7 — Standoff, M3, L:5.0mm — 970050351
SC8 Screw, Phillips, M3, 6mm — M3, 6mm — STDF8 — Standoff, M3, L:5.0mm — 970050351
SC9 Screw, Phillips, M3, 6mm — M3, 6mm — STDF9 — Standoff, M3, L:5.0mm — 970050351
SC10 Screw, Phillips, M3, 6mm — M3, 6mm — STDF10 — Standoff, M3, L:5.0mm — 970050351
SC11 Screw, Phillips, M3, 6mm — M3, 6mm — STDF11 — Standoff, M3, L:5.0mm — 970050351

Real Digital — LG1
AMD Xilinx — LG2
PYNQ — LG3

REAL DIGITAL

Title: RFSoC 4X2 Gen3	*Variant:* Prototype	
Page Contents: [45] - MECH AND PWR SEQUENCING.SchDoc		
Size: A3	*DWG NO:* KT-000-001-001-001	*Revison:* V2I1
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DOC: REVISION HISTORY

Schematic:

1. Update Title Block: “CONFIDENTIAL Do not distribute” and “CR 2021 REAL DIGITAL” from all schematic pages
2. Update Cover Page (Sheet 1)
3. Update Block Diagram (Sheet 2)
4. Update Power Diagram (Sheet 3)
5. Remove design notes (Sheet 4, Sheet 18, and Sheet 28)
6. Update POWER SEQUENCING diagram (Sheet 45)

Schematic and PCB

1. Swap MIO33_UA1_RXD and MIO32_UA1_TXD (Sheet 20)
2. Change Sheet 12 name from “SD CARD” to “SD CARD AND EEPROM”. Add the EEPROM memory AT24MAC402-MAHM-T connected to the Syzygy I2C bus.
3. Change the status for the resistors connected to SPI_CLK/SMCLK (38) and SPI_DO/SMDAT (39) to “No Load” (Sheet 9, USB5742/2G).
4. Change the status for the capacitors connected to VCM01_224 (AL5), VCM23_224 (AL4), VCM01_226 (AJ5), and VCM23_226 (AJ4) to “NoLoad” (Sheet 27).
5. Rename the net between the power supply sequencer IC86.17 and the OLED display DISP1.8 to be SEQ_POR_N and add a pull-up resistor (10k) to Vccp3v3_SEQ on SEQ_POR_N (Sheet 44).
6. Connect SEQ_POR_N to NVT2008BQ level shifter pin B6 and connect PS_POR_N to NVT2008BQ level shifter pin A6 (Sheet 14).
7. Change the status for the pull-up resistor connected to PS_POR_N to “Load” (Sheet 19).
8. Change DDR4 memory part number from "MT40A512M16JY-083E" to "MT40A512M16LY-062E".
10. Add the AC decoupling capacitors for the RF clocks.
11. Remove the 3dB attenuator for the external input reference clock.
12. Increase the output capacitance for the LDOs (Sheet 40).
13. Silkscreen changes:
    - Remove the QR Code;
    - Change the Xilinx logo to be AMD_Xilinx;
    - Add PYNQ logo;
    - Change "USD DEVICE" to "USB DEVICE";
    - Add labels for the programming headers: JTAG, SI5395 PROG, SEQ PROG, CLK PROG
    - Change DAC0, DAC1, ADC0, ADC1, etc. to DAC_A, DAC_B, ADC_A, ADC_B, etc.
14. Add 200k pull-up resistors connected for the NVT2008BQ "EN" pin, update "VREFB" connection, and add pull-ups on the B side of the level translators. (Sheet 05 - 3 ICs, Sheet 10 - 1 IC, Sheet 14 - 1 IC)
15. Increase the input capacitance for the ADM7172ACPZ-R7 LDOs (Sheet 40).
16. Update the USB3.0 Slave connector schematic symbol and footprint (Sheet 8).
17. Increased the value of the resistors to reduce the brightness of the white and RGB user LEDs
    - Change R2, R3, R4, and R5 resistors values from 330R to 1k
    - Change R16, R20, R24, and R26 resistors values from 86R6 to 270R
    - Change R16, R20, R24, and R26 resistors values from 150R to 470R

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