AUP-ZU3 Reference Manual

Revision: A1

Overview

The AUP-ZU3 is a high-performance embedded computing platform built around AMD's Zynq UltraScale+ MPSoC "ZU3EG" device. This advanced system-on-chip combines a powerful multicore Arm® processing system (PS) with a rich set of peripherals and high-speed interfaces, all tightly integrated with ASIC-class programmable logic (PL) fabric.

The ZU3's programmable logic fabric enables high-speed, low-latency, and fully customizable hardware acceleration for compute-intensive tasks such as graphics rendering, video processing, and AI workloads. Developers can implement custom IP blocks to create specialized compute engines like Deep Learning Processing Units (DPUs), hardware co-processors, or custom memory hierarchies, unlocking capabilities and enabling powerful new designs that are simply not possible with fixed-function processor architectures.

With over 6,000 high-bandwidth interconnects between the PS and PL, the ZU3's architecture ensures seamless, high-speed communication that far outperforms traditional multichip solutions.

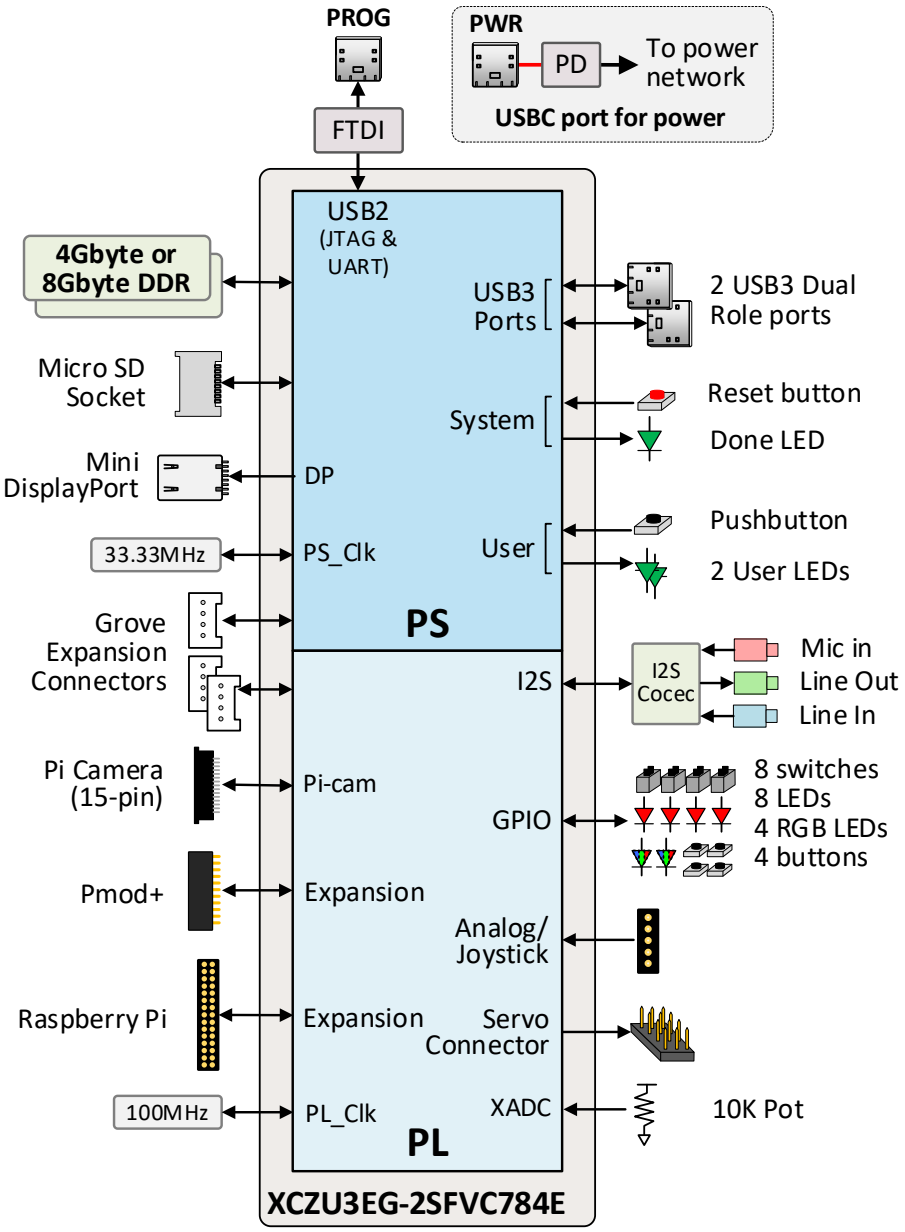

Figure 1: AUP-ZU3 Block Diagram

The AUP-ZU3 board features four or eight gigabytes of high-speed DDR memory, onboard ROM, audio and video interfaces, general-purpose I/O, and multiple expansion connectors compatible with Raspberry Pi, PMOD, Grove, and standard camera modules. This makes it a versatile solution for rapid prototyping and embedded system development across a wide range of applications.

The board supports AMD-Xilinx's Vitis and Vivado toolchains, along with the Python-based PYNQ framework, offering flexibility for both software and hardware development. Programming can be done directly via USB 2.0 or through SD card boot, giving developers a convenient and adaptable workflow.

PYNQ

PYNQ (Python Productivity for Zynq) is an open-source framework that streamlines the development process on AMD-Xilinx platforms by providing a high-level, Python-based interface for interacting with programmable logic. Built on Jupyter notebooks, PYNQ allows developers to load hardware overlays and control custom logic without the need for traditional, hardware-centric design tools.

By abstracting the complexity of hardware design, PYNQ makes it easier for software developers, data scientists, and system engineers to leverage the power of hardware acceleration in their applications. This greatly expands access to custom hardware capabilities, enabling rapid prototyping and development in a more familiar software environment.

When combined with high-performance platforms like AMD's MPSoC, PYNQ unlocks advanced visualization and signal analysis capabilities - making it a powerful tool for many compute-intensive applications and real-time data processing.

XCZU3 MPSoC and AUP-ZU3 board Major Features

The MPSoC board is centered around the ZYNQ UltraScale+ XCZU3EQ device in the SFVC784 package. The XCZU3EQ includes:

- A 64-bit quad-core ARM Cortex-A53 and a 32-bit dual-core ARM Cortex-R5F
- Large on-chip cache memories for each core
- A tightly coupled and large programmable logic array with 154K logic cells and 360 DSP slices
- An ARM Mali-400 based GPU and NEON advanced SIMD media processing engine
- A single and/or double precision floating point unit
- 256Kbytes of PS RAM, and a combined 9.4Mb of UltraRAM and distributed RAM
- Support for 32-bit, 3200MHz DDR4 with an 8-channel DMA controller
- Support for PCI Express, SATA, DisplayPort, Gbit Ethernet, USB3 and other common ports
- System Memory Management Unit

The ZU3 board surrounds the ZYNQ device with everything needed to build complex digital systems, including high-speed memories, highly stable power supplies, clean and fast clocks, and high-speed data offload. Major board features include:

- Multiple USB ports, including a USB2 port for UART/JTAG and two USB3 dual-role ports
- Up to 8GBtyes of 32-bit, 3200MTPS DDR4 connected to the Processing System (PS)
- Mini DisplayPort and I2S audio codec
- MicroSD card reader
- Raspberry PI, Grove, and Pmod+ expansion connectors
- GPIO devices including pushbuttons, slide switches, LEDs, RGB LEDs.

The figure below shows theZU3 board with callouts for major features and interfaces.

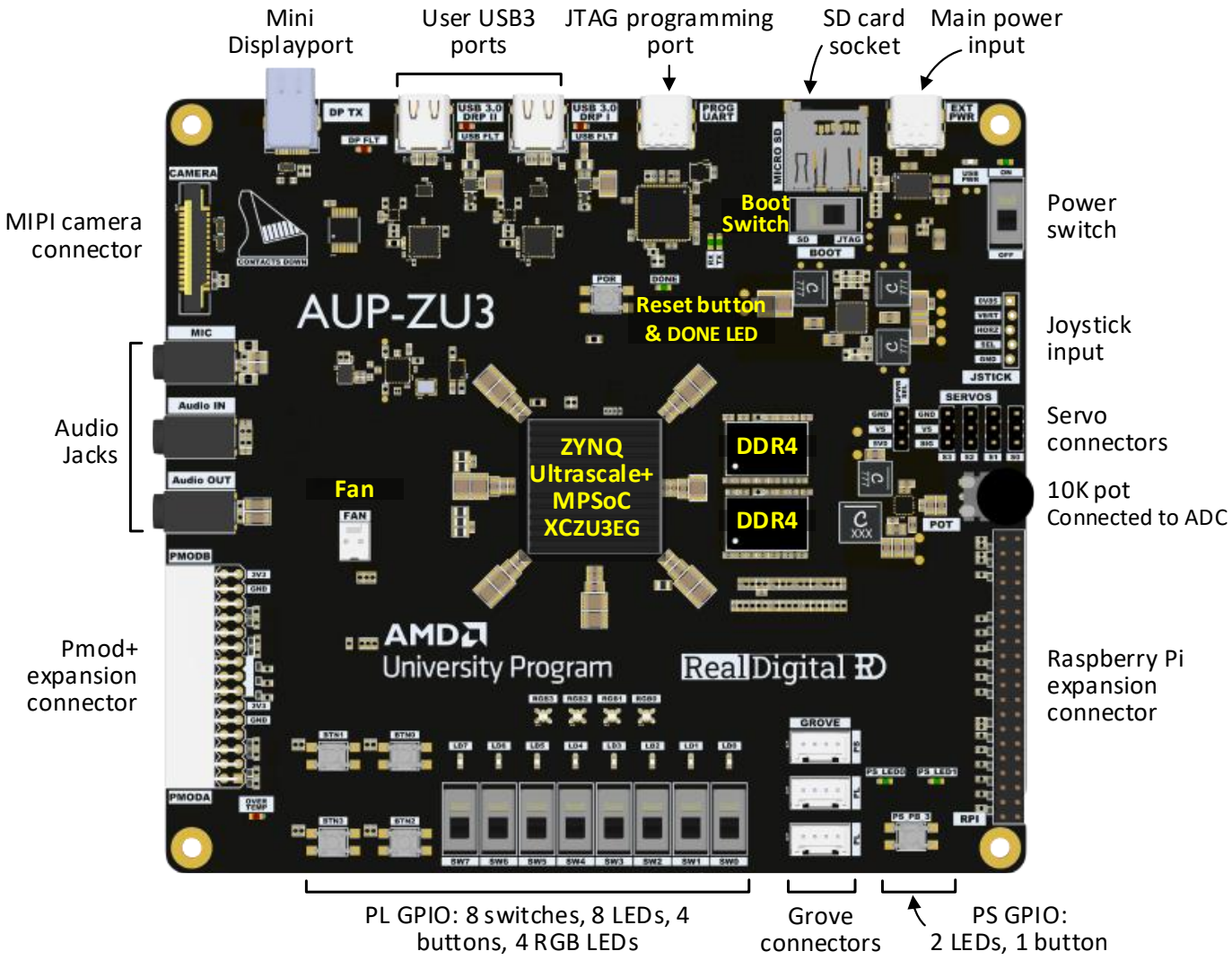

Figure 2: ZU3 Board Major Components

Programming

The ZU3 board features a USB2-based JTAG port for programming and debugging. This interface supports direct hardware configuration from within the Vivado design suite, and enables software development, execution, and debugging through the Vitis environment. An independent UART/COM port is also always available over this same USB2 connection.

Alternatively, the board can boot from a MicroSD card loaded with hardware and software configuration files produced by Vivado and Vitis. A BOOT mode switch located near the SD card slot selects between USB-JTAG and SD card boot modes. On power-up, if a properly formatted SD card is inserted, the ZU3 device will automatically load its configuration and programming files from the SD card. These files can be generated using AMD-Xilinx tools such as Vivado and Vitis, and written to an SD card using any of several freely available SD card writing programs.

The ZU3 board also supports the PYNQ framework. To use PYNQ, the board must be booted from a MicroSD card preloaded with a PYNQ image specific to the ZU3. Any branded 16GB or larger MicroSD card (with a minimum write speed of 10MB/s) can be used, and a compatible SD card is included with the optional ZU3 kit.

The latest PYNQ image from AMD can be downloaded from www.pynq.io and written to an SD card using any of several freely available SD card writing programs.

A system Reset button is available to restart the board and trigger a new configuration cycle. A status LED labeled “Done” will illuminate once configuration is complete.

Clocks

The ZU3 uses two primary clock sources: a 33.3333MHz oscillator that provides the primary clock source for the PS, and a 25MHz crystal that drives a TI CDCE6214 Clock Generator. The TI clock generator is factory programmed to produce five clock signals: two single-ended 24MHz clocks that drive the two on-board Microchip USB2 transceivers; a dual-ended 100MHz clock that provides the main PL clock source; and two dual-ended 100MHz clocks that drive the Gigabit transceiver (GTR) blocks that interface with the USB3 and DP blocks.

While the clock generator is in-system programmable, reconfiguration is not recommended for most users. However, it can be controlled via three GPIO pins (GPIO1, GPIO4, and HW_SW_CNTL) and an I²C interface, all routed from the PS. For detailed guidance on modifying clock settings, please refer to the **CDCE6214 datasheet** available on the Texas Instruments website.

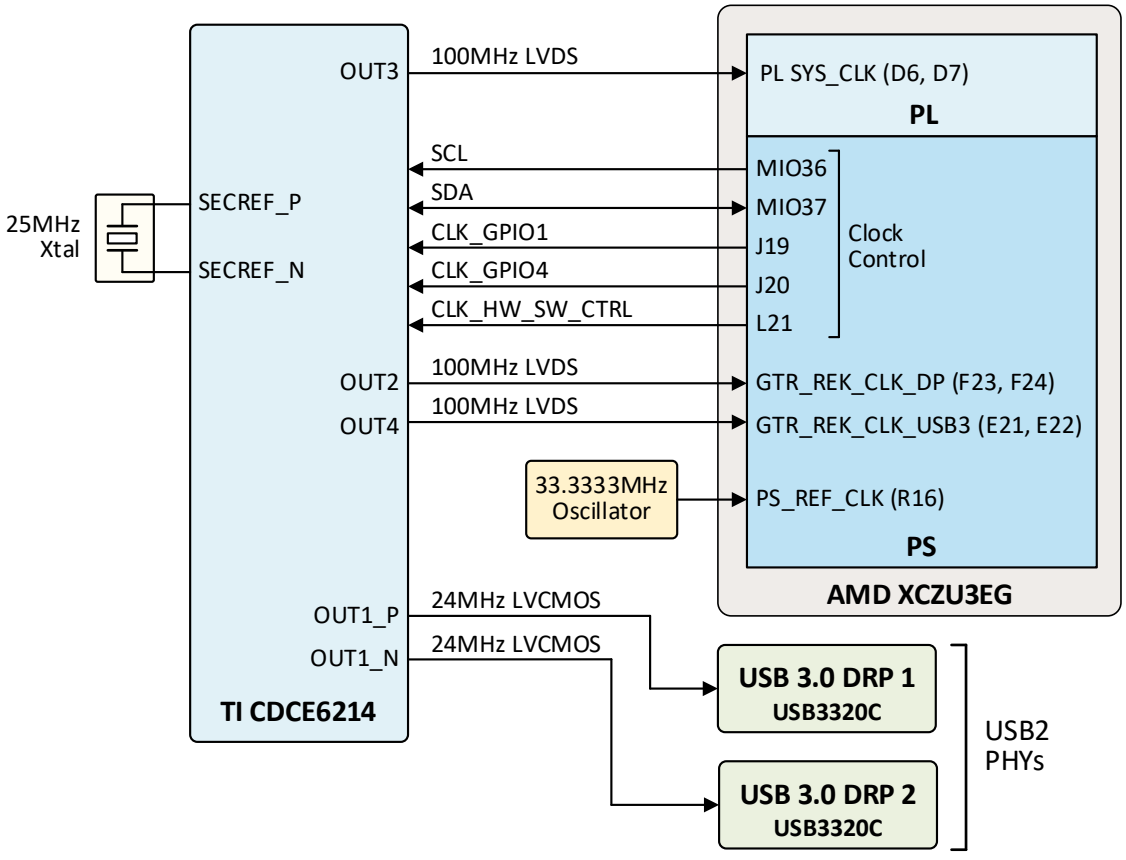

Figure 3: AUP-ZU3 Clocking Scheme

Power Supplies

The AUP-ZU3 board is powered via a USB-C adapter connected to the onboard USB-C port labeled “EXT PWR.” A TPS25730 USB Power Delivery (PD) controller negotiates with the power source to request 9V at up to 3A. Once negotiated, the input power is routed to three downstream switching regulators, which generate all required system voltages.

The board supports any USB-C power source that complies with the USB PD standard and that can deliver 9V at 3A. A compatible USB-C power adapter is included in the board kit.

Under typical operating conditions, the ZU3EG MPSoC may dissipate up to about 12W. To manage this thermal load, a passive heatsink is pre-installed. However, during sustained high-performance workloads, heat dissipation may exceed the capacity of passive cooling. In such cases, an active fansink can be added for improved thermal management. The board includes a built-in fan controller and a 2-pin fan connector, allowing easy integration of a standard off-the-shelf, clip-on 23mm x 23mm fansink. As examples, the Radian “FJ23/1.3+Y+T725” fansink is available from radianheatsinks.com, and the HF23 with an added fan is available from Malico.

If the fan controller detects an over-temperature condition, it will automatically reset the ZU3 MPSoC device to prevent thermal damage. During this condition, the controller will hold the ZU3 in reset and illuminate a red LED located near the fan connector to indicate the fault. The board will remain in this state until the temperature drops below a safe threshold. Once normal thermal conditions are restored, the board will automatically attempt to reboot from the selected configuration source. To address persistent over-temperature issues, consider using a modified design that reduces the processing load on the MPSoC, or install an active fansink to improve cooling performance.

All required board voltages are generated by a series of onboard switching regulators, as illustrated in the figure below. Two power status LEDs, located in the upper-right corner of the board, indicate the operational state of the PD controller and the main regulator.

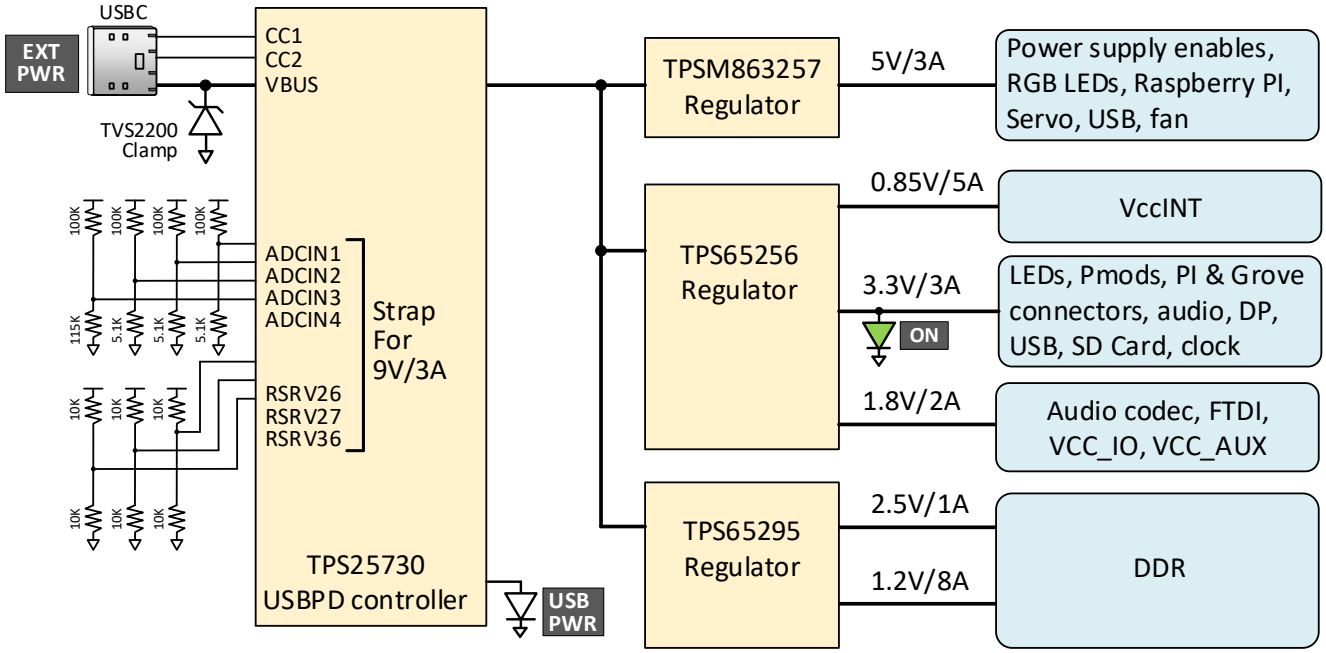

Figure 4: AUP-ZU3 power supplies

Memories

The AUP-ZU3 board is available with either 4GB or 8GB of 3200 MT/s DDR4 memory. The 4GB configuration uses two Micron MT40A2G8T devices, while the 8GB version uses two dual-die MT40A2G8T devices. Both configurations implement a 32-bit data bus, with address, control, and timing signals routed in parallel to both DDR devices. Data lines and data strobes are routed separately to ensure signal integrity and performance.

Pin assignments for the memory interface can be found in the schematic.

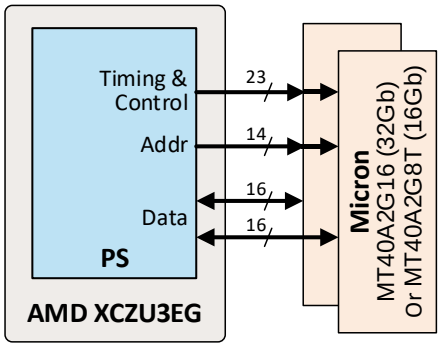

Figure 5: ZU3 DD4 Memory

In addition to the external DDR4 memory, the ZU3EG MPSoC integrates several internal memory resources, including 7.6 Mb of UltraRAM, 1.8 Mb of distributed RAM within the programmable logic, and a 256 KB SRAM memory block within the processing system.

These internal memory blocks provide fast, low-latency storage for real-time tasks and can be used to optimize memory hierarchies in performance-critical applications.

Data Ports

The AUP-ZU3 board features multiple high-speed data interfaces for flexible connectivity and development. It includes two dual-role USB 3.0 user ports, a USB 2.0 port for JTAG programming and UART communication, and a MicroSD card socket for booting and storage.

All data interfaces are fully supported by drivers included in the Linux distribution provided with the PYNQ boot image. This image is available for download from both the Real Digital and PYNQ websites, enabling out-of-the-box support for USB peripherals, serial communication, and SD-based file systems.

USB2/UART port

The AUP-ZU3 board includes a USB-C connector labeled “PROG UART” along the top edge, providing both JTAG and UART (COM) functionality over a single cable. This interface is powered by an FTDI2232 USB 2.0 controller, which appears to the host computer as two separate devices: a JTAG programming interface recognized by AMD-Xilinx development tools, and a standard COM port accessible from Windows and Linux systems.

The JTAG and COM functions operate independently and are always available when the board is connected to a host via the PROG UART port.

The COM port uses a two-wire UART interface, with signals connected to the ZU3EG processing system on pins J16 (RXD) and L16 (TXD). Two onboard LEDs labeled RX and TX, located near the USB-C connector, indicate UART activity for easy monitoring during development and debugging.

USB3 Ports

The AUP-ZU3 board's two USB 3.0 user ports support SuperSpeed (5.0 Gb/s), High-Speed, Full-Speed, and Low-Speed modes in all configurations. USB 2.0 signaling is handled by USB3320C transceivers, while Multi-Gigabit Transceivers (MGTs) on the ZU3EG MPSoC handle the USB 3.0 SuperSpeed signals. Both USB host ports can supply up to 2A of current to connected devices.

To protect against overcurrent conditions, each port includes a Texas Instruments TPS25200 electronic fuse (e-fuse). If the current draw exceeds approximately 2.5A, the e-fuse will disconnect power from the USB port. In such an event, a red LED labeled “USB FLT” near the corresponding port will illuminate, indicating that current flow has been interrupted.

The USB device (slave) port supports up to 12 endpoints and can operate at speeds of up to 5.0 Gb/s, making it suitable for high-speed data transfer and peripheral emulation.

SD Card

A MicroSD card socket located along the top edge of the AUP-ZU3 board supports standard MicroSD cards for boot images, file systems, and general-purpose data storage. This provides a convenient and flexible option for embedded Linux systems and custom applications requiring removable storage.

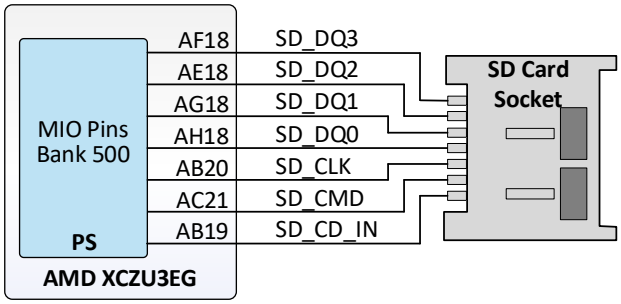

Figure 6. SD Card interface

GPIO

The ZU3 board offers several general-purpose I/O devices, including pushbuttons, slide switches and LEDs that can be used for customized control inputs and status indicators. All GPIO inputs and outputs are active high.

Processing System: One pushbutton and two green LEDs, labelled on the board as shown in the diagram, are connected to MIO pins and are directly accessible by the PS. All three devices are located at the bottom of the board between the Grove and Raspberry PI connectors.

Programmable Logic: Eight pushbuttons, eight white LEDs and four RGB LEDs, labelled on the board as shown in the diagram, are connected to FPGA pins. All devices are located along the bottom edge of the board.

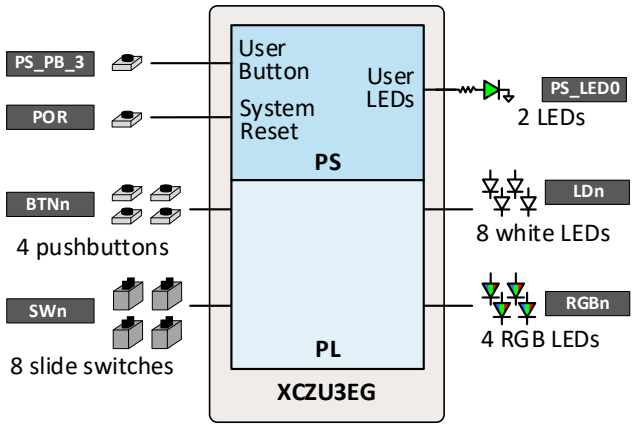

Figure 7: GPIO (pinouts in Appendix A)

Pin numbers for all GPIO devices can be found in Appendix A.

Mini DisplayPort

The AUP-ZU3 board includes a Mini DisplayPort interface capable of driving high-resolution external displays. This interface is driven directly by the Zynq UltraScale+ MPSoC, which includes an integrated DisplayPort controller capable of operating high-speed serial transceivers at up to 6 Gb/s. No additional interface components are required.

The DisplayPort implementation conforms to the VESA DisplayPort Standard Version 1, Revision 2a, and supports multiple data paths for streaming or memory-based audio/video feeds from both the Processing System (PS) and the Programmable Logic (PL). It supports dual audio/video pipelines, enabling simultaneous rendering with features such as alpha blending, chroma resampling, color space conversion, and audio mixing.

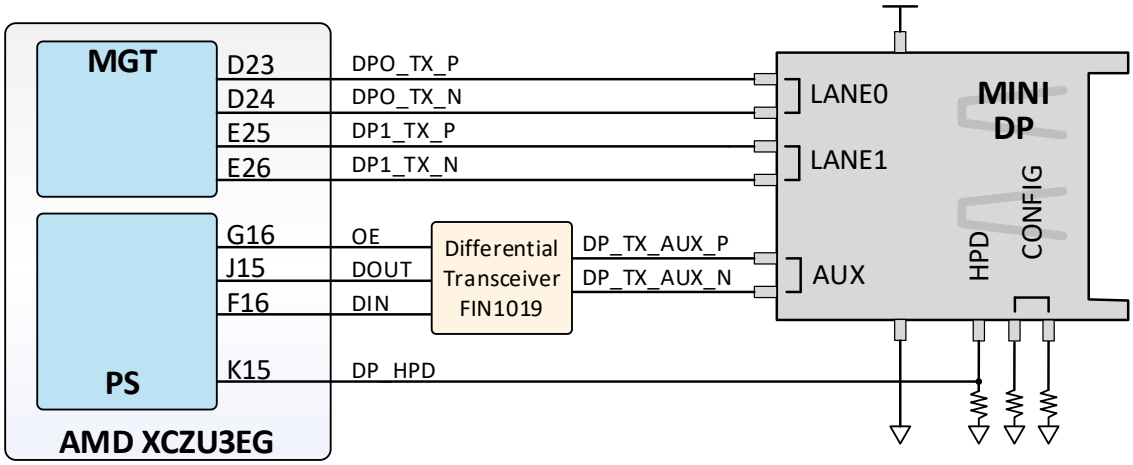

Figure 8. DP Interface

The DisplayPort interface can derive its pixel clock either from one of the PS PLLs or from a clock provided by the PL, giving developers flexible clocking options for custom display applications.

To protect the 3.3V power rail on the DisplayPort connector, a Texas Instruments TPS25200 e-fuse is used. If more than approximately 2.5A of current is drawn, the e-fuse will cut power to the connector. In this case, an LED labeled “DP FLT” will illuminate, indicating a fault condition.

Audio Codec

The ZU3 board features a TLV320 stereo audio codec, capable of recording and playback at sample rates ranging from 8 kHz to 96 kHz. Audio input can be sourced from either a microphone connected to the MIC_IN jack or a line-level signal via the LINE_IN jack. The codec includes advanced signal processing features such as programmable filters, programmable gain amplifiers (PGAs) with automatic gain control (AGC), and noise gate functionality, enabling flexible input conditioning for a variety of audio applications.

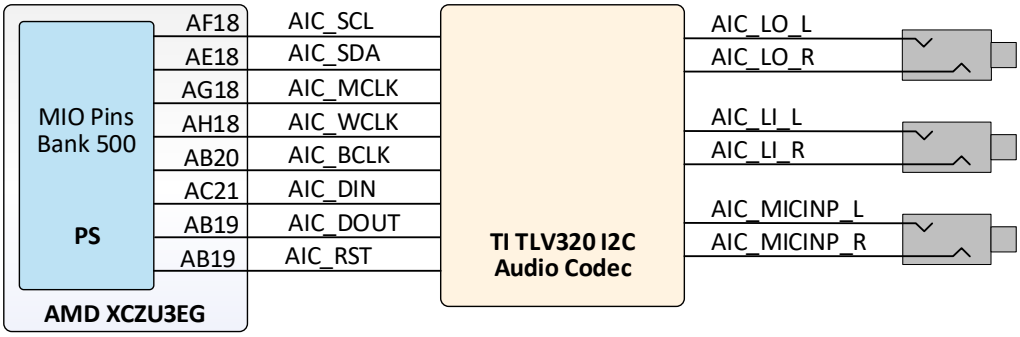

Figure 9. Audio Codec

Audio output is provided through the LINE_OUT jack, which can drive resistive loads ranging from 600 ohms to 10 kΩ, making it suitable for use with amplified headphones or external powered speakers.

The TLV320 codec communicates with the system over the I²C bus using 7-bit addressing, and supports both standard-mode (100 kbps) and fast-mode (400 kbps) I²C operation for configuration and control.

Pmod+ Port

The AUP-ZU3 board includes a single 30-pin Pmod+ connector, providing a versatile interface for custom peripherals and standard Pmod modules. This connector routes 24 high-speed, differentially-paired signals from the PL to a compact, low-cost 100-mil DIP header. It supports signal speeds up to approximately 50 MHz, making it suitable for a wide range of user-defined I/O functions.

Of the 30 available pins, 4 are connected to ground, 4 to VDD, and 22 to FPGA I/O signals, arranged as 11 differential pairs. The connector is organized so that it can accept either two standard 12-pin Pmod modules, inserted into designated subsets of the 30-pin footprint, or a single 30-pin double-Pmod module, using the full connector width.

This flexible arrangement allows developers to easily prototype with off-the-shelf modules or design custom daughterboards. Pmod signal assignments can be found in Appendix A of the documentation.

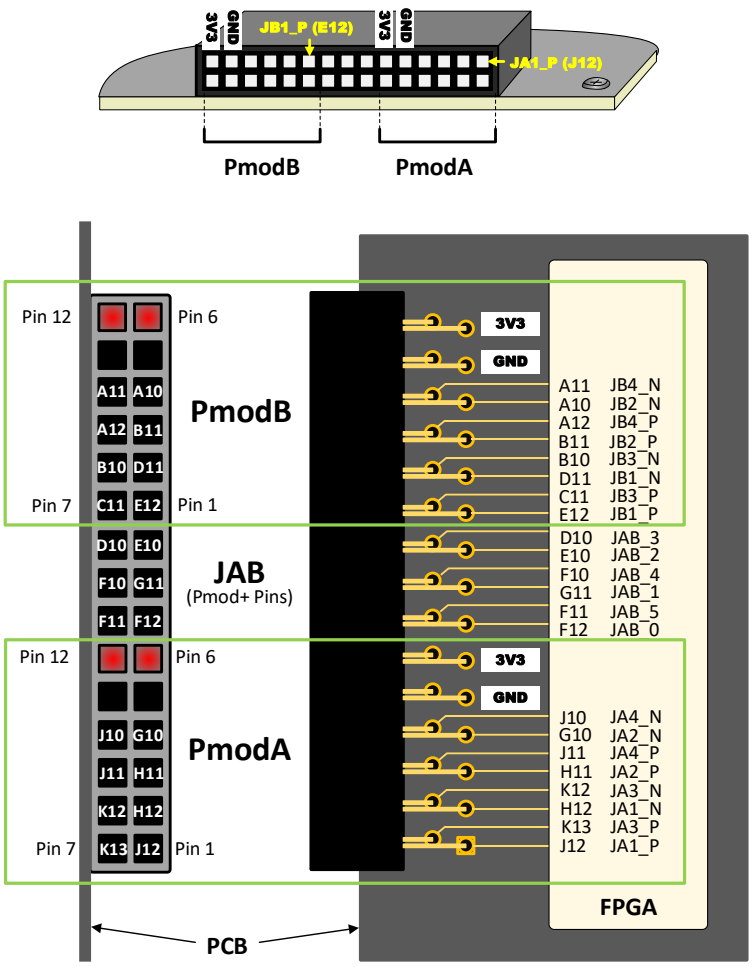

Figure 10: Pmod+ Connector

Joystick and Analog Ports

The ZU3 board includes an unpopulated 5-pin header designed for compatibility with analog joysticks. The joystick's X and Y axis signals are routed to channels 8 and 9 of the Xilinx XADC (Analog-to-Digital Converter), enabling direct analog input capture. Additionally, the board features a 10K potentiometer connected to the primary XADC input channels, providing a convenient analog input source for testing or user interaction.

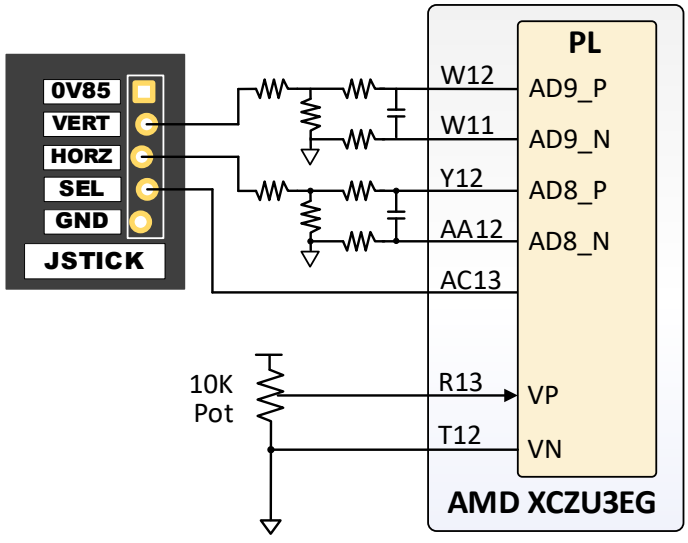

Figure 11. Joystick/Analog ports

Servo Ports

The ZU3 board includes four 3-pin headers designed for compatibility with standard hobby servo motors. These connectors provide signal, power, and ground lines, supporting direct connection to commonly used servos. Because servo motors can draw several hundred milliamps each, power availability must be considered carefully.

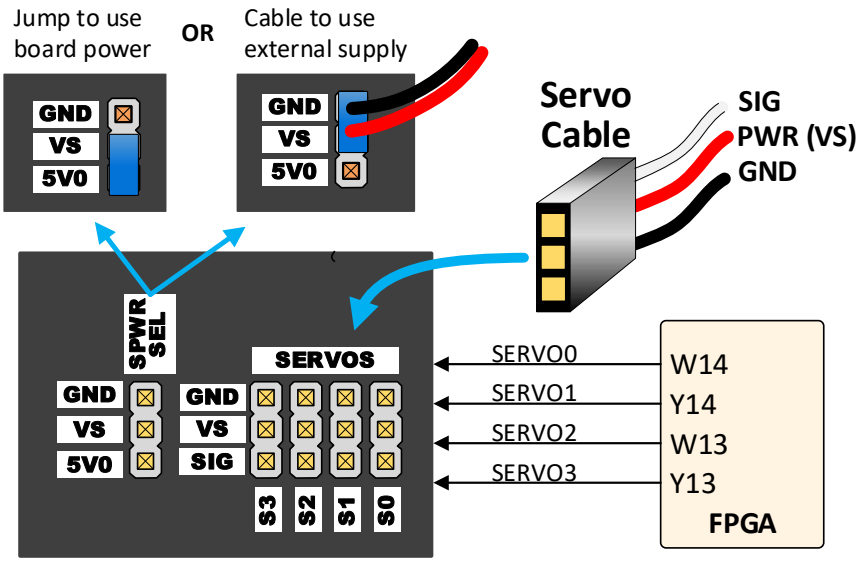

Figure 12. Servo ports

The board's main power supply may be sufficient to drive one or two servos, depending on the total current draw. Servo motor power is routed through the jumper labelled “SPWR SEL”. To power servos using the main supply, install a jumper across the **VS** and **5V** pins on this jumper.

If additional current is required, a two-pin MTE cable can be used to connect an external bench power supply directly to the **VS** and **GND** pins on the “SPWR SEL” jumper, providing a higher-capacity power source for more demanding servo configurations.

Grove connectors

Grove connectors offer a standardized, modular interface for connecting a broad range of peripherals such as sensors, motors and actuators, displays, and other modules to system boards like the ZU3. Each Grove connector features a 4-pin interface comprising 3.3V and GND power rails, along with two signal lines that support multiple protocols, including I²C, UART, or general-purpose digital I/O.

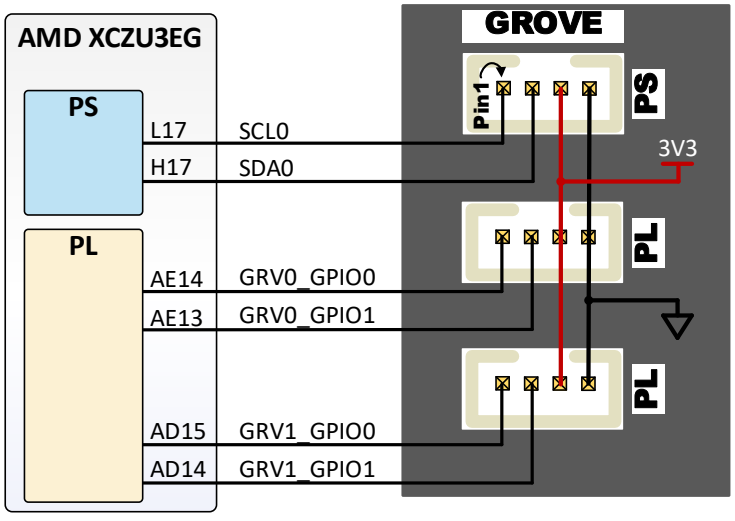

Figure 13. Grove connectors

The ZU3 includes three Grove connectors to support rapid hardware

expansion. One connector is routed to the Processing System (PS), making it ideal for I²C-based modules that can be managed entirely through software. The remaining two connectors are connected to the Programmable Logic (PL), allowing for more flexible use. These can interface with EMIO-connected I²C or UART buses, or be controlled through custom logic blocks implemented in the FPGA fabric.

A wide variety of low-cost Grove modules—ranging from sensors and relays to displays and wireless communication modules—are readily available from Seeed Studio and other vendors. These modules provide a simple and efficient way to extend the functionality of the ZU3 platform with minimal development overhead.

Raspberry Pi Hat port and MIPI Camera connector

The ZU3 is equipped with a full Raspberry Pi expansion connector and a MIPI CSI-2 camera interface. The Raspberry Pi connector supports a wide range of standard “HAT” add-on boards, enabling extensive expansion and customization using components readily available from various manufacturers.

The MIPI CSI-2 camera connector supports cameras compliant with the MIPI standard, offering compatibility with a broad selection of camera modules available from multiple vendors.

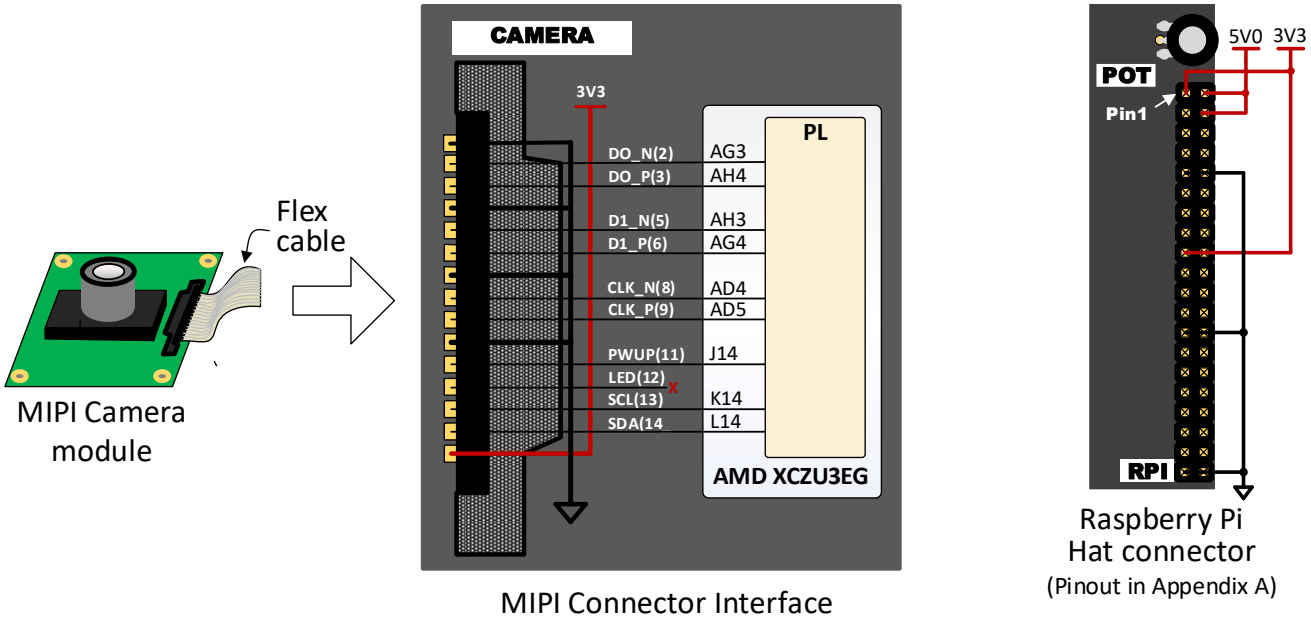

Figure 14. Raspberry Pi and MIPI Interfaces

Appendix A. PL Pinout Table

White LEDs (LVCMOS12)	
PL_USER_LED0	AF5
PL_USER_LED1	AE7
PL_USER_LED2	AH2
PL_USER_LED3	AE5
PL_USER_LED4	AH1
PL_USER_LED5	AE4
PL_USER_LED6	AG1
PL_USER_LED7	AF2

RGBs (LVCMOS12)	
PL_LEDRGB0_R	AD7
PL_LEDRGB0_G	AD9
PL_LEDRGB0_B	AE9
PL_LEDRGB1_R	AG9
PL_LEDRGB1_G	AE8
PL_LEDRGB1_B	AF8
PL_LEDRGB2_R	AF7
PL_LEDRGB2_G	AG8
PL_LEDRGB2_B	AG6
PL_LEDRGB3_R	AF6
PL_LEDRGB3_G	AH6
PL_LEDRGB3_B	AG5

Switches (LVCMOS12)	
PL_USER_SW0	AB1
PL_USER_SW1	AF1
PL_USER_SW2	AE3
PL_USER_SW3	AC2
PL_USER_SW4	AC1
PL_USER_SW5	AD6
PL_USER_SW6	AD1
PL_USER_SW7	AD2

Pushbuttons (LVCMOS33)	
PL_USER_PB0	AB6
PL_USER_PB1	AB7
PL_USER_PB2	AB2
PL_USER_PB3	AC6

Audio (LVCMOS18)	
I2C_AIC_SCL	F5
I2C_AIC_SDA	G5
AIC_nRST[0]	E2
AIC_SDATA_O	G3
AIC_SDATA_I	G4
AIC_SCLK	G1
AIC_LRCLK	F2
AIC_MCLK	F3

Joystick (LVCMOS33)	
SEL_JOYSTICK	AC13
VERT_AD9_P	W12
VERT_AD9_N	W11
HORIZ_AD8_P	Y12
HORIZ_AD8_N	AA12

Servo (LVCMOS33)	
SERVO[0]	W14
SERVO[1]	Y14
SERVO[2]	W13
SERVO[3]	Y13

Grove PL (LVCMOS33)	
PL_GRV_[0]	AE14
PL_GRV_[1]	AE13
PL_GRV_[2]	AD15
PL_GRV_[3]	AD14

Camera (LVCMOS12)	
CAM0_LN0_P	AG3
CAM0_LN0_N	AH3
CAM0_LN1_P	AG4
CAM0_LN1_N	AH4
CAM0_CLK_P	AD5
CAM0_CLK_N	AD4
CAM0_SCL	K14
CAM0_SDA	L14
CAM0_PWUP	J14

PMods (LVCMOS33)	
JA_[0]	J12
JA_[1]	H12
JA_[2]	H11
JA_[3]	G10
JA_[4]	K13
JA_[5]	K12
JA_[6]	J11
JA_[7]	J10
JB_[0]	E12
JB_[1]	D11
JB_[2]	B11
JB_[3]	A10
JB_[4]	C11
JB_[5]	B10
JB_[6]	A12
JB_[7]	A11
JAB_[0]	F12
JAB_[1]	G11
JAB_[2]	E10
JAB_[3]	D10
JAB_[4]	F10
JAB_[5]	F11

Raspberry Pi (LVCMOS3)	
RBP_GPIO[0]	AF10
RBP_GPIO[1]	AG10
RBP_GPIO[2]	AC12
RBP_GPIO[3]	AD12
RBP_GPIO[4]	AE12
RBP_GPIO[5]	AE10
RBP_GPIO[6]	AB11
RBP_GPIO[7]	AD11
RBP_GPIO[8]	AG11
RBP_GPIO[9]	AH11
RBP_GPIO[10]	AH12
RBP_GPIO[11]	AH10
RBP_GPIO[12]	AD10
RBP_GPIO[13]	AA11
RBP_GPIO[14]	AE15
RBP_GPIO[15]	AF13
RBP_GPIO[16]	AB10
RBP_GPIO[17]	AG14
RBP_GPIO[18]	AC11
RBP_GPIO[19]	AB9
RBP_GPIO[20]	AA10
RBP_GPIO[21]	Y9
RBP_GPIO[22]	AH13
RBP_GPIO[23]	AG13
RBP_GPIO[24]	AF12
RBP_GPIO[25]	AF11
RBP_GPIO[26]	AA8
RBP_GPIO[27]	AH14