

Revision: August 5, 2025

1. (12 points) Sketch a block diagram for one bit slice of a magnitude comparator circuit that has two data bits as inputs, and produces EQ, LT, and GT signals as outputs (note that your bit slice circuit will also need to receive additional inputs from neighboring slices). Write Verilog code to implement the bit-slice circuit, and sketch a logic circuit the bit-slice circuit.
2. (5 points) Sketch a block diagram for a 4-bit comparator that uses the bit slice circuits above. Observe that the EQ, LT, and GT outputs are mutually redundant – you can use this observation to create a more efficient 4-bit-slice block diagram circuit by eliminating one of the EQ, LT, and GT outputs. Be sure to eliminate one that offers the best efficiency!

3. (16 points) Complete truth tables and K-maps for HA and FA circuits, using XOR patterns where appropriate. Loop minimum SOP equations, and sketch the circuits (assume all inputs and outputs are active high).

Half Adder

A	B	S	Cout
0	0		
0	1		
1	0		
1	1		

	B	0	1
A	0		
	1		

S =

	B	0	1
A	0		
	1		

Cout =

Full Adder

A	B	Cin	S	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

	B	Cin	00	01	11	10
A	0					
	1					

S =

	B	Cin	00	01	11	10
A	0					
	1					

Cout =

4. (12 points) Sketch an entire Carry-Propagate-Generate circuit that can form the carry-ins for all four bits of 5-bit CLA.

5. (22 points) Complete the four 2's complement arithmetic problems below assuming that all operations use an adder. Showing both the decimal and binary numbers in each case.

$$\begin{array}{r} 17 \\ -11 \\ \hline \end{array} \quad + \quad \begin{array}{r} 000010001 \\ 111110101 \\ \hline \end{array}$$

$$\begin{array}{r} -22 \\ +6 \\ \hline \end{array} \quad + \quad \underline{\hspace{2cm}}$$

$$\begin{array}{r} 35 \\ -42 \\ \hline \end{array} \quad + \quad \underline{\hspace{2cm}}$$

$$\begin{array}{r} 19 \\ -(-7) \\ \hline \end{array} \quad + \quad \underline{\hspace{2cm}}$$

$$\underline{\hspace{2cm}} \quad + \quad \begin{array}{r} 10100110 \\ 11110101 \\ \hline \end{array}$$

Is the answer to the equation on the left correct in 8 bits? Explain.

6. (8 points) Complete the number conversions indicated. Note that all binary numbers are two's complement representations.

$$-19_D = \underline{\hspace{2cm}}_B$$

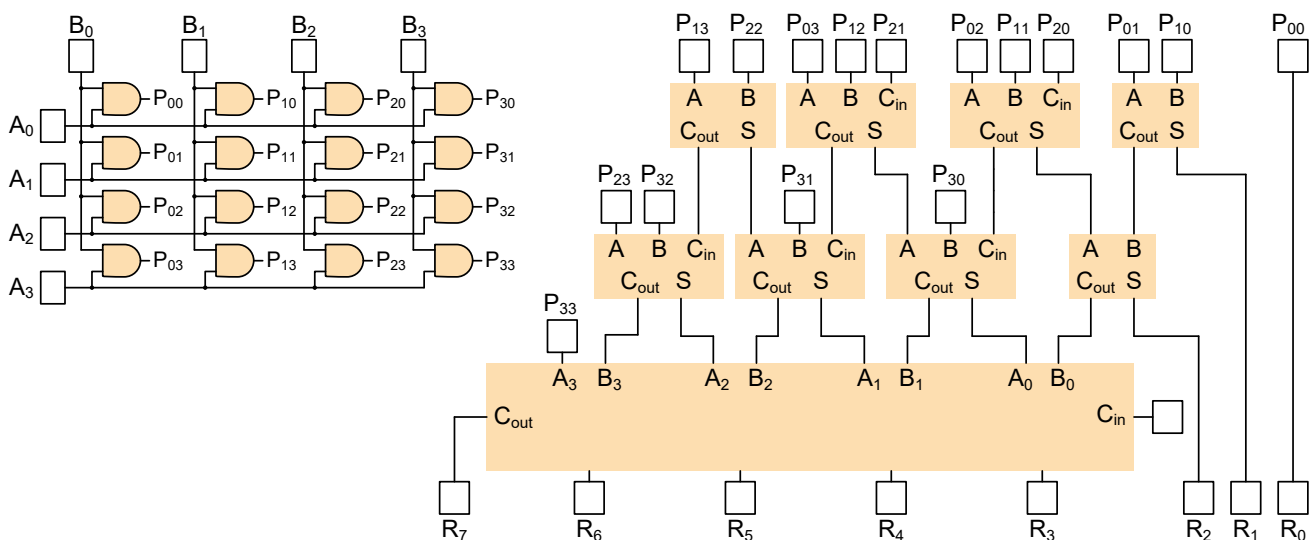
$$10011010_B = \underline{\hspace{2cm}}_D$$

$$10000000 = \underline{\hspace{2cm}}_D$$

$$-101_D = \underline{\hspace{2cm}}_B$$

7. (12 points) Examine several examples of addition overflow and subtraction underflow, and sketch a circuit below that can output a '1' whenever an addition or subtraction result is incorrect due to underflow or overflow. Assume that both operands and result of the addition and subtraction are N-bits. (Hint: compare the carry in and carry out signals of the most-significant bit).

8. (12 points) Fill in the squares below to show all signal values when "1101" and "1010" are multiplied.



Extra Credit

1. (20 points) Design a full-subtractor bit-slice circuit (Borrow-Ripple Subtractor). Label the inputs A, B, and Bin, and label the outputs D and Bout. Start by completing the subtraction examples, then complete the truth table and K-maps, and then sketch the circuit.

$$\begin{array}{r} \text{...}0010\text{...} \\ - \text{...}1000\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0010\text{...} \\ - \text{...}1100\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0110\text{...} \\ - \text{...}1000\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0110\text{...} \\ - \text{...}1100\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0010\text{...} \\ - \text{...}1010\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0010\text{...} \\ - \text{...}1110\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0110\text{...} \\ - \text{...}1010\text{...} \\ \hline \end{array}$$

$$\begin{array}{r} \text{...}0110\text{...} \\ - \text{...}1110\text{...} \\ \hline \end{array}$$

A	B	Bin	D	Bout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

	B _{in}	00	01	11	10
A					
0					
1					

D =

	B _{in}	00	01	11	10
A					
0					
1					

Bout =

2. (12 points) Sketch a circuit to convert a 4-bit binary number to its 2's complement representation using only 3 XOR/XNOR gates and 2 AND or OR gates.

3. (8 points) Sketch a block diagram for a full adder using two half-adder blocks and an OR gate.