

PROJECT 6: STRUCTURAL VERILOG FOR COMBINATIONAL SYSTEMS

Digital Logic Project Submission Form

Revision Date: Sept 28, 2018



I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Point Scale
 4: Exemplary
 3: Complete
 2: Incomplete
 1: Minor effort
 0: Not submitted

Print Name

Sign Name

Date

#	Deliverable	Wt	Pts	Date	Asst. Signature
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Requirements

1: Simulate CombCirc Module and Show the Glitch

1	Program demo	2			
2	Verbal questions answered well	2			

2: Change OR Gate Delay to 2 ns and Simulate the Circuit

1	Program demo	3			
2	Verbal questions answered well	3			

3: Change the Delay of All Gates to 5ns and Simulate the Circuit

1	Program demo	4			
2	Verbal questions answered well	4			

Challenges

1: Delay in Decoder

1	Program demo	3			
2	Verbal questions answered well	3			

Extensions

Describe

1	Program demo				
2	Verbal questions answered well				

Homework Problems

1	N/A	N/A	N/A	N/A	N/A
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