Overview

The RFSoC 4x2 board is a high-performance computing system optimized for sampling signals at up to 5GSPS (Giga Samples Per Second) and generating signals at up to 9.85GSPS. Based on AMD-Xilinx ZYNQ Ultrascale+ Gen3 RFSoC device, the board offers four high-speed ADC ports, two high-speed DAC ports, 8GBytes of fast DDR4 memory, and a QSFP28 port for high-speed data offload.

The RFSoC board is ideally suited to serve as a powerful and highly configurable software defined radio (SDR) system. The AMD-Xilinx ZYNQ UltraScale+ device includes a quad-core ARM Cortex-A53, a dual-core ARM Cortex R5F, monolithic direct RF-sampling ADCs and DACs, and several other high-performance cores to assist with acquiring and processing high speed data.

The RFSoC board works with all AMD-Xilinx Vitis/Vivado tools and the PYNQ open-source framework. The board can be programmed directly using the on-board USB2 programming port, or system configurations and software can be loaded from an SD card at power-on.

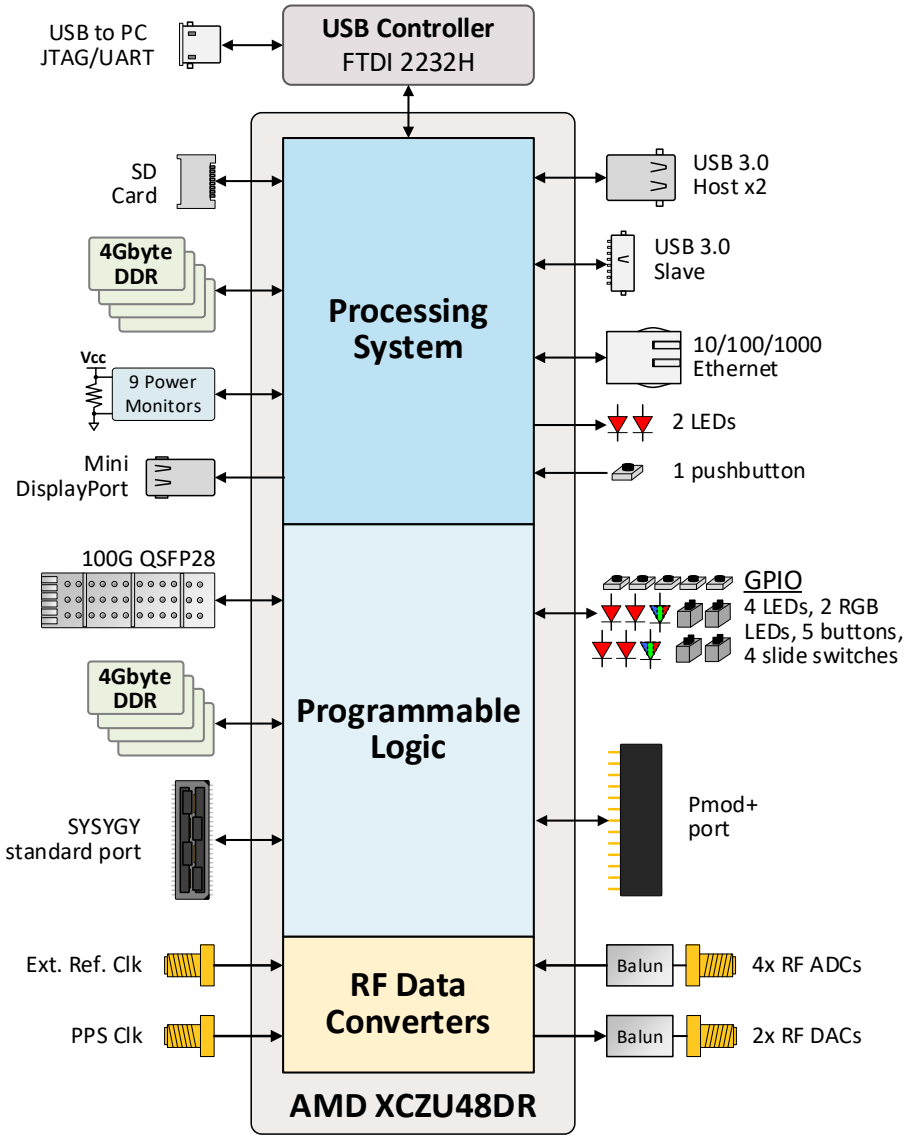


Figure 1: RFSoC Block Diagram

PYNQ

The PYNQ framework is an open-source environment that makes it easier to use AMD-Xilinx platforms. PYNQ is based on Jupyter and provides a Python-based interface to load hardware overlays and control the programmable logic, without the need for ASIC-style, hardware-centric design tools. The PYNQ framework greatly simplifies the process of using of customized hardware in digital systems, and lets a broader range of engineers realize the benefits of using custom hardware in their digital systems.

The combination of the RFSoC's high-performance hardware and the PYNQ framework brings a whole new level of visualization and analysis tools to RF design environments.

RFSoC 4x2 Major Features

The RFSoC 4x2 board is centered around the ZYNQ XCZU48DR UltraScale+ RFSoC device from AMD-Xilinx, and the most critical features are implemented in the AMD-Xilinx device. The XCZUDR48 includes:

Processing System

- A 64-bit quad-core ARM Cortex-A53 and a 32-bit dual-core ARM Cortex-R5F
- An ARM Mali-400 based GPU and NEON advanced SIMD media processing engine
- Single/double precision floating point unit
- 256Kbytes of PS RAM, and a combined 60Mb of 72-bit UltraRAM and block RAM
- Support for 64-bit, 2400MHz DDR4 with an 8-channel DMA controller
- Support for PCI Express, SATA, DisplayPort, Gbit Ethernet, USB3 and other common ports
- System Memory Management Unit

Programmable Logic

- Large Programmable logic array with 930K logic cells and 4.2K DSP slices
- IEEE 802.3 compliant 100G Ethernet

RF System

- 8 14-bit RF ADCs with 5.0GSPS max sample rate
- 8 14-bit RF DACs with 9.85GSPS max sample rate
- 8 SD-FEC IP blocks
- Hardware support for up to 40x decimation/interpolation

The RFSoC board surrounds the ZYNQ device with everything needed to build an SDR system, including high-speed memories, highly stable power supplies, clean and fast clocks, and high-speed data offload. Major board features include:

- Four 14-bit RF ADC SMA ports with sample rates up to 5GSPS
- Two 14-bit RF DAC SMA ports with sample rates up to 9.85GSPS
- External clock, synchronization, and pulse-per-second SMA ports
- Multiple USB ports, including a USB2 port for UART/JTAG, two USB3 host ports, and a USB3 slave port
- 10/100/1000 Ethernet
- 100G QSFP28 port
- 4GBtye, 64-bit, 2400MHz DDR4 connected to the Processing System (PS)
- 4GBtye, 64-bit, 2400MHz DDR4 connected to the Programmable Logic (PL)
- MicroSD card reader
- Multiple high stability, high speed clock sources with advanced jitter reduction
- Mini DisplayPort
- 16-character x 2 row OLED display
- Batter-backed real-time clock
- Active monitoring of power supply currents and voltages
- SYZYGY and Pmod+ expansion connectors
- GPIO devices including pushbuttons, slide switches, LEDs, RGB LEDs.

The figure below shows the RFSoC board with callouts for major features and interfaces.

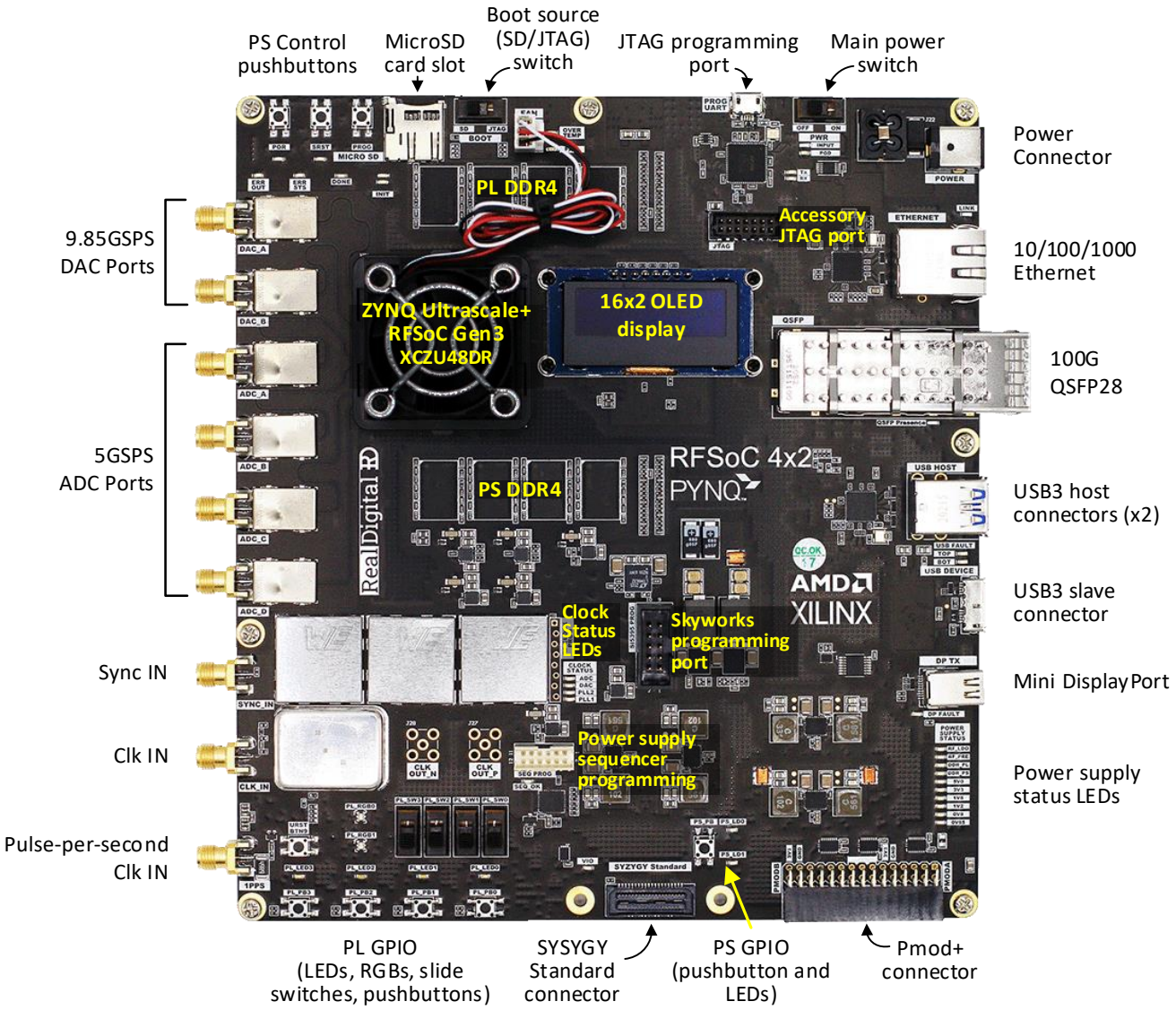


Figure 2: RFSoC Board Major Components

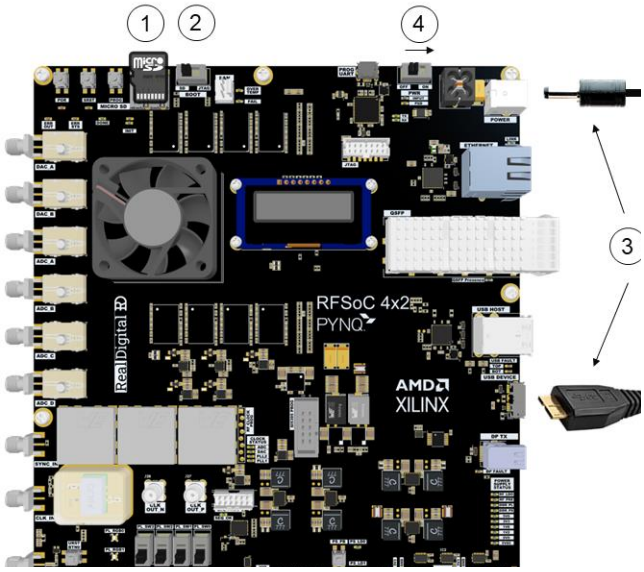
Getting Started

The RFSoC 4x2 board has been designed to work within the PYNQ framework, and with all AMD-Xilinx Vitis/Vivado tools. The PYNQ framework contains many powerful hardware and software resources/IP blocks that can make the advanced features of the RFSoC 4x2 board readily available to all users.

The following four steps offer a quick and easy procedure for setting up the RFSoC 4x2 board and connecting to it from the PYNQ framework. For more detailed instructions on getting started on all supported platforms and for more information, examples and resources see http://www.rfsoc-pynq.io.

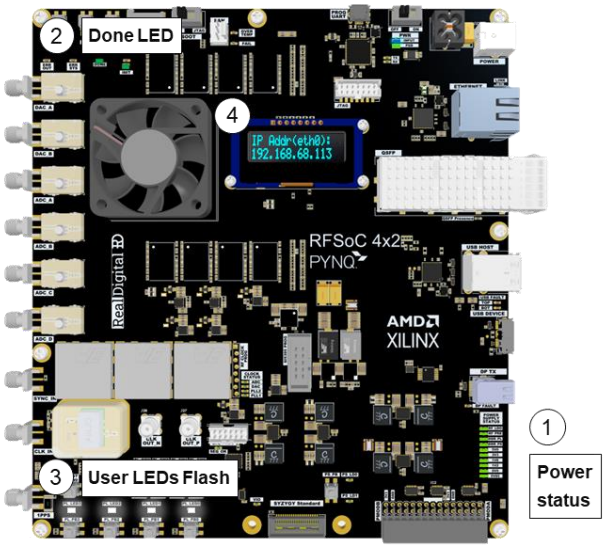
Step 1: Board Set-up

1. Insert the SD card
2. Set the boot mode to SD
3. Connect the USB3 and power cables
4. Slide power switch to ON position



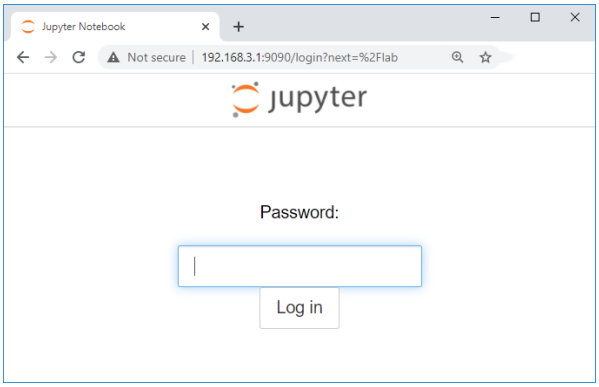
Step 2: Board Power-on

1. After power-on, the power status LEDs will turn on
2. After ~30 seconds, the DONE & INIT LEDs will turn on
3. The 4 white user LEDs will flash briefly and remain on
4. The OLED display will display an IP address



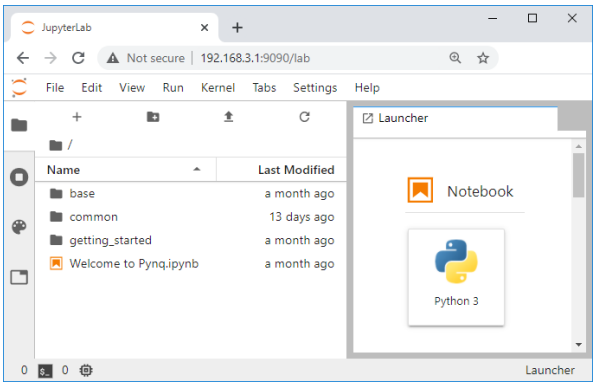
Step 3: Connect to the board

1. On your computer, open a web browser and go to http://192.168.3.1/lab
2. Enter *xilinx* as the password and log in



Step 4: Launch the IDE

You are now in the Jupyter Lab IDE and the PYNQ framework. Use the example notebooks included with PYNQ to start exploring the RFSoC 4x2.



Programming

The RFSoC board includes a USB2-based JTAG programming/debugging port that can be used to download hardware configurations directly from the Vivado environment, and to download, execute and debug software projects from the Vitis environment.

Hardware and software configuration files stored on a MicroSD card can also be used to configure the board. A slide switch labelled “BOOT” near the SD card slot selects between booting from the USB2-JATG port and the SD card.

At power on, if the ZYNQ RFSoC device detects that a properly formatted SD card is present in the SD card socket, it will automatically download its configuration and programming files from the card. The AMD-Xilinx configuration/programming tool can be used to create a properly formatted card from custom designs created in the Vitis and/or Vivado environments.

The PYNQ environment can also be used to configure the RFSoC board. To use PYNQ, the board must be booted from an SD card containing a PYNQ image for the RFSoC 4x2. A MicroSD card preloaded with an RFSoC 4x2 image is included with the RFSoC kit. Additional MicroSD cards can be programmed with the RFSoC PYNQ image and used to boot the system. It is recommended you use a branded MicroSD card, class 10 (or better), and 16GB (or bigger). For example, the SanDisk Edge 16GB Class 10 card available from many retailers. The RFSoC PYNQ image is available through www.realdigital.org and/or www.rfsoc-pynq.io.

Several pushbutton inputs and LED status indicators are available to control and track programming status.

Button	Function
PROG	PL reset. Clears all configuration data and initiates a new PL programming cycle.
POR	PS reset. Resets processing system and initiates a new programming cycle.
SRST	System Reset. Resets entire system and initiates a new programming cycle.

LED	Indication
Done	PL configuration complete
ERR_Out	PMU fault during programming
ERR_Status	Error condition in PMU
PS_POR	Asserted when POR button pressed
PS_SRST	Asserted when SRST button pressed
PS_INIT	PL initialized

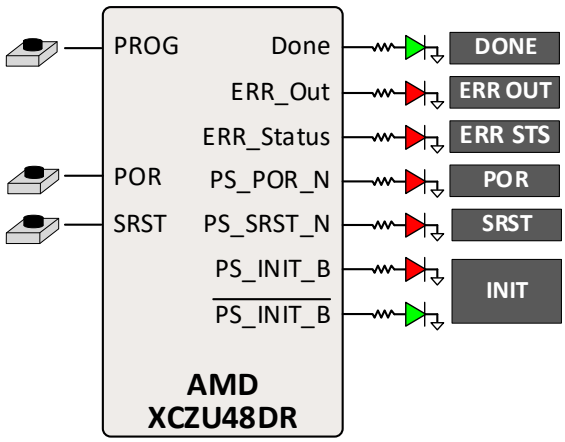


Figure 3: Programming status and control

Sampling Circuits

The ADC input and DAC output signals pass through decoupling capacitors and a balun, with no active components in the signal chain.

A MABA-011118 balun rated at 10 MHz - 10GHz is connected between each SMA and ADC, allowing a single ended antenna and other signal sources to be connected with no external circuitry required. On the RFSoC board, the baluns and capacitors are underneath six 10mm x 14mm RF shields to better isolate the circuits.

Appendix D contains a table from AMD-Xilinx document DS926 showing the RF-ADC electrical characteristics for the XCZU48DR. Refer to the source document on the AMD-Xilinx website for more information.

Appendix E contains a table from AMD-Xilinx document DS926 showing the RF-DAC electrical characteristics for the XCZU48DR. Refer to the source document on the AMD-Xilinx website for more information.

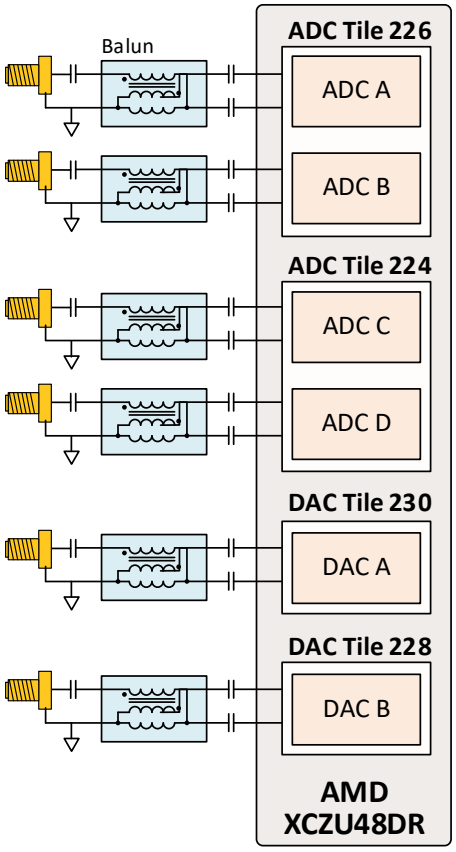


Figure 4: ADC inputs and DAC outputs

The ADCs and DACs in the RFSoC device are organized into tiles, with two ADCs and two DACs per tile. On the RFSoC 4x2 board, SMA connectors drive four ADCs in two tiles: ADCA and ADCB (as labelled on the board) are connected to the ADCs in tile 226, and ADCC and ADCD to the ADCs in tile 224; and two DACs in two tiles: DACA in tile 230 and DACB in tile 228. Each tile includes a PLL and all the necessary clock handling logic and distribution routing for the analog and digital logic, along with a Digital Down Converter (DDC) for each ADC, and Digital Up Converters (DUC) for each DAC.

The AMD-Xilinx Zynq Ultrascale+ RFSoC Gen3 includes 14-bit direct RF-sampling analog-to-digital (RF-ADC) converters at up to 5GSPS, and 14-bit RF-sampling digital-to-analog (RF-DAC) data converters at up to 9.85GSPS. The data converters are high-precision, high-speed and power efficient. Both are highly configurable and tightly integrated with the programmable logic (PL) resources of the Zynq UltraScale+ RFSoC.

Customizable blocks for the data converters are available in the Vivado IP catalog, and configuration parameters can be readily entered using a dialog-box interface. Sample data is transported in and out of the converter blocks using the AXI stream interface, which is configurable up to 512 bits wide. Data can be configured as real or I/Q, and Digital Up Converters (DUC) and Digital Down Convertors (DDC) are configurable for each channel, along with mixer settings and Nyquist zone selection.

Clocks

The RFSoC uses several precision clock synthesizers and jitter attenuators to produce the highly stable and accurate clocks required by the FPGA fabric and RF/sampling circuits.

Most of the clocking signals used by the processing system and FPGA fabric are produced by a Skyworks Si5395 clock multiplier/jitter attenuator driven by a 48MHz crystal resonator. The Si5395 device can generate a wide range of frequencies based on user-programmed parameters stored in its internal configuration ROM. On the RFSoC board, those parameters have been factory-programmed to generate the frequencies shown in the figure below (the full part number for the pre-programmed device is SI5395B-A13886-GM). The ROM can be reprogrammed to generate other frequencies using the on-board I2C programming port/connector labelled "SI5395 PROG". Note the ROM can only be updated twice. See the Skyworks document UG286 for information on obtaining and using the Skyworks ClockBuilderPro software and programming dongle.

A Texas Instruments LMK04828 ultra low noise clock jitter cleaner is used to generate additional FPGA fabric clocks from a 10MHz clock supplied by the Si5395. The LMK device receives a second clock input from a 160MHz VCXO, and can use that input to generate clocks to drive two RF frequency synthesizers. The RF synthesizers produce the high-speed, stable clock signals used by the RFSoC sampling circuits. By default, the LMK is programmed to drive two LEDs labelled "PLL1" and "PLL2" that indicate when the internal VCOs are producing stable clock signals to the RF synthesizers.

An external clock input (CLK IN) and synchronization input (SYNC IN) are also available to the LMK via SMA connectors. The external clock input allows an external time base to be used, and the SYNC input allows synchronization across multiple RFSoC boards. If the SYNC input is needed, OUT1 and OUT5 of the LMK must be enabled to synchronize the downstream LMX's (OUT1 and OUT5 are powered off by default). Enabling OUT1 and OUT5 will also reset the dividers in the LMX's so that all ADC and DAC clocks are fully synchronized.

The ADC and DAC sample clocks are produced by Texas Instruments LMX2594 RF frequency synthesizers. The LMX devices each drive an LED that indicates when the synthesizers are producing stable clock signals.

At power-on, the LMK and LMX devices must be programmed to produce the specified output frequencies before they can be used. The LMX and two LMX chips are connected to the ZYNQ RFSoC's processing system via an SPI bus so they can be programmed at runtime. The software environment provided as a part of the PYNQ framework automatically programs the LMK and LMXs during the start-up sequence when an RFSoC 4x2 overlay is loaded.

It is possible to change the LMK input clock source, and to change the frequencies generated by the LMK and LMX devices by changing the device parameters programmed during the startup sequence. To create a new programming file for the LMK or LMX devices, the free TI TICSPRO software tool can be used to generate a "TICS" file with the desired configuration (see https://www.ti.com/tool/TICSPRO-SW). The TICS file produced by the TICSPRO software can then be used to program the LMK and/or LMX during the startup sequence. The PYNQ 'xrfclk' package supports configuration of the LMK and LMX using TICS files; see the PYNQ documentation for more information.

On the RFSoC board, the LMK and LMX devices are underneath three 20mm x 20mm RF shields to better isolate the circuits and attenuate possible emissions.

The following diagram shows clock generation and routing on the RFSoC 4x2 board. Note that all frequencies shown in the diagram are the default frequencies generated by the RFSoC PYNQ overlay; these can all be changed by reprogramming the LMK and LMX devices.

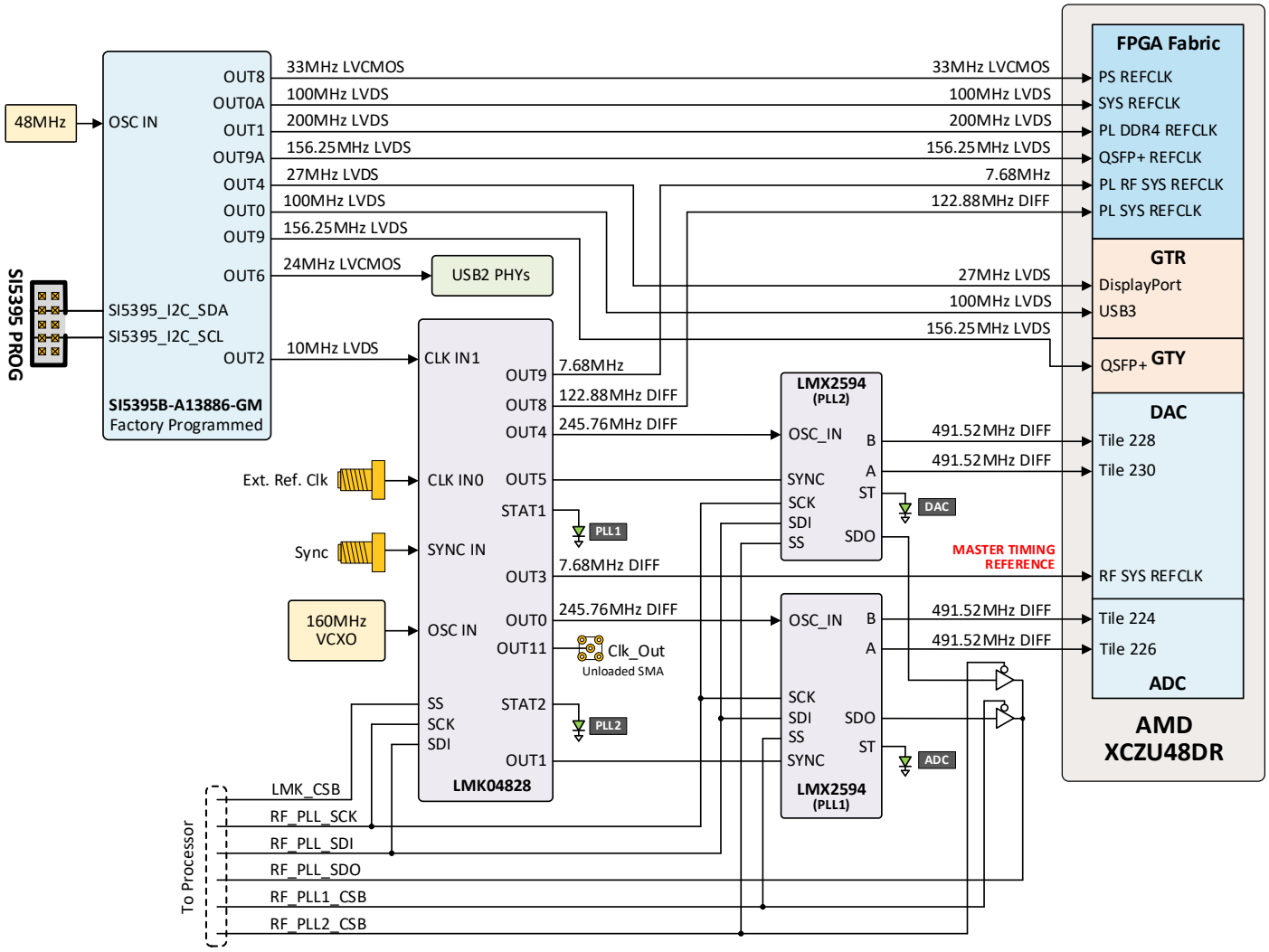


Figure 5: RFSoC Clocking Scheme

Pulse-per-second (PPS) interface

The RFSoC board contains a PPS interface that can be used to capture PPS radio beacon signals. PPS signals are typically very accurate and stable, and are broadcast by various devices to create a wireless synchronization pulse across a relatively wide area. PPS receivers can use the PPS pulse to minimize the effect of clock drift over time, and to maintain synchronization with other receivers.

The RFSoC board provides two PPS signals derived from a comparator and a Schmidt trigger, and an 8-bit value SPI ADC. Pin connections are shown in Appendix A.

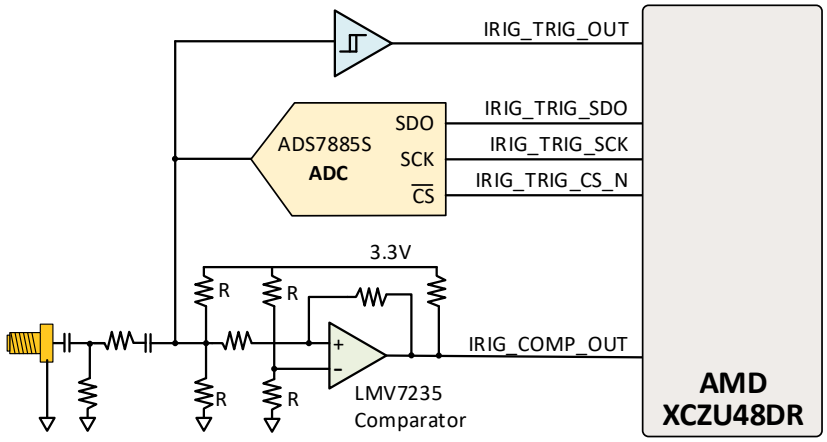


Figure 6: PPS signal conditioning

Power Supplies

Board power is supplied by an external 12V, 10A wall-plug power supply with a 2.1mm, center-positive barrel connector (included with the kit). Input power input is routed through an EMI filter and a power FET controlled by a Texas instruments LM25069 overvoltage/overpower protection circuit. The LM25069 is enabled by the "ON-OFF" switch in the upper right corner of the board. When the power switch is on, the LM25069 will turn on the power FET when the input voltage is in the specified range of 10.7V to 13.3V DC, and it will keep power flowing until the switch is turned off, until an excessive power condition (more than about 110W) is detected, or until an under-voltage or over-voltage condition is detected. The blue LED near the main power switch indicates whether input voltage is present, and the green LED indicates whether the LM25069 has allowed input power to flow to the main regulators.

Because the AMD-Xilinx ZYNQ Ultrascale+ RFSoC can dissipate more than 20W, a heatsink and fan are required to remove excess heat. The fan controller drives two status LEDs. A yellow LED near the fan connector labelled "FAIL" indicates a stuck fan motor rotor, and if illuminated, a new heatsink and fan assembly should be installed. A red LED near the connector labelled "OVER TEMP" indicates a die temperature fault. An over-temperature fault will activate the RFSoC's power-on reset signal to reset the system. If the over-temperature LED continues to be illuminated after a reset cycle, turn off the main switch, unplug the power connector, remove all accessory boards and unplug all cables. After waiting at least two minutes, repower the board and make sure the LED is not illuminated and that heatsink fan is operating normally.

If the LM25069 shuts down main power due to an error condition (i.e., excessive power or under or over voltage), turn off the main switch, unplug the power connector, remove all accessory boards and unplug all cables. After waiting at least two minutes, repower the board and make sure the heatsink fan is operating normally.

The first figure below shows the main power supplies. A series of switching power supplies generate all required system voltages, and status LEDs show the operating status of most supplies (the LED's are all located on the lower right corner of the board, and are labelled as shown in the drawing). Three of the switching-supply outputs deliver power to the ADC and DAC sampling circuits, but not directly - these three supplies drive downstream LDOs, and the LDO's provide power to the sampling circuits. This topology creates the quietest ADC and DAC voltages possible (see the second figure below).

Texas Instruments INA220 power monitor IC's are used to provide active monitoring on nine of the most critical power supplies. The INA220 measures supply voltage and shunt drop with 0.5% accuracy, and the processing system can access the data on the CMON I2C bus at the addresses shown in the figure below.

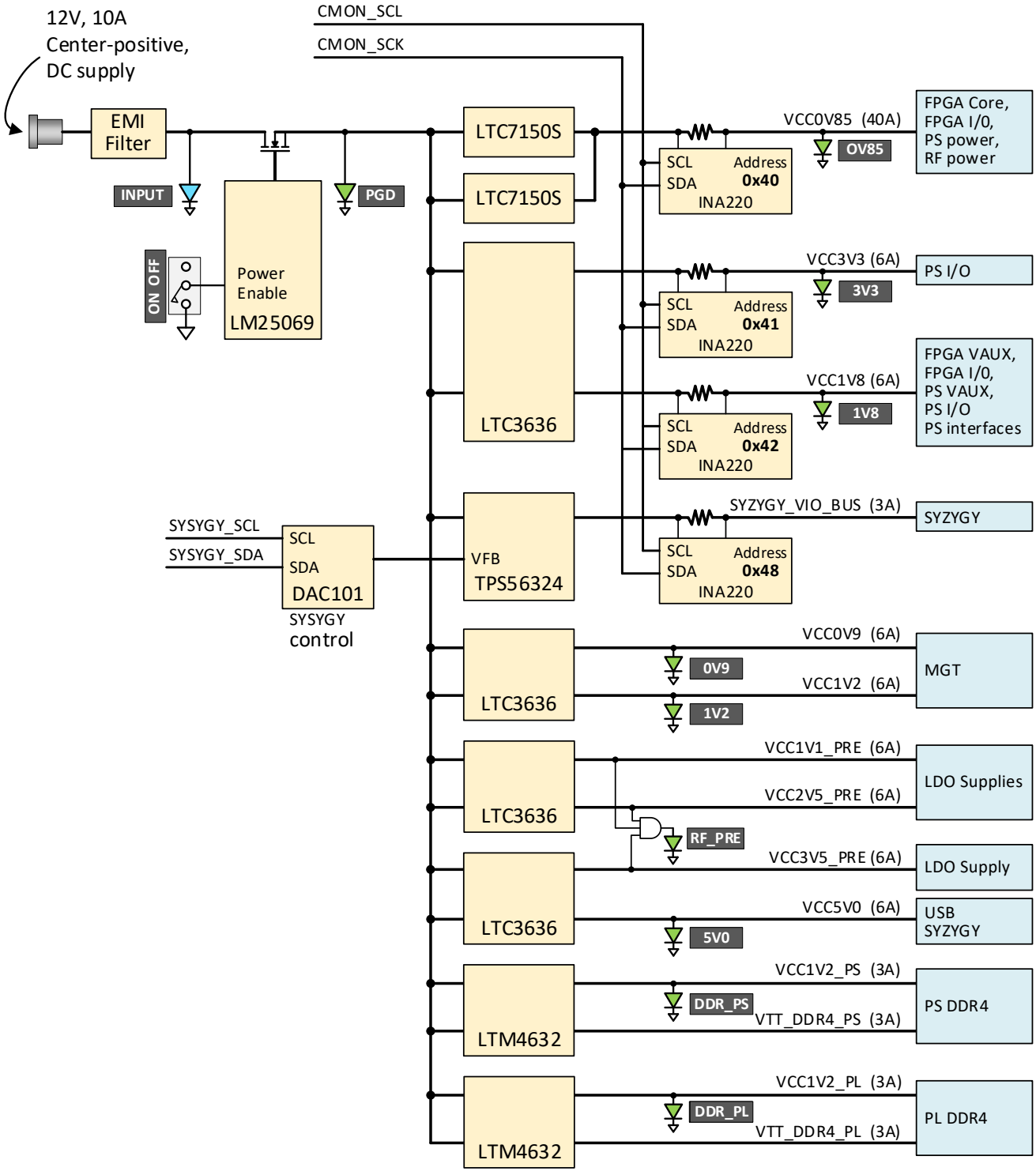


Figure 7: Main RFSoC 4x2 power supplies

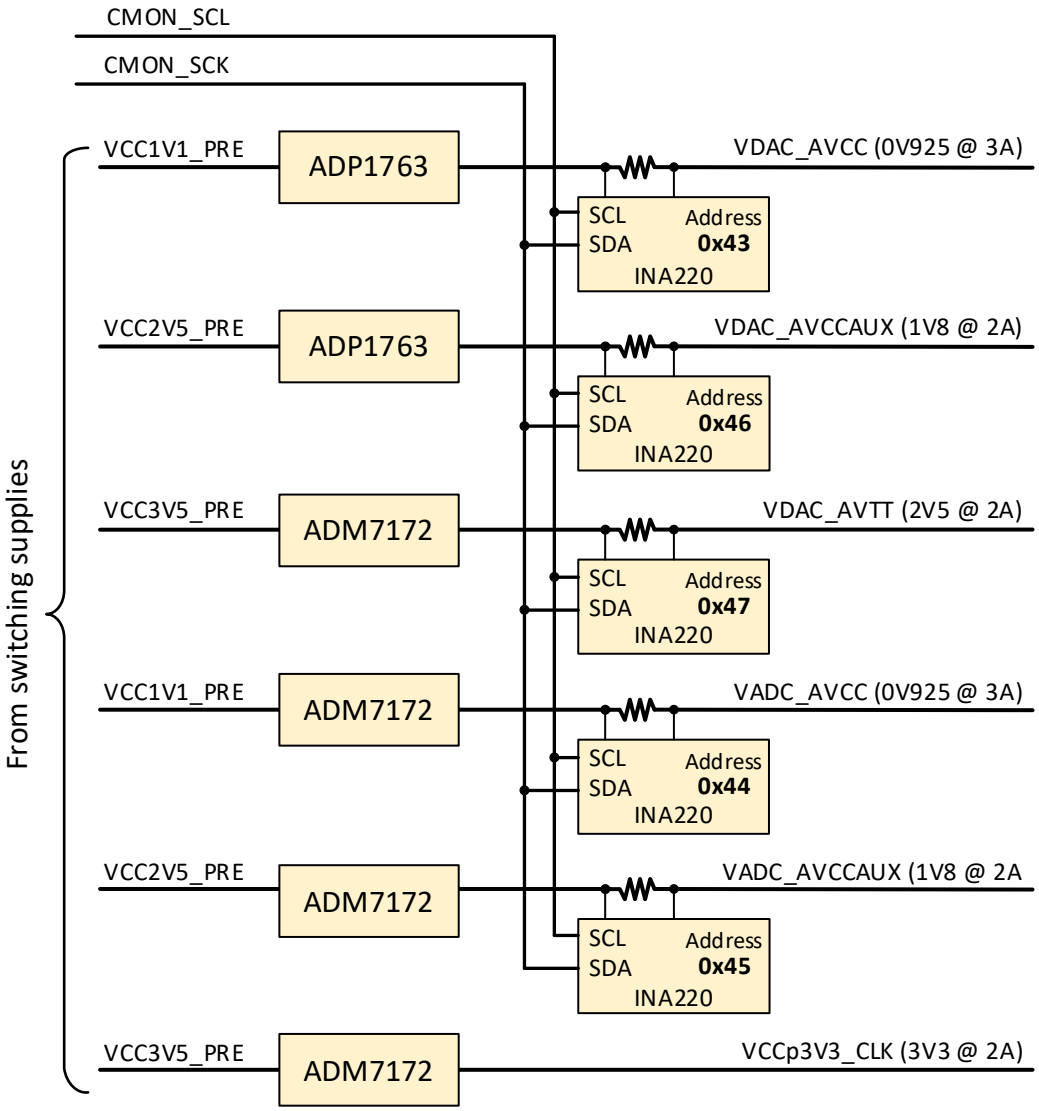


Figure 8: LDO power supplies for RFSoC 4x2 sampling circuits

Memories

The RFSoC includes two separate 4GByte, 64-bit, 2400MHz DDR4 memory arrays – one connected to the processing system for processor operations, and one connected to the FPGA fabric for sample data. Both memory arrays use four 512Mbyte 16-bit memories, with address, timing and control routed to all memories in parallel, and data and data strobes routed separately.

Both memory busses can sustain transfers at 2400MHz. Individual pin assignments can be found in the schematic and in the pinout file in appendix A.

In addition to the external DDR4 memories, the programmable logic section of RFSoC device includes a combined 60Mb of UltraRAM and dual-port block ram, and the processing system includes 256Kbytes of SRAM.

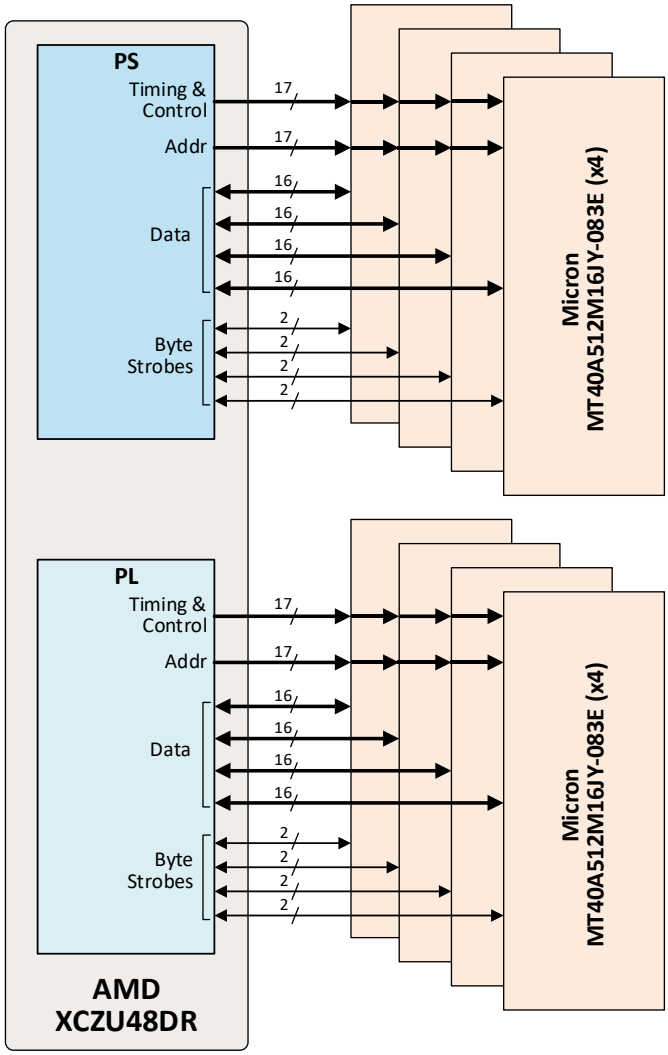


Figure 9: RFSoC External Memory Organization

Data Ports

The RFSoC board offers several ports for high speed data offload, and for exchanging status, control and programming information. All data ports are supported with drivers in the Linux installation that is a part of the PYNQ boot image available on the Real Digital and RFSoC PYNQ websites.

QSFP28 Port

The RFSoC board includes a QSFP28 (Quad Small Form Factor Pluggable) transceiver port that supports Ethernet, Fiber, InfiniBand and SONET/SDH standards with different data rate options up to 100Gbps. An LED labelled “QSFP PRESENCE” near the connector will illuminate when a plug-in is recognized.

Ethernet

A Texas Instruments DP83867CRRGZR ethernet PHY is connected to one of the four available tri-speed ethernet MAC’s available in the RFSoC’s processing system using the RGMII interface. The MAC supports jumbo frames and time stamping through interfaces based on the IEEE Std 1588v2.

Three status LEDs show ethernet status. A yellow LED integrated into the Halo RJ45 ethernet connector shows gigabit link status, and a green LED in the connector shows activity. A blue “LINK” LED near the RJ45 connector shows link status for 10/100 connections.

USB2/UART port

A microUSB port labelled “PROG UART”, located near the main power switch, is driven by an FTDI2232 USB2 slave controller. The FTDI device binds to FTDI drivers on a host computer, and offers a JTAG programming port for use by the AMD-Xilinx tools, and also a COM port for general use. The JTAG and COM ports are independent, and both are always available.

The COM port uses a two-wire interface connected to processing system pins A26 (RXD) and A27 (TXD). Two LEDs near the microUSB connector labelled RX and TX show UART activity.

USB3 Ports

The RFSoC board includes two USB3 host ports and one USB3 slave port.

The host port is compliant to the USB 3.0 and the Intel XHCI specifications, and supports super, high, full and low speed modes in all configurations. The host ports are driven from a USB5742 2-port HS USB Hub Controller, and all signals are protected with ESD diodes. Both host port connectors can provide up to about 2.5A to connected devices. A Texas Instruments TPS25200 e-fuse will interrupt the flow of power to the USB connector’s power pins if more than about 2.5A are drawn from the connector. LEDs labelled “USB FAULT TOP/BOTTOM” will illuminate if the e-fuse interrupts current flow.

The device/slave port supports up to 12 end points and can operate at speeds up to 5.0Gb/s.

GPIO

The RFSoC board offers several general-purpose I/O devices, including pushbuttons, slide switches and LEDs that can be used for customized control inputs and status indicators. All GPIO inputs and outputs are active high, except the URST button which is active low.

Processing System: One pushbutton and two green LEDs, labelled on the board as shown in the diagram, are all located at the bottom of the board between the SYZYGY and Pmod connectors.

Programmable Logic: Five pushbuttons, four white LEDs and two RGB LEDs, labelled on the board as shown in the diagram, are connected to FPGA pins. All devices are in the lower left corner of the board.

Pin numbers for all GPIO devices can be found in Appendix A.

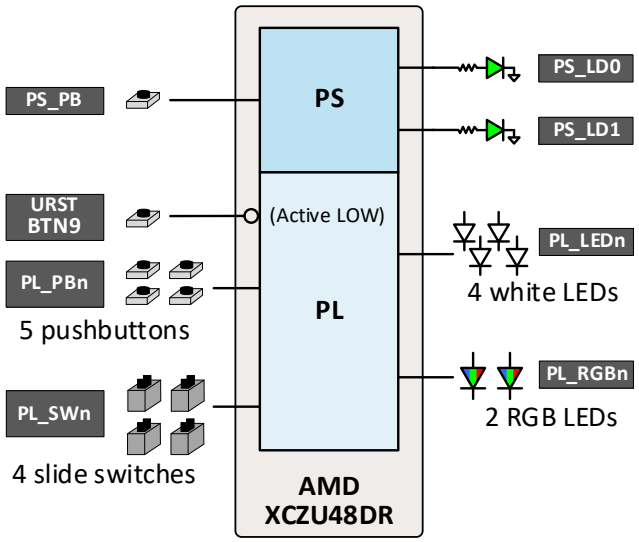


Figure 10: GPIO

OLED Display

The RFSoC board contains a NewHaven 0216AW 16x2 character display connected to the processing system via an SPI bus. The default PYNQ framework uses the display to show board status during start-up and normal operations. Drivers exist in the framework to allow the display of custom messages.

Mini DisplayPort

The RFSoC 4x2 board includes a mini DisplayPort interface for driving high-resolution displays.

The Zynq UltraScale+ RFSoC includes an integrated DisplayPort interface module that can drive high-speed serial transceivers at up to 6Gb/s, so no other interface components are needed. The DisplayPort interface is based on the VESA DisplayPort Standard Version 1, Revision 2a and provides multiple interfaces that process live audio/video feeds from either the PS or the PL, or store audio/video from memory frame buffers. It simultaneously supports two audio/video pipelines, providing on-the-fly rendering features like alpha blending, chroma resampling, color-space conversion, and audio mixing. The DisplayPort can use one of PS PLLs or the clock from PL to generate the pixel clock.

A Texas Instruments TPS25200 e-fuse will interrupt the flow of power to the DisplayPort's 3.3V power pin if more than about 2.5A are drawn from the connector. An LED labelled "DP FAULT" will illuminate if the e-fuse interrupts current flow.

Expansion Connectors

SYZGY Port

The RFSoC board includes one standard SYZYGY port. The 40-pin Samtec QSE SYZYGY connector includes 32 differentially routed FPGA signals capable of moving data at up to 500MHz, a differential clock, an I2C bus, a fixed 5V/3A supply, a fixed 3.3V/3A supply, and a 3A, 1.2V to 3.3V user-programmable supply. A status LED near the SYZYGY illuminates when the VIO voltage is enabled.

Several manufacturers produce plug-in boards that add various capabilities to FPGA systems, and custom boards can readily be produced at a relatively low cost. See www.syzygyfpga.io for more information.

Pmod+ Port

The RFSoC board includes one 30-pin Pmod+ port. The Pmod port brings 24 differentially-routed FPGA signals to a simple and low-cost 100-mil DIP connector. Users can attach custom peripheral boards with signals speeds up to about 50MHz, or any one of a variety of Pmod peripherals offered from several vendors.

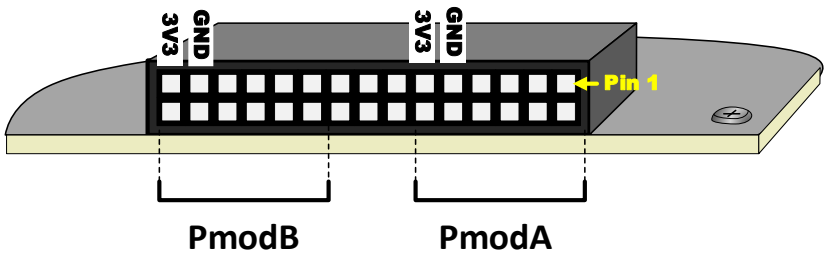


Figure 11: Pmod+ Connector

Of the 30 connector pins available on the Pmod+ port, 4 are connected to ground, 4 to Vdd, and 22 to FPGA signals. All 22 FPGA signals are routed as differential pairs. The connector signals are organized so that two standard 12-pin Pmod connectors can be inserted into the marked subsets of holes, or the entire 30-pin connector can be used for a double-Pmod. Pmod pin assignments are available in appendix A.

Appendix A. RFSoC 4x2 Pinout Tables

All signals use I/O Standard LVCMOS18 unless otherwise noted

Clock Signals

Programmable Logic Clocks				
Signal	**Use**	**Pin**	**Speed**	**IO Standard**
PL_DDR4_REF_CLK_P	DDR4 CLOCK	G12	200 MHz	DIFF_SSTL12
PL_DDR4_REF_CLK_N	DDR4 CLOCK	G13	200 MHz	DIFF_SSTL12
SYS_CLK_100M_P	GENERAL PL CLOCK	AM15	100 MHz	LVDS
SYS_CLK_100M_N	GENERAL PL CLOCK	AM15	100 MHz	LVDS
SYS_CLK_QSFP_P	QSFP SUBSYSTEM	AL17	156.25 MHz	LVDS
SYS_CLK_QSFP_N	QSFP SUBSYSTEM	AM17	156.25 MHz	LVDS
FPGA_REFCLK_IN_P	FOR ADC/DAC SUBSYSTEM	AN11	122.88 MHz	LVDS
FPGA_REFCLK_IN_N	FOR ADC/DAC SUBSYSTEM	AP11	122.88 MHz	LVDS
SYS_REF_FPGA_P	FOR ADC/DAC SUBSYSTEM	AP18	7.68 MHz	LVDS
SYS_REF_FPGA_N	FOR ADC/DAC SUBSYSTEM	AR18	7.68 MHz	LVDS

Processing System Clocks				
PS_REF_CLK	PS reference clock	AC30	33.333MHz	LVCMOS18
GTR_505_REF_CLK_DP_N	DisplayPort	AJ34	27MHz	LVDS
GTR_505_REF_CLK_DP_N		AJ35		LVDS
GTR_505_REF_CLK_USB3_P	USB3	AG35	100MHz	LVDS
GTR_505_REF_CLK_USB3_N		AG35		LVDS

Programmable Logic Signals

PMOD Connector	
Signal	**Pin**
PMOD0_0	AF16
PMOD0_1	AG17
PMOD0_2	AJ16
PMOD0_3	AK17
PMOD0_4	AF15
PMOD0_5	AF17
PMOD0_6	AH17
PMOD0_7	AK16
PMOD1_0	AW13
PMOD1_1	AR13
PMOD1_2	AU13
PMOD1_3	AV13
PMOD1_4	AU15
PMOD1_5	AP14
PMOD1_6	AT15
PMOD1_7	AU14
PMOD01_0	AW16
PMOD01_1	AW15
PMOD01_2	AW14
PMOD01_3	AR16
PMOD01_4	AV16
PMOD01_5	AT16

1PPS Control	
IRIG_ADC_SDO	AK13
IRIG_ADC_SCLK	AH12
IRIG_COMP_OUT	AJ13
IRIG_TRIG_OUT	AH13

SYZYGY Connector	
Signal	**Pin**
SYZYGY_D0_P	AU2
SYZYGY_D0_N	AU1
SYZYGY_D1_P	A7
SYZYGY_D1_N	A6
SYZYGY_D2_P	AV3
SYZYGY_D2_N	AV2
SYZYGY_D3_P	C8
SYZYGY_D3_N	C7
SYZYGY_D4_P	AW4
SYZYGY_D4_N	AW3
SYZYGY_D5_P	E9
SYZYGY_D5_N	E8
SYZYGY_D6_P	AT7
SYZYGY_D6_N	AT6
SYZYGY_D7_P	F6
SYZYGY_D7_N	E6
SYZYGY_S16	B8
SYZYGY_S17	AR6
SYZYGY_S18	D6
SYZYGY_S19	AR7
SYZYGY_S20	C6
SYZYGY_S21	AU7
SYZYGY_S22	B5
SYZYGY_S23	AV7
SYZYGY_S24	A5
SYZYGY_S25	AU8
SYZYGY_S26	C5
SYZYGY_S27	AV8
SYZYGY_P2C_CLK_P	AV6
SYZYGY_P2C_CLK_N	AV5
SYZYGY_C2P_CLK_P	B10
SYZYGY_C2P_CLK_N	B9

User Pushbutton	
Signal	**Pin**
PL_USER_PB0	AV12
PL_USER_PB1	AV10
PL_USER_PB2	AW9
PL_USER_PB3	AT12

User Slide Switches	
PL_USER_SW0	AN13
PL_USER_SW1	AU12
PL_USER_SW2	AW11
PL_USER_SW3	AV11

User LEDs	
PL_USER_LED0	AR11
PL_USER_LED1	AW10
PL_USER_LED2	AT11
PL_USER_LED3	AU10
PL_LEDRGB0_R	AM8
PL_LEDRGB0_G	AM7
PL_LEDRGB0_B	AN8
PL_LEDRGB1_R	AR12
PL_LEDRGB1_G	AP8
PL_LEDRGB1_B	AT10

QSFP		
Signal	**Pin**	**Notes**
SFP_MODPRSL	AL22	MODULE PRESENT
SFP_INTL	AM22	MODULE INTERRUPT
SFP_RESETL	AL21	MODULE RESET
SFP_LPMODE	AN22	MODULE LOW POWER MODE
SFP_MODSEL	AK22	MODULE SELECT
GTY_128_REF_CLK_QSFP_P	AA33	156.25 MHz
GTY_128_REF_CLK_QSFP_N	AA34	156.25 MHz
QSFP_TX1_P	Y35	
QSFP_TX1_N	Y36	
QSFP_TX2_P	T35	
QSFP_TX2_N	T36	
QSFP_TX3_P	V35	
QSFP_TX3_N	V36	
QSFP_TX4_P	R33	
QSFP_TX4_N	R34	
QSFP_RX1_P	R38	
QSFP_RX1_N	R39	
QSFP_RX2_P	W38	
QSFP_RX2_N	W39	
QSFP_RX3_P	U38	
QSFP_RX3_N	U39	
QSFP_RX4_P	AA38	
QSFP_RX4_N	AA39	

Miscellaneous		
URST_B	AN12	USER RESET PUSH BUTTON ACTIVE LOW
CMON_ALERT	AG12	COMMON CURRENT MONITOR ALERT (PL I2C0)

Processing System Signals

MICRO SD (Boot)	
Signal	**Pin**
MIO13_SD0_DQ0	R28
MIO14_SD0_DQ1	P29
MIO15_SD0_DQ2	U28
MIO16_SD0_DQ3	R29
MIO21_SD0_CMD	V29
MIO22_SD0_CLK	Y28
MIO24_SD0_CD_N	Y29
MIO25_SD0_WP_N	W29

Display Port		
Signal	**Pin**	**Notes**
MIO27_DP_AUX_DATA_OUT	C25	
MIO28_DP_HPD	F25	
MIO29_DP_AUX_DATA_OE	B25	
MIO30_DP_AUX_DATA_IN	D25	
DP1_TX_P	AK36	GTR0
DP1_TX_N	AK37	GTR0
DP0_TX_P	AH36	GTR1
DP0_TX_N	AH37	GTR1

UART	
MIO32_UA1_RXD	A26
MIO33_UA1_TXD	A27

OLED		
OLED_SPI_SCLK	W26	MIO6
OLED_SPI_CSN	R27	MIO9
OLED_SPI_MISO	V27	MIO10
OLED_SPI_MOSI	P28	MIO11

Ethernet	
MIO38_GEM1_TX_CLK	E27
MIO39_GEM1_TX_D0	B28
MIO40_GEM1_TX_D1	D26
MIO41_GEM1_TX_D2	C28
MIO42_GEM1_TX_D3	E28
MIO43_GEM1_TX_CTL	D28
MIO44_GEM1_RX_CLK	F27
MIO45_GEM1_RX_D0	G27
MIO46_GEM1_RX_D1	A29
MIO47_GEM1_RX_D2	C29
MIO48_GEM1_RX_D3	D29
MIO49_GEM1_RX_CTL	B29
MIO50_GEM1_MDC	E28
MIO51_GEM1_MDIO	D28
MIO26_ENET_RESET_B	G25

I2C Control/Monitor		
CMON_SCL	Y27	MIO18 I2C0 CURRENT MONITORS
CMON_SDA	Y27	MIO19 I2C0
I2C_SCL1	C27	I2C1 SYZYGY, MAC EEPROM, QSFP
I2C_SDA1	F26	MIO37 I2C1

LEDs		
PS_LED0	V28	
PS_LED1	T29	

Pushbutton		
PS_BTN	U29	

USB3 Slave		
Signal	**Pin**	**Notes**
MIO52_USB0_CLK	N26	
MIO53_USB0_DIR	L25	
MIO54_USB0_D2	M26	
MIO55_USB0_NXT	J25	
MIO56_USB0_D0	L26	
MIO57_USB0_D1	H25	
MIO58_USB0_STP	H26	
MIO59_USB0_D3	H27	
MIO60_USB0_D4	J26	
MIO61_USB0_D5	G28	
MIO62_USB0_D6	K26	
MIO63_USB0_D7	G29	
USB0_US_TX_P	AF36	GTR2
USB0_US_TX_N	AF37	GTR2
USB0_US_RX_P	AE38	GTR2
USB0_US_RX_N	AE39	GTR2
USB3 Host		
MIO64_USB1_CLK	K27	
MIO65_USB1_DIR	L27	
MIO66_USB1_D2	N27	
MIO67_USB1_NXT	J28	
MIO68_USB1_D0	H29	
MIO69_USB1_D1	M27	
MIO70_USB1_STP	K28	
MIO71_USB1_D3	H28	
MIO72_USB1_D4	J29	
MIO73_USB1_D5	K29	
MIO74_USB1_D6	M28	
MIO75_USB1_D7	N28	
MIO76_USB_RESET_B	M29	COMMON TO USB0 AND USB1
MIO77_USB_VBUS_DET	L29	
USB1_US_TX_P	AD36	GTR3
USB1_US_TX_N	AD37	GTR3
USB1_US_RX_P	AC38	GTR3
USB1_US_RX_N	AC39	GTR3

DDR4 Pins for Processing System and Programmable Logic

Signal	Pin Name	PL PIN	PS PIN	IO Standard
DQM0	PL_DDR4_DQM0	J15	AU23	POD12_DCI
DQM1	PL_DDR4_DQM1	N14	AT27	POD12_DCI
DQM2	PL_DDR4_DQM2	D18	AL24	POD12_DCI
DQM3	PL_DDR4_DQM3	G17	AM27	POD12_DCI
DQM4	PL_DDR4_DQM4	F21	AV36	POD12_DCI
DQM5	PL_DDR4_DQM5	J23	AT35	POD12_DCI
DQM6	PL_DDR4_DQM6	C23	AM36	POD12_DCI
DQM7	PL_DDR4_DQM7	N20	AJ32	POD12_DCI
DQ63	PL_DDR4_DQ63	L19	AG30	POD12_DCI
DQ62	PL_DDR4_DQ62	L23	AF32	POD12_DCI
DQ61	PL_DDR4_DQ61	M19	AG32	POD12_DCI
DQ60	PL_DDR4_DQ60	N19	AH30	POD12_DCI
DQ59	PL_DDR4_DQ59	L21	AJ30	POD12_DCI
DQ58	PL_DDR4_DQ58	L22	AJ31	POD12_DCI
DQ57	PL_DDR4_DQ57	L20	AK31	POD12_DCI
DQ56	PL_DDR4_DQ56	M20	AK32	POD12_DCI
DQ55	PL_DDR4_DQ55	B20	AN35	POD12_DCI
DQ54	PL_DDR4_DQ54	C20	AN36	POD12_DCI
DQ53	PL_DDR4_DQ53	A21	AM34	POD12_DCI
DQ52	PL_DDR4_DQ52	C22	AM35	POD12_DCI
DQ51	PL_DDR4_DQ51	A20	AN38	POD12_DCI
DQ50	PL_DDR4_DQ50	B24	AM39	POD12_DCI
DQ49	PL_DDR4_DQ49	A24	AM38	POD12_DCI
DQ48	PL_DDR4_DQ48	C21	AL39	POD12_DCI
DQ47	PL_DDR4_DQ47	H21	AP34	POD12_DCI
DQ46	PL_DDR4_DQ46	H23	AP33	POD12_DCI
DQ45	PL_DDR4_DQ45	H22	AR33	POD12_DCI
DQ44	PL_DDR4_DQ44	L24	AR34	POD12_DCI
DQ43	PL_DDR4_DQ43	G23	AW33	POD12_DCI
DQ42	PL_DDR4_DQ42	K24	AW34	POD12_DCI
DQ41	PL_DDR4_DQ41	G22	AV33	POD12_DCI
DQ40	PL_DDR4_DQ40	J21	AU33	POD12_DCI
DQ39	PL_DDR4_DQ39	G20	AW35	POD12_DCI
DQ38	PL_DDR4_DQ38	F24	AV35	POD12_DCI
DQ37	PL_DDR4_DQ37	F20	AW36	POD12_DCI

Signal	Pin Name	PL PIN	PS PIN	IO Standard
DQ36	PL_DDR4_DQ36	E23	AV38	POD12_DCI
DQ35	PL_DDR4_DQ35	E21	AU35	POD12_DCI
DQ34	PL_DDR4_DQ34	E22	AU37	POD12_DCI
DQ33	PL_DDR4_DQ33	D21	AU38	POD12_DCI
DQ32	PL_DDR4_DQ32	E24	AU39	POD12_DCI
DQ31	PL_DDR4_DQ31	F15	AM28	POD12_DCI
DQ30	PL_DDR4_DQ30	E18	AN28	POD12_DCI
DQ29	PL_DDR4_DQ29	E17	AN26	POD12_DCI
DQ28	PL_DDR4_DQ28	H18	AN27	POD12_DCI
DQ27	PL_DDR4_DQ27	G15	AK27	POD12_DCI
DQ26	PL_DDR4_DQ26	F16	AK28	POD12_DCI
DQ25	PL_DDR4_DQ25	E16	AL25	POD12_DCI
DQ24	PL_DDR4_DQ24	G18	AK26	POD12_DCI
DQ23	PL_DDR4_DQ23	A16	AK23	POD12_DCI
DQ22	PL_DDR4_DQ22	B19	AN23	POD12_DCI
DQ21	PL_DDR4_DQ21	C16	AK24	POD12_DCI
DQ20	PL_DDR4_DQ20	D15	AM25	POD12_DCI
DQ19	PL_DDR4_DQ19	A19	AN25	POD12_DCI
DQ18	PL_DDR4_DQ18	C17	AP23	POD12_DCI
DQ17	PL_DDR4_DQ17	A17	AP24	POD12_DCI
DQ16	PL_DDR4_DQ16	D16	AP25	POD12_DCI
DQ15	PL_DDR4_DQ15	M12	AW26	POD12_DCI
DQ14	PL_DDR4_DQ14	M15	AV27	POD12_DCI
DQ13	PL_DDR4_DQ13	M13	AV26	POD12_DCI
DQ12	PL_DDR4_DQ12	M17	AU27	POD12_DCI
DQ11	PL_DDR4_DQ11	L12	AR27	POD12_DCI
DQ10	PL_DDR4_DQ10	N15	AU25	POD12_DCI
DQ9	PL_DDR4_DQ9	N13	AP26	POD12_DCI
DQ8	PL_DDR4_DQ8	N17	AT25	POD12_DCI
DQ7	PL_DDR4_DQ7	L17	AR23	POD12_DCI
DQ6	PL_DDR4_DQ6	J19	AR24	POD12_DCI
DQ5	PL_DDR4_DQ5	K16	AV22	POD12_DCI
DQ4	PL_DDR4_DQ4	J18	AV23	POD12_DCI
DQ3	PL_DDR4_DQ3	H16	AW23	POD12_DCI
DQ2	PL_DDR4_DQ2	H17	AV25	POD12_DCI
DQ1	PL_DDR4_DQ1	J16	AW24	POD12_DCI
DQ0	PL_DDR4_DQ0	K17	AW25	POD12_DCI

Signal	Pin Name	PL PIN	PS PIN	IO Standard
DQS0_P	PL_DDR4_DQS0_P	K19	AT24	DIFF_POD12_DCI
DQS0_N	PL_DDR4_DQS0_N	K18	AU24	DIFF_POD12_DCI
DQS1_P	PL_DDR4_DQS1_P	L15	AR26	DIFF_POD12_DCI
DQS1_N	PL_DDR4_DQS1_N	L14	AT26	DIFF_POD12_DCI
DQS2_P	PL_DDR4_DQS2_P	B18	AM23	DIFF_POD12_DCI
DQS2_N	PL_DDR4_DQS2_N	B17	AM24	DIFF_POD12_DCI
DQS3_P	PL_DDR4_DQS3_P	G19	AL26	DIFF_POD12_DCI
DQS3_N	PL_DDR4_DQS3_N	F19	AL27	DIFF_POD12_DCI
DQS4_P	PL_DDR4_DQS4_P	D23	AV37	DIFF_POD12_DCI
DQS4_N	PL_DDR4_DQS4_N	D24	AW37	DIFF_POD12_DCI
DQS5_P	PL_DDR4_DQS5_P	J20	AT34	DIFF_POD12_DCI
DQS5_N	PL_DDR4_DQS5_N	H20	AU34	DIFF_POD12_DCI
DQS6_P	PL_DDR4_DQS6_P	B22	AM37	DIFF_POD12_DCI
DQS6_N	PL_DDR4_DQS6_N	A22	AN37	DIFF_POD12_DCI
DQS7_P	PL_DDR4_DQS7_P	K21	AH31	DIFF_POD12_DCI
DQS7_N	PL_DDR4_DQS7_N	K22	AH32	DIFF_POD12_DCI
RAS	PL_DDR4_A16_RAS_N	E13	AP28	SSTL12_DCI
CAS	PL_DDR4_A15_CAS_N	F14	AP30	SSTL12_DCI
WE	PL_DDR4_A14_WE_N	K13	AR28	SSTL12_DCI
A13	PL_DDR4_A13	H11	AU32	SSTL12_DCI
A12	PL_DDR4_A12	D13	AT30	SSTL12_DCI
A11	L_DDR4_A11	G7	AT32	SSTL12_DCI
A10	PL_DDR4_A10	C15	AT31	SSTL12_DCI
A9	L_DDR4_A9	H6	AP29	SSTL12_DCI
A8	PL_DDR4_A8	A11	AM29	SSTL12_DCI
A7	PL_DDR4_A7	H13	AM30	SSTL12_DCI
A6	PL_DDR4_A6	J7	AL29	SSTL12_DCI
A5	PL_DDR4_A5	F11	AU28	SSTL12_DCI
A4	PL_DDR4_A4	D14	AW31	SSTL12_DCI
A3	PL_DDR4_A3	F10	AU29	SSTL12_DCI
A2	PL_DDR4_A2	A14	AV28	SSTL12_DCI
A1	PL_DDR4_A1	G6	AW28	SSTL12_DCI
A0	PL_DDR4_A0	B13	AV31	SSTL12_DCI
BA0	PL_DDR4_BA0	A12	AN30	SSTL12_DCI
BA1	PL_DDR4_BA1	H10	AM32	SSTL12_DCI
BG0	PL_DDR4_BG0	H12	AN32	SSTL12_DCI
CS_N	PL_DDR4_CS_N	E11	AW29	SSTL12_DCI

Signal	Pin Name	PL PIN	PS PIN	IO Standard
ACT_N	PL_DDR4_ACT_N	B14	AL30	SSTL12_DCI
CLKE	PL_DDR4_CLKE	F12	AW30	SSTL12_DCI
ODT	PL_DDR4_ODT	A15	AV32	SSTL12_DCI
RESET_N	PL_DDR4_RAM_RESET_N	E14	AM33	LVCMOS12
PARITY	PL_DDR4_PARITY	**B12***	AN31	LVCMOS12
ALERT	PL_DDR4_ALERT	**G8***	AL32	LVCMOS12
TEN	PL_DDR4_TEN	**E12***	AU30	LVCMOS12
CLK_P	PL_DDR4_CLK_P	J11	AV30	DIFF_SSTL12_DCI
CLK_N	PL_DDR4_CLK_N	J10	AU23	DIFF_SSTL12_DCI
*** Not used in design**				

RF Subsystem Signals

RF Clock Generation and Control		
Signal	**Pin**	**Notes**
RF_PLL_SCLK	R26	MIO0
RF_PLL2_CSB	P26	MIO1
RF_PLL1_CSB	Y26	MIO2
LMK_CSB	T27	MIO3
RF_PLL_SDO	V26	MIO4 (MISO)
RF_PLL_SDI	AA26	MIO5 (MOSI)
LMK_RST	T26	MIO7
LMK_CLK_IN_SEL0	U27	MIO8
LMK_CLK_IN_SEL1	N29	MIO12

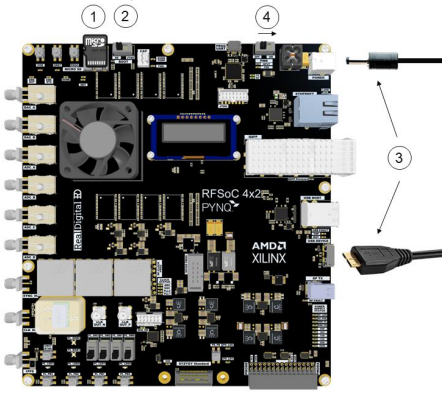
ADC Tile 224 & 226		
ADC_VIN_I23_226_P	AD2	ADC_A (ADC0)
ADC_VIN_I23_226_N	AD1	ADC_A (ADC0)
ADC_VIN_I01_226_P	AF2	ADC_B (ADC1)
ADC_VIN_I01_226_N	AF1	ADC_B (ADC1)
ADC_VIN_I23_224_P	AM1	ADC_C (ADC2)
ADC_VIN_I23_224_N	AM2	ADC_C (ADC2)
ADC_VIN_I01_224_P	AP1	ADC_D (ADC3)
ADC_VIN_I01_224_N	AP2	ADC_D (ADC3)
ADC_224_REFCLK_P	AF5	DEFAULT 491.52 MHz
ADC_224_REFCLK_N	AF4	
ADC_226_REFCLK_P	AB5	DEFAULT 491.52 MHz
ADC_226_REFCLK_N	AB4	

DAC Tile 228 & 230		
DAC_VOUT0_230_P	U2	DAC_A (DAC0)
DAC_VOUT0_230_N	U1	
DAC_VOUT0_228_P	U2	DAC_B (DAC1)
DAC_VOUT0_228_N	U1	
DAC_228_REFCLK_P	R5	DEFAULT 491.520MHz
DAC_228_REFCLK_N	R4	
DAC_230_REFCLK_P	N5	DEFAULT 491.520MHz
DAC_230_REFCLK_N	N4	
DAC_230_SYSREF_P	U5	DEFAULT 7.680MHz
DAC_230_SYSREF_N	U4	

Appendix B. Getting Started card

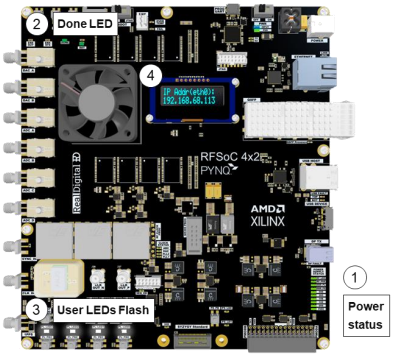
RFSoC 4x2 Quick Start Guide

1. Board Set-Up



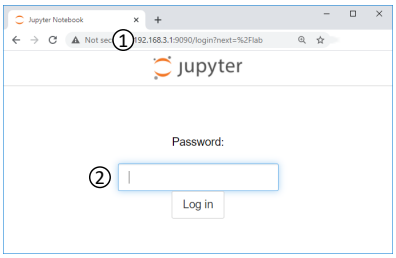
① Insert the SD card.
② Set the boot mode to SD
③ Connect the USB 3 and power cables.
④ Slide power switch to the right to turn on the board.

2. Power-On



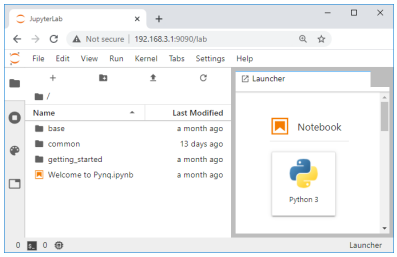
① After power-on, the *power status* LEDs will turn on.
② After ~30 seconds, the **DONE** & **INIT** LEDs will turn on.
③ The 4 white user LEDs will flash briefly and remain on.
④ The LCD will display an IP address

3. Connect to the Board



① On your computer, open a web browser and go to http://192.168.3.1/lab
② Enter *xilinx* as the password and click **Log In**

4. Launch the IDE



You are now in the Jupyter Lab IDE and the PYNQ framework. Use the example notebooks included with PYNQ to start exploring the RFSoC 4x2.

For more detailed instructions on getting started on all supported platforms and for more information, examples and resources see **www.rfsoc-pynq.io**

Appendix C. Major BOM Components

Component	Designator	Manufacturer	PN
OLED Display	DISP1	Newhaven Display	NHD-0216AW-SB3
Fan/heatsink	HS1	Radian Thermal Products	FA40
Voltage Regulator	IC4	Texas Instruments	TL1963A-33DCYR
USB Interface	IC6	FTDI	FT2232HQ-REEL
Oscillator 12MHz	IC10	Microchip	DSC6111CI2A-012.0000T
EEPROM 2K	IC12	Microchip	93LC56BT-I/OT
USB Transceiver (Slave)	IC13, IC20	Microchip Technology	USB3320C-EZK
USB Host PHY	IC16	Microchip Technology	USB5742/2G
Oscillator 25MHz	IC17, IC30	Microchip	DSC6111CI2A-025.0000T
Fuse	IC19, IC21, IC26	Texas Instruments	TPS25200DRV
ADC 8-bit	IC24	Texas Instruments	ADS7885SDBVT
Ethernet PHY	IC29	Texas Instruments	DP83867CRRGZR
Regulator	IC31	Texas Instruments	TPSM82822SILR
Clock Synthesizer	IC32	Silicon Labs	Si5395B-A13886-GM
Crystal	Y2	Connor Winfield	CS-043-048.0M
Clock Synthesizer	IC33	Texas Instruments	LMK04828BISQX/NOPB
Oscillator 160MHz	IC34	Abracon LLC	ABLJO-V-160.000MHZ
Clock Synthesizer	IC37, IC39	Texas Instruments	LMX2594RHAR
ZYNQ RFSoC	IC41	AMD-Xilinx	XCZU48DR-1FFVG1517E
DDR4	IC45 - IC52	Micron Technology Inc.	MT40A512M16LY-062E:E
Regulator	IC53, IC74	Texas Instruments	TPS563240DDCR
Hot swap controller	IC54	Texas Instruments	LM25069PMM-1/NOPB
Regulator	IC59, IC60	Analog Devices Inc.	LTC7150SEY#PBF
Regulator	IC61, IC62, IC64, IC65	Analog Devices Inc.	LTC3636EUFD#PBF
Regulator	IC63, IC68 - IC71	Analog Devices Inc.	ADM7172ACPZ-1.8-R7
Regulator	IC66, IC67	Analog Devices Inc.	ADP1763ACPZ-R7
PMIC	IC72, IC73	Analog Devices Inc.	LTM4632EY#PBF
DAC	IC75	Texas Instruments	DAC101C081CIMK/NOPB
Power Monitor	IC77 - IC85	Texas Instruments	INA220BIDGST
Power sequencer	IC86	Analog Devices Inc.	LTC2937CUHE#PBF
Balun	T1 - T6	MACOM	MABA-011118
Crystal	Y1	TXC CORPORATION	9HT10-32.768KDZF-T
SD Card	NA	SanDisk Class 10 16GByte	SDSDQAD-016G
Power Supply	NA	Power Supply	POSC121000D-C14, 12V/10A

Appendix D. RF-ADC Electrical Characteristics for the ZU48DR

Reprinted from AMD-Xilinx Document DS926 at https://docs.xilinx.com/r/en-US/ds926-zynq-ultrascale-plus-rfsoc

Table 117: **RF-ADC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog inputs					
Resolution		14	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.5	GS/s
	Devices using dual ADC tile channel	1	–	5	GS/s
Full-scale input[3]	Input 100Ω on-die termination when DSA attenuation = 0 dB	–	1	–	V_{PPD}
		–	1	–	dBm
Maximum allowed input power	Input 100Ω on-die termination when DSA attenuation ≥ 15 dB	–	4.8	–	V_{PPD}
		–	14.6	–	dBm
Digital Attenuation Range		0	–	27	dB
Attenuator step size		–	1	–	dB
Auto attenuation	Automatically set when amplitude over-voltage is asserted	–	15	–	dB
Analog input bandwidth[4]	Full-power bandwidth (–3 dB)	–	6	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
Optimized common mode voltage range	Performance optimized range. AC and DC coupling modes[6]	0.68	0.7	0.72	V
Maximum common mode voltage range	Available range before triggering over-voltage protection. AC and DC coupling modes[6]	0.4	0.7	1	V
Crosstalk isolation between channels[7]	F_{IN} = 0–4 GHz	–	–75	–	dBc
	F_{IN} = 0–6 GHz	–	–70	–	dBc

Notes:

1. Analog inputs at –1 dBFS, unless otherwise noted in the test conditions.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. Full scale range is defined as the approximate input power required to drive the ADC to full scale output for a 5 MHz input tone. The full scale range can vary from dual to quad ADCs. It is also subject to variation across process, voltage, and temperature and from package types. The typical average value is provided.
4. ADC bandwidth is defined as the RF input bandwidth, or where the input amplitude response drops 3 dB relative to a low-frequency reference point of 100 MHz.
5. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details because input characteristics depend on channel and package selection. The RL reference plan is close to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
6. When using DC coupling mode, use the VCM output pin to bias the input to the RF-ADC.
7. Values represent two channel crosstalk worst-case values for any combination of channel selections. This specification is only characterized on the XCZU46DR-H1760.

Appendix E. RF-DAC Electrical Characteristics for the ZU48DR

Reprinted from AMD-Xilinx Document DS926 at https://docs.xilinx.com/r/en-US/ds926-zynq-ultrascale-plus-rfsoc

Table 132: **RF-DAC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample rate[3]	-2E, -2I, -2LI speed grade without clock forwarding, datapath modes 2, 3, and 4	0.5	–	9.85	GS/s
	-2E, -2I, -2LI speed grade with clock forwarding, datapath modes 2, 3, and 4	0.5	–	9.70	GS/s
	-1E, -1I, -1LI, -1M speed grade, datapath modes 2, 3, and 4	0.5	–	8.92	GS/s
	All speed grades, datapath mode 1	0.5	–	7.0	GS/s
Maximum output power	V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	–18.5	–	6.5	dBm
Output current range	AC coupling: V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	2.25	–	40.5	mA
	DC coupling: V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	6.4	–	32	mA
Variable output current step size		–	43.75	–	µA
Variable output power range Equivalent dynamic range from output current range[4]	At 240 MHz	24	–	–	dB
	At 3500 MHz	20	–	–	dB
	At 4900 MHz	18	–	–	dB
	At 5900 MHz	17	–	–	dB
Analog bandwidth	Full power bandwidth (–3 dB)	–	6	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
On-die termination	Single-ended on-die termination to external 3V V_{DAC_AVTT}	–	50	–	Ω
Crosstalk isolation between channels[6]	F_{OUT} = 0–4 GHz	–	–75	–	dBc
	F_{OUT} = 0–6 GHz	–	–70	–	dBc

Notes:

1. RF-DAC sampling rate is the highest rate using external sampling clock.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. See the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for additional information on datapath modes.
4. The variable output power effective dynamic range depends on the signal frequency that is shown in the equivalent dynamic range. The specification is supplied for AC coupling mode. A derating of 12 dB is applied for DC coupling mode.
5. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details as input characteristics depend on channel and package selection. The RL reference plan is closed to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
6. Values represent two channel crosstalk worst-case values for any combination of channel selections. This specification is only characterized on XCZU46DR-H1760.