Digital Logic Problem Set #10

Revision: August 5, 2025

1. (8 points) Sketch a block diagram for a 4-bit ALU built from bit-slice ALU circuits that can implement the functions shown in the table. (Note: You don't need to sketch the circuits inside the bit-slice module, but rather a circuit that uses the bit-slices as blocks). Label all signals. Recall that inputs to the bit slices must come from the A and B input busses as well as from neighboring bit slices, and outputs from the slices must drive the F output bus as well as neighboring bit slices. To design the signals that communicate information between slices, you must understand the ALU operations and the implications for information transfer (e.g., does the operation A PLUS B require that information be transferred between slices? If so, what? Does the operation A OR B require that information be transferred?).

Operation Code	ALU function
000	A PLUS B
001	A PLUS 1
010	A MINUS B
011	A MINUS 1
100	A XOR B
101	A'
110	A OR B
111	A AND B

2. (8 points) The ALU operation table from the module has been reproduced below, but opcode 3 has been redefined as "decrement". Complete the F and Cout table entries to define the decrement logic functions.

Op Code	Function	F	Cout
000	A + B	A **xor** B **xor** Cin	(A **and** B) **or** (Cin **and** (A **xor** B))
001	Inc A	A **xor** Cin	A **and** Cin
010	A - B	A **xor** B **xor** Cin	(A' **and** B) **or** (Cin **and** (A **xor** B)')
011	Dec A		
100	A XOR B	A **xor** B	0
101	A'	A'	0
110	A OR B	A **or** B	0
111	A AND B	A **and** B	0

3. (8 points) Sketch a circuit for one ALU bit slice.