Problem Set #7

RealDigital

1. (24 points) Sketch circuits for the NAND and NOR basic cells, and label the S and R inputs and Q output (and be sure the output Q comes from the proper gate – either the gate driven by Set or the gate driven by reset – it will only work properly if Q comes from the right gate). Then sketch their respective block diagrams (being sure to show bubbles on inputs that are asserted low), and complete the truth tables to document their operation.

NAND Basic Cell Circuit

NAND Cell Block Diagram

S	R	Q
0	0	
0	1	
1	0	
1	1	

NAND Cell Truth Table

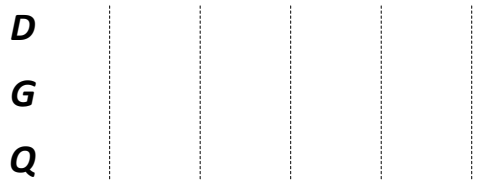
NOR Basic Cell Circuit

NOR Cell Block Diagram

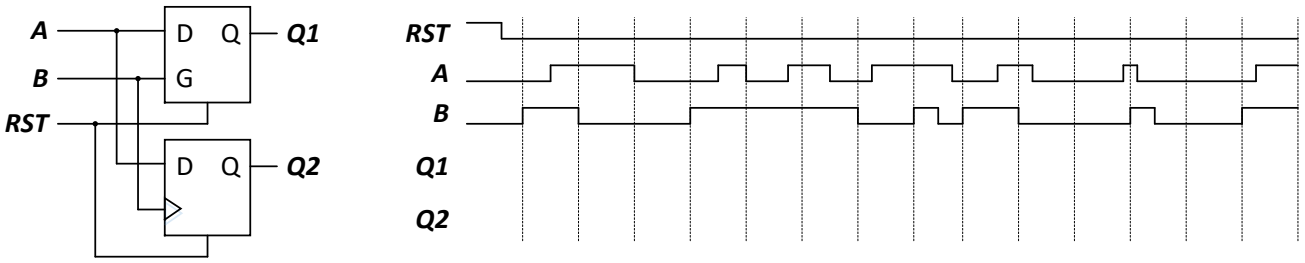
S	R	Q
0	0	
0	1	
1	0	
1	1	

NOR Cell Truth Table

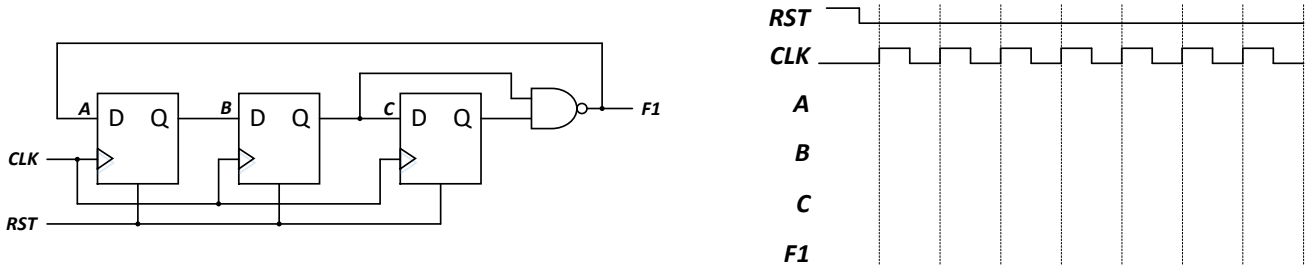
2. (10 points) Sketch the circuit for a D latch based on a NAND basic cell, and then sketch a timing diagram to illustrate its function. Be sure to illustrate all the important states in your timing diagram (hint: there are four).



3. (12 points) Complete the timing diagrams to document the behavior of a D-latch and a D-flip-flop.



4. (12 points) Complete the timing diagram to show the time course for circuit nodes A, B, C, and F1.



5. (16 points) Simulate the Following Sequence shown in the table below (Requirement 3 in Project 7: SR-Latches and D-Latch) and fill out the table below by writing the corresponding letters to empty columns based on your simulation.

A. Set operation
B. Reset operation
C. Confounded outputs (both outputs at the same voltage)
D. Storing a value in memory
E. A metastable state

Time	Set	Reset	NAND Cell	NOR Cell
100ns	1→0	1→1		
200ns	0→1	1→0		
300ns	1→1	0→1		
400ns	1→0	1→0		
500ns	0→1	0→1		
600ns	1→0	1→0		
700ns	0→0	0→1		
800ns	0→1	1→0		