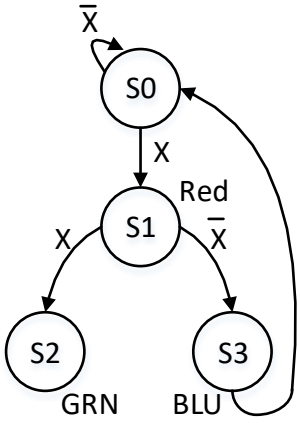
Digital Logic Problem Set #12

Revision: August 5, 2025

1. (16 points) A simple state machine must assert three outputs (R, G, B) in sequence for 333ms each. An input signal called “Start” is driven by a pushbutton. Sketch a state machine that can output the required sequence of signals (R, G, and B) once each time the button is pressed. You have a 3Hz clock and a 1KHz clock to work with. The push button can bounce for up to 2ms on any transition. *(Hint: You can use two state machines).*

2. (8 points) A state machine receives an input X that is synchronous with the system clock. If X is a 1, then the machine must output a signal RED for one clock cycle. Then, if X is still asserted, the machine must output a signal GRN for one clock cycle, but if X is not asserted, the machine must assert an output called BLU. The state diagram below meets these requirements. Can you sketch a machine that can meet these same requirements, but that uses just one flip-flop?



3. (6 points) Sketch a block diagram and state diagram for the button debouncing state machine from design requirement #1.

4. (15 points) Sketch a detailed block diagram for the reaction time monitoring system, showing all the major blocks and interconnections between the major blocks. Provide names for all blocks and all signals.