Digital Logic Problem Set #6

Revision: August 5, 2025

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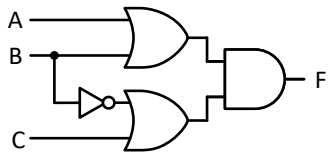
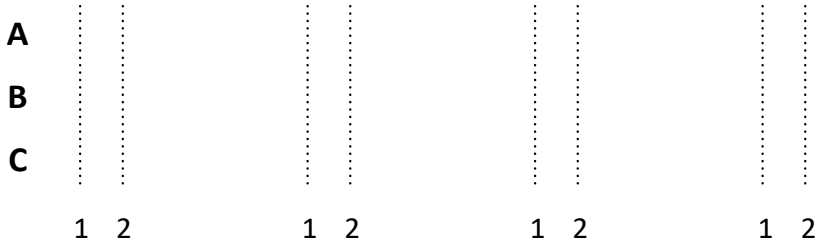
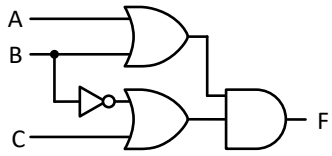
1. (8 points) Complete a timing diagram to show how a glitch might form in the SOP circuit below. Note the pairs dotted lines in the timing diagram – you should show signal changes on the left line (labelled '1'), and assume the time between the dotted lines is the delay for ALL gates (not just the inverter). You don't need to use all the dotted lines – just use enough of the timing diagram to clearly show the glitch.

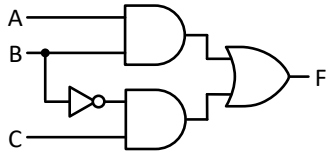


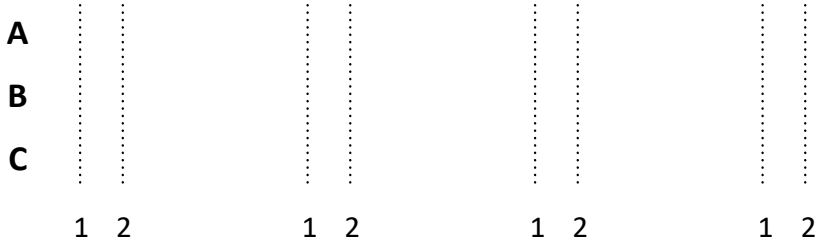


2. (4 points) The circuit above is copied below – sketch a modification to the circuit below to demonstrate how the potential for a glitch can be removed.

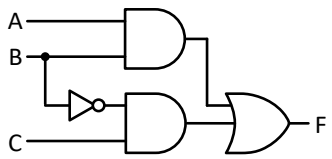


3. (8 points) Complete a timing diagram to show how a glitch might form in the POS circuit below. As before, show signal changes on the left line (labelled '1'), and assume the time between the dotted lines is the delay for ALL gates (not just the inverter). You don't need to use all the dotted lines – just use enough of the timing diagram to clearly show the glitch.





4. (4 points) The circuit above is copied below – sketch a modification to the circuit below to demonstrate how the potential for a glitch can be removed.



5. (8 points) Add any needed logic term(s) to the equations below to remove the possibility of a glitch.

$X <= A \cdot \overline{B} + \overline{A} \cdot C + B \cdot \overline{C}$

$Y <= (\overline{A}+B) \cdot (A+\overline{C}) \cdot (\overline{B}+C)$