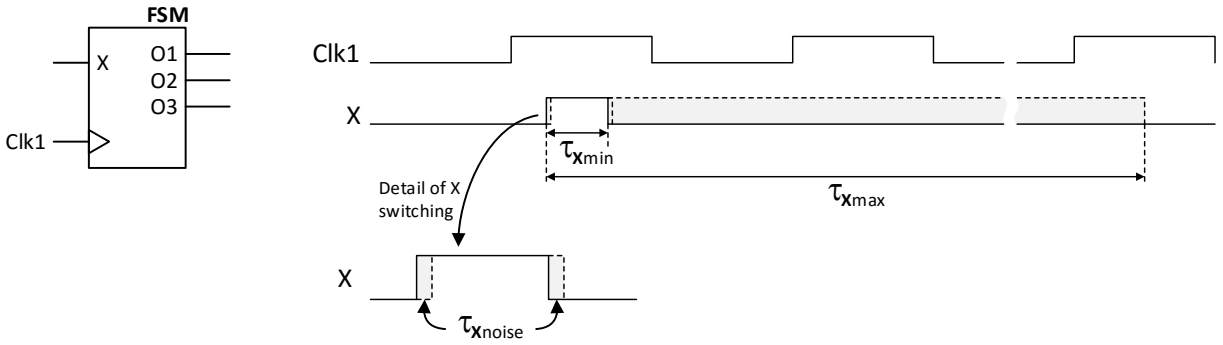
Digital Systems Problem Set #3

Revision: 9/18/19

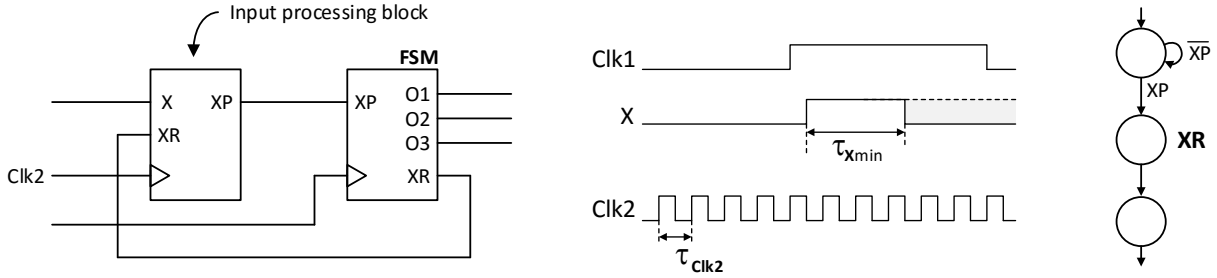
RealDigital

You are tasked with designing a state machine that receives a single input X and clock signal Clk1, and produces three outputs O1, O2, and O3. The input X is from an unknown clock domain; it may bounce or have glitches for up to time τ_{Xnoise}; it may be asserted for a time τ_{Xmin} that is shorter than the Clk1 period; and it may be asserted for a time τ_{Xmax} that is indeterminate.



You decide to add an input processing block that uses a new clock (Clk2) that has a period less than τ_{Xmin} but greater than time τ_{Xnoise} (Clk2 can be used to sample X, because at least one rising edge will occur during the time X is asserted, and it will filter out the logic/switching noise). But because τ_{Xmax} isn't specified, there could be any number of rising edges on Clk2 during the time X is asserted.

The signal XP should be asserted long enough to ensure the FSM receives it, and it should be de-asserted after the FSM has received it, so that the FSM only responds once for each assertion of X, regardless of how long it is asserted. To accommodate dealing with X appropriately, you decide to modify FSM by adding a feedback signal XR that will be asserted on the next rising edge of Clk1 after the "processed X" signal XP has been received.



1. (16 points) Sketch a state diagram for the input processing block that meets all the requirements.

2. (4 points) Can the output XR be generated as a Mealy/conditional output? Briefly explain your answer.