

# AUP-ZU3

Variant: Prototype

4/28/2026  
V4I2

# RELEASED

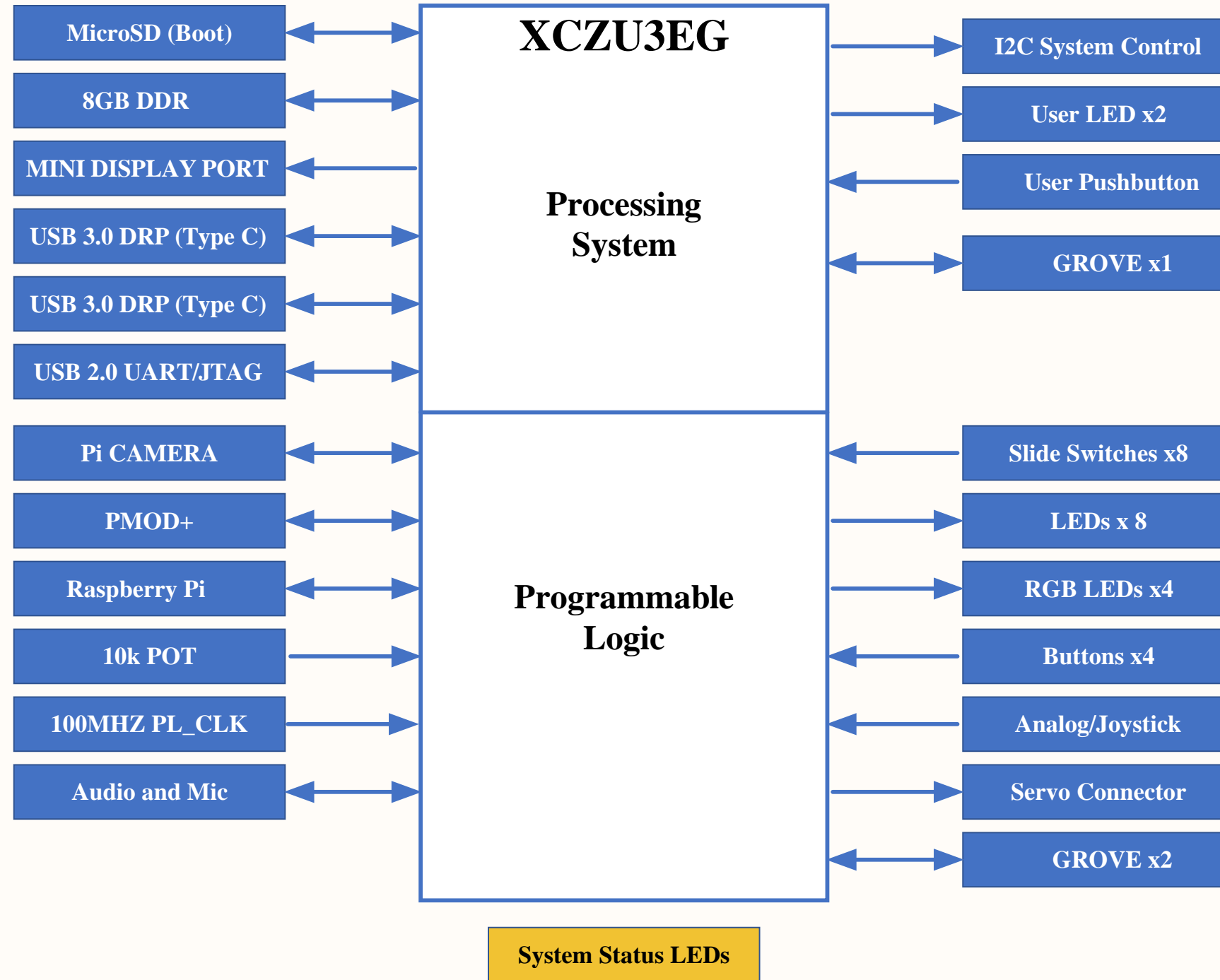
Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	13	SD CARD	25	FAN CONTROLLER	37	.....
2	BLOCK DIAGRAM	14	CLOCK	26	PWR I	38	.....
3	POWER DIAGRAM	15	MPSoC CONFIG	27	PWR II	39	.....
4	USER IO, LEDs	16	PS 500-502	28	PWR III	40	.....
5	PMOD HEADERS	17	PS 504	29	MECH AND PWR SEQUENCING	41	.....
6	CAMERA AND RPI	18	PS MGT	30	DOC REVISION HISTORY	42	.....
7	AUDIO AND MIC	19	PL BANKS 43-46	31	.....	43	.....
8	ANALOG AND SERVO	20	PL BANKS 64-66	32	.....	44	.....
9	DISPLAY PORT	21	MPSoC PWR AND GND PINS	33	.....	45	.....
10	USB-JTAG, USB-UART	22	MSoC DECOUPLING	34	.....	46	.....
11	USB 3.0 DRP I	23	DDR4 MEMORY PS I	35	.....	47	.....
12	USB 3.0 DRP II	24	DDR4 MEMORY PS II	36	.....	48	.....

DISCLAIMER:



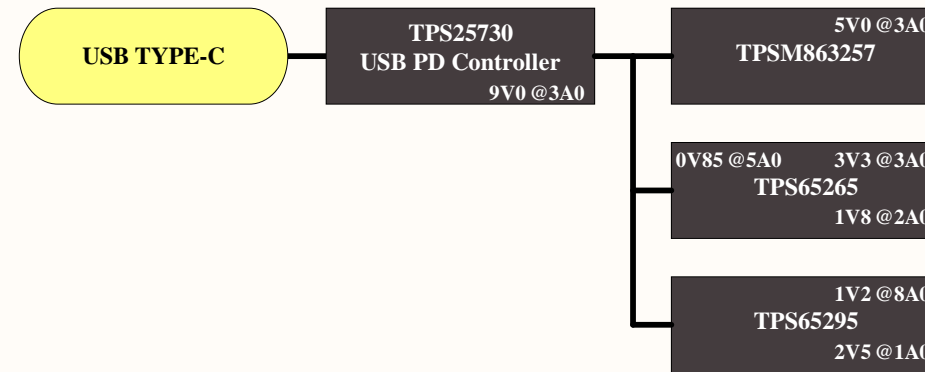
<b>REAL DIGITAL</b>		© Real Digital 2024	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [01] - COVER PAGE.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V4I2	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 1 of 30	

# AUP-ZU3 (Block Diagram)

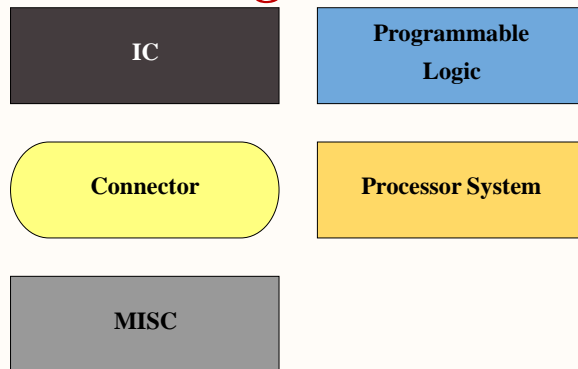


<b>REAL DIGITAL</b>		© Real Digital 2024	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [02] - BLOCK DIAGRAM.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V412	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 2 <i>of</i> 30	

# AUP-ZU3 (Power Diagram)



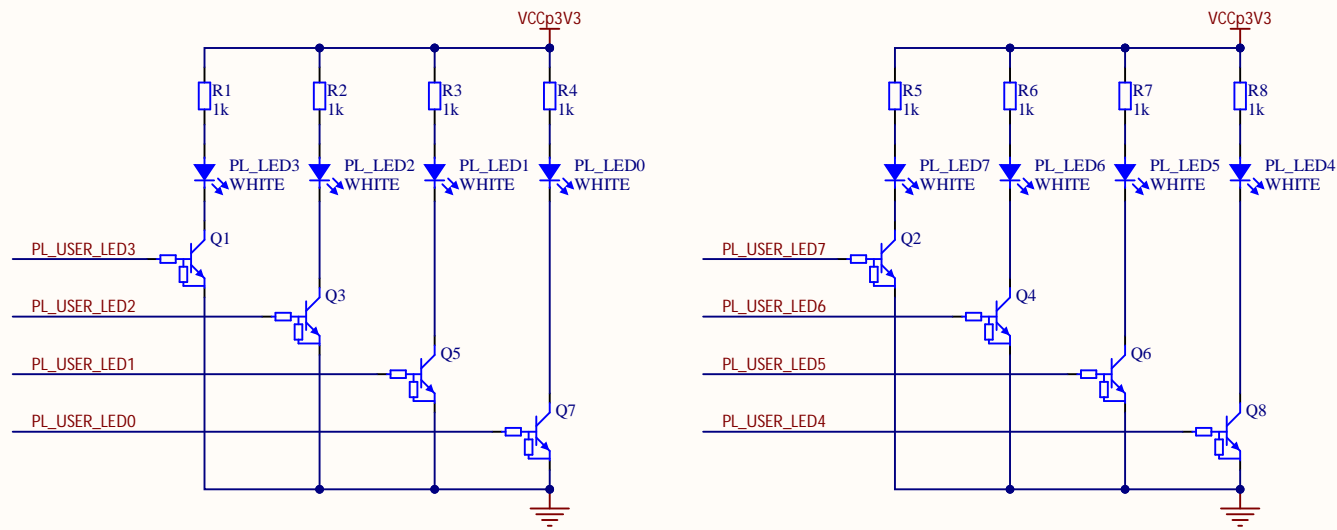
## Legend



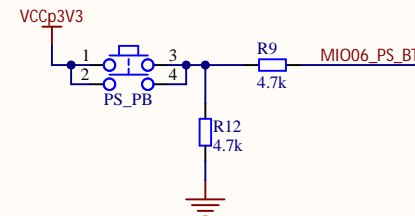
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [03] - POWER DIAGRAM.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V4I2	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 3 <i>of</i> 30	

# USER IO, LEDs

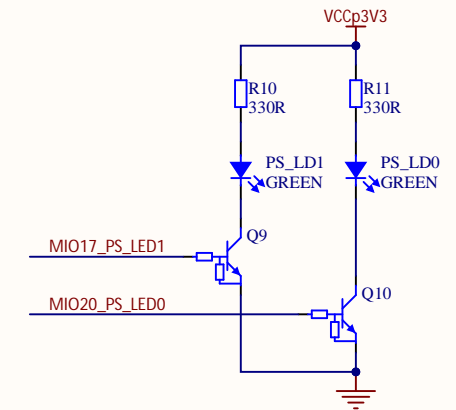
## PL user-defined white LEDs



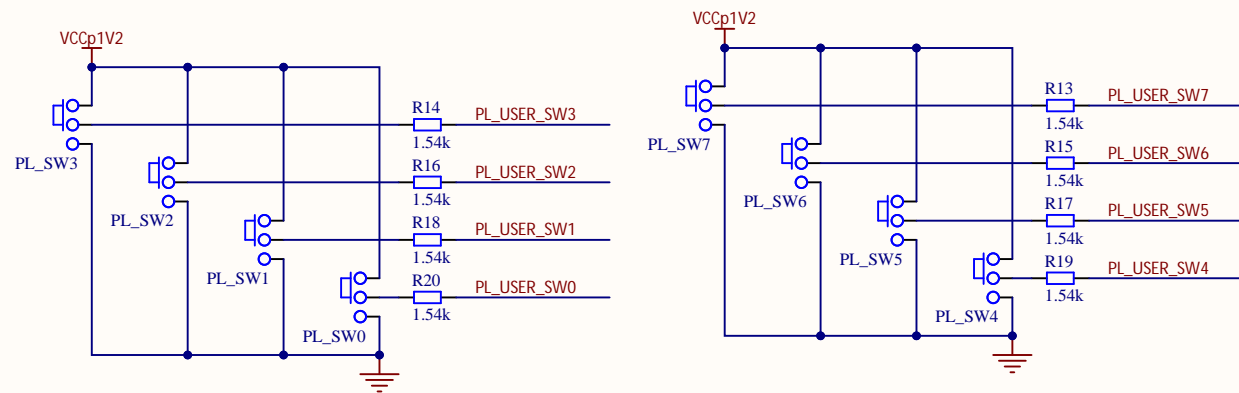
## PS user-defined pushbutton



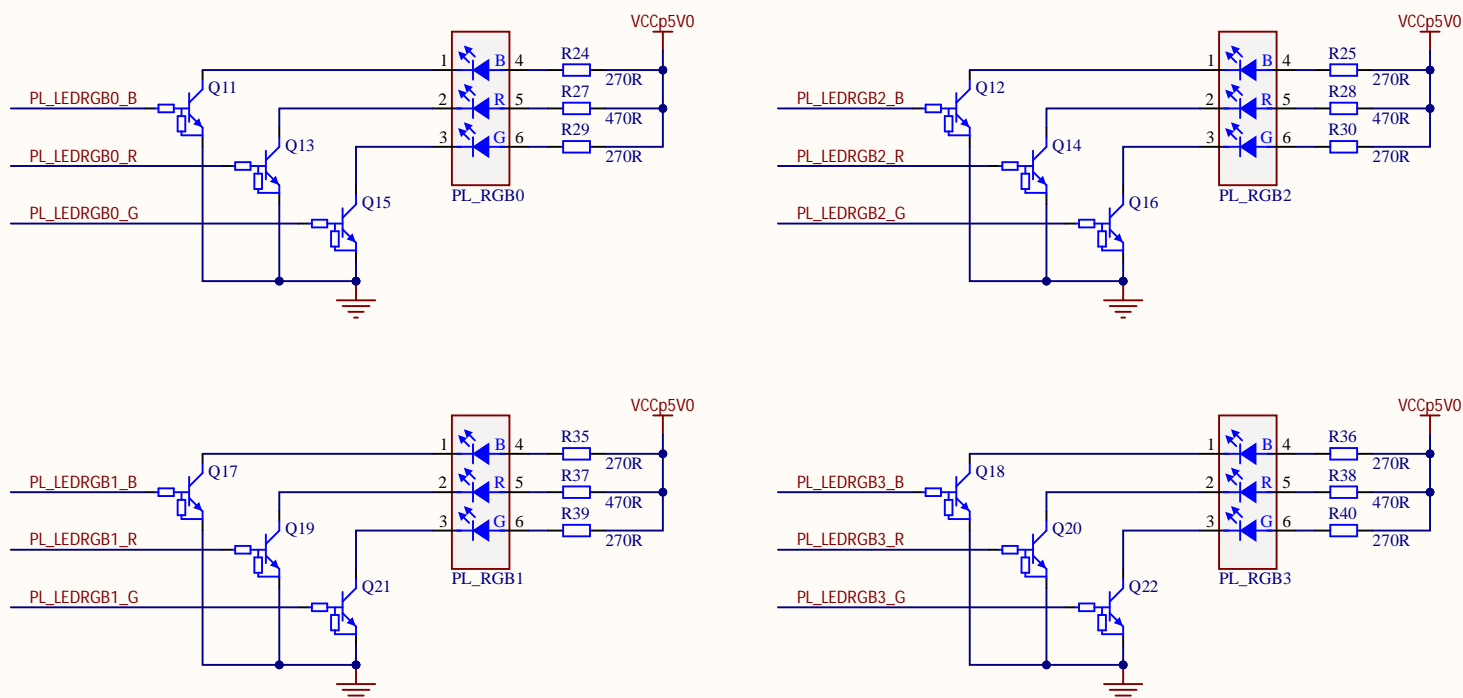
## PS user-defined green LEDs



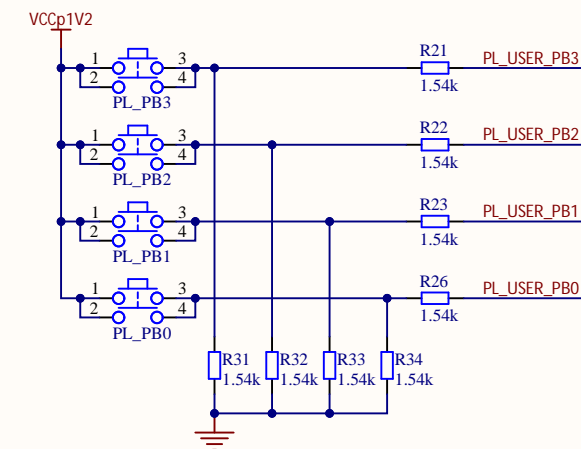
## PL user-defined switches



## PL user-defined RGB LEDs



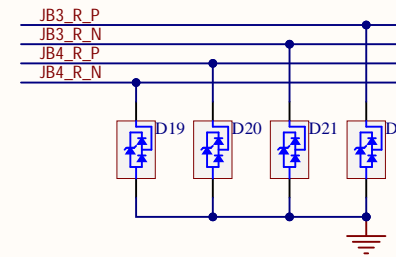
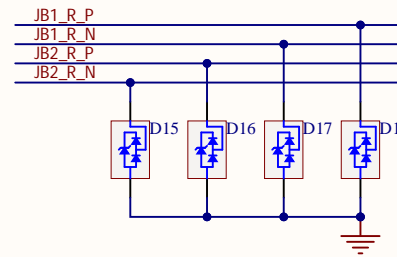
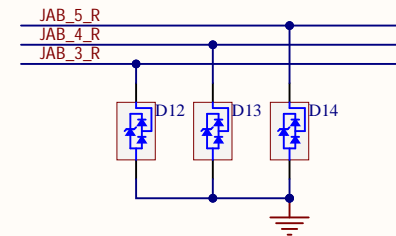
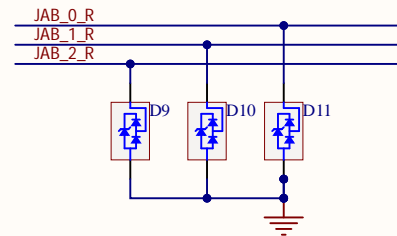
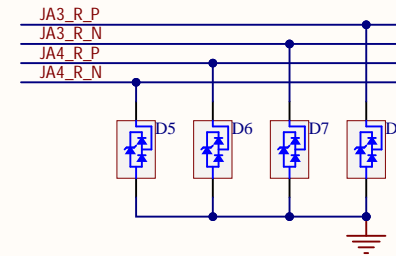
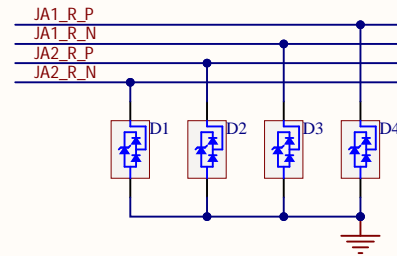
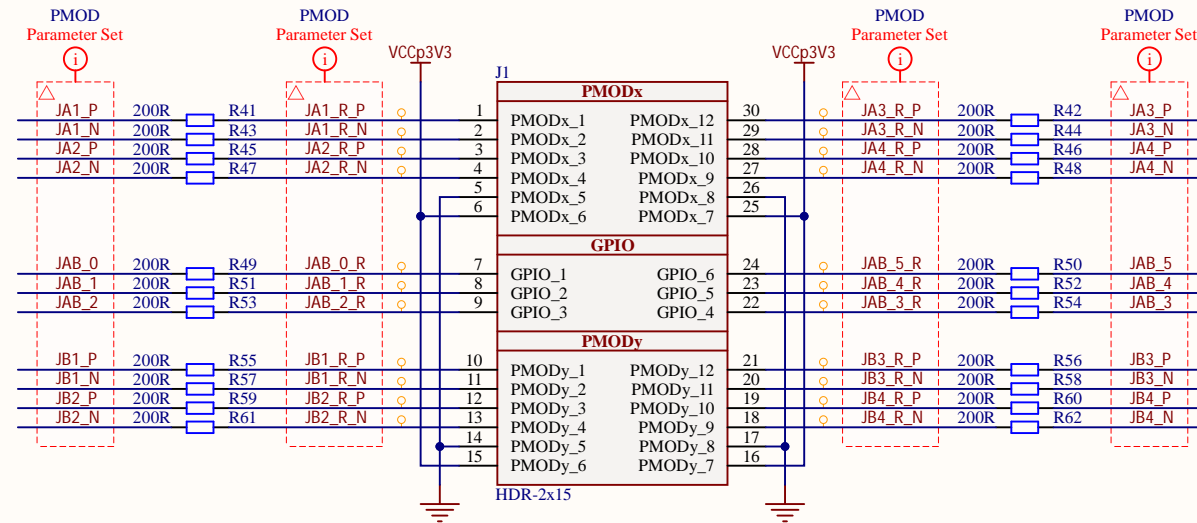
## PL user-defined pushbuttons



<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [04] - USER IO, LEDs.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 4 of 30	

# PMOD HEADERS

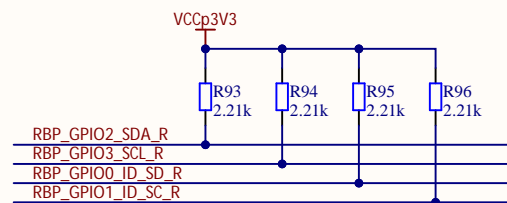
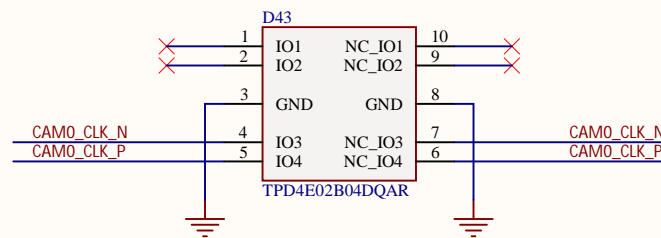
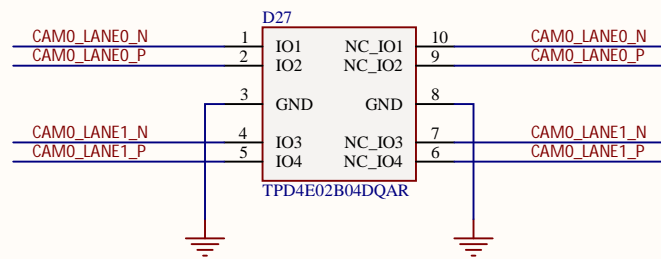
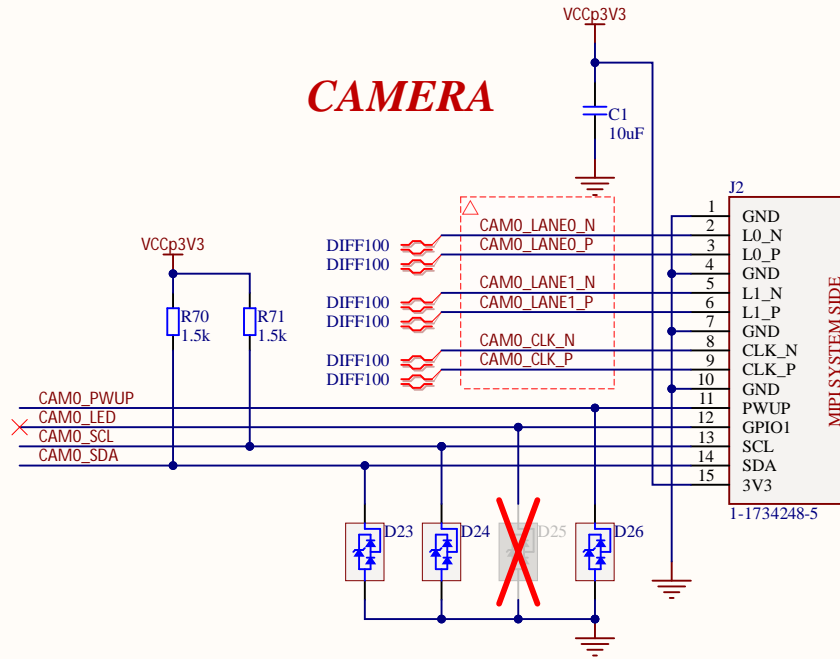
## PMOD A and B



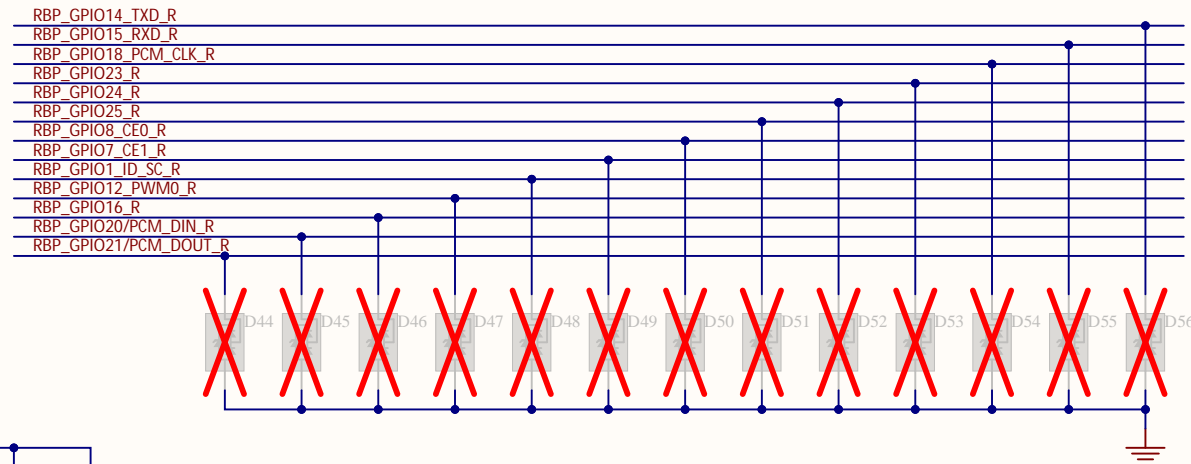
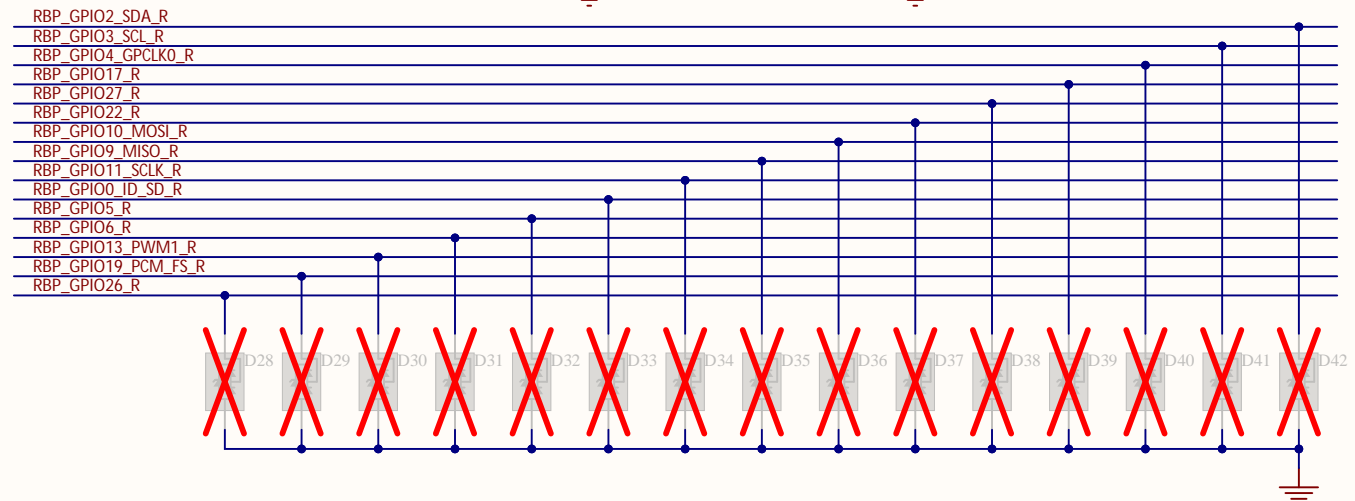
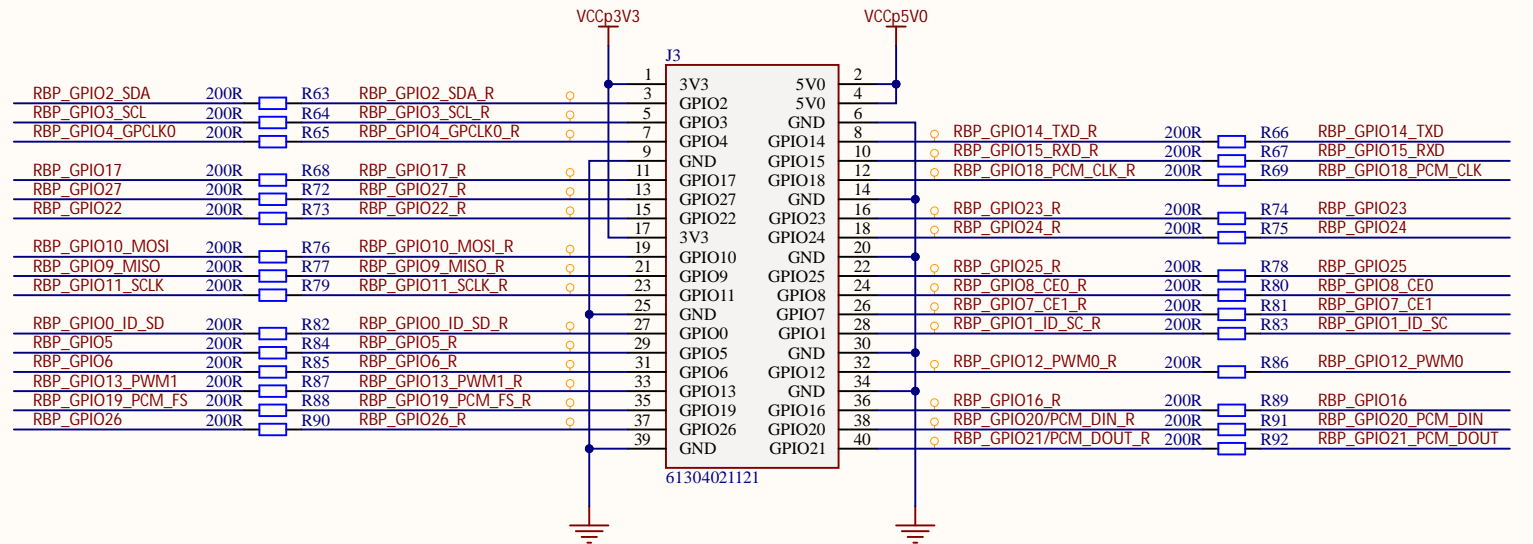
REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [05] - PMOD HEADERS.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 5 of 30	

# CAMERA AND RPI

## CAMERA

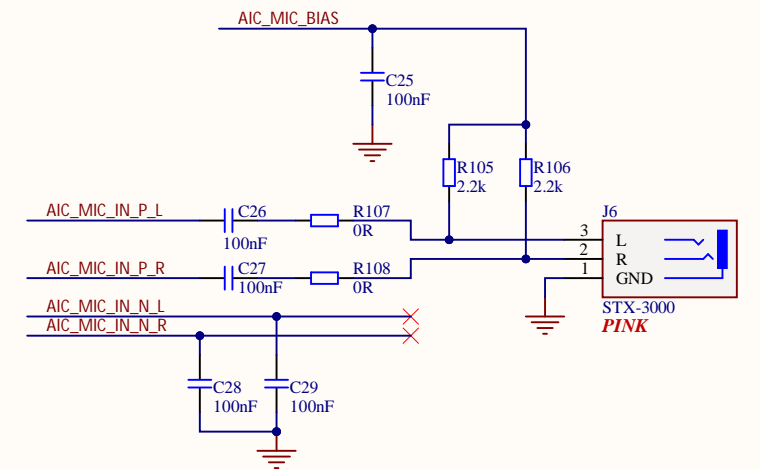
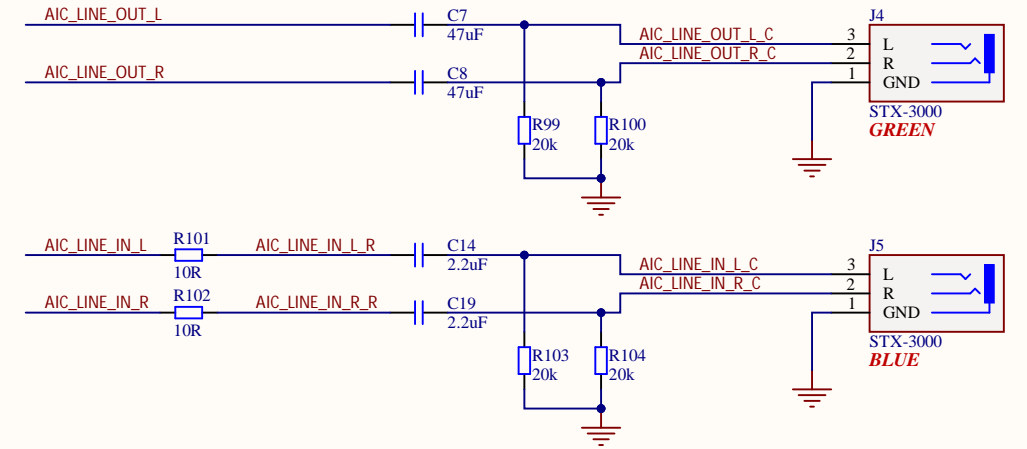
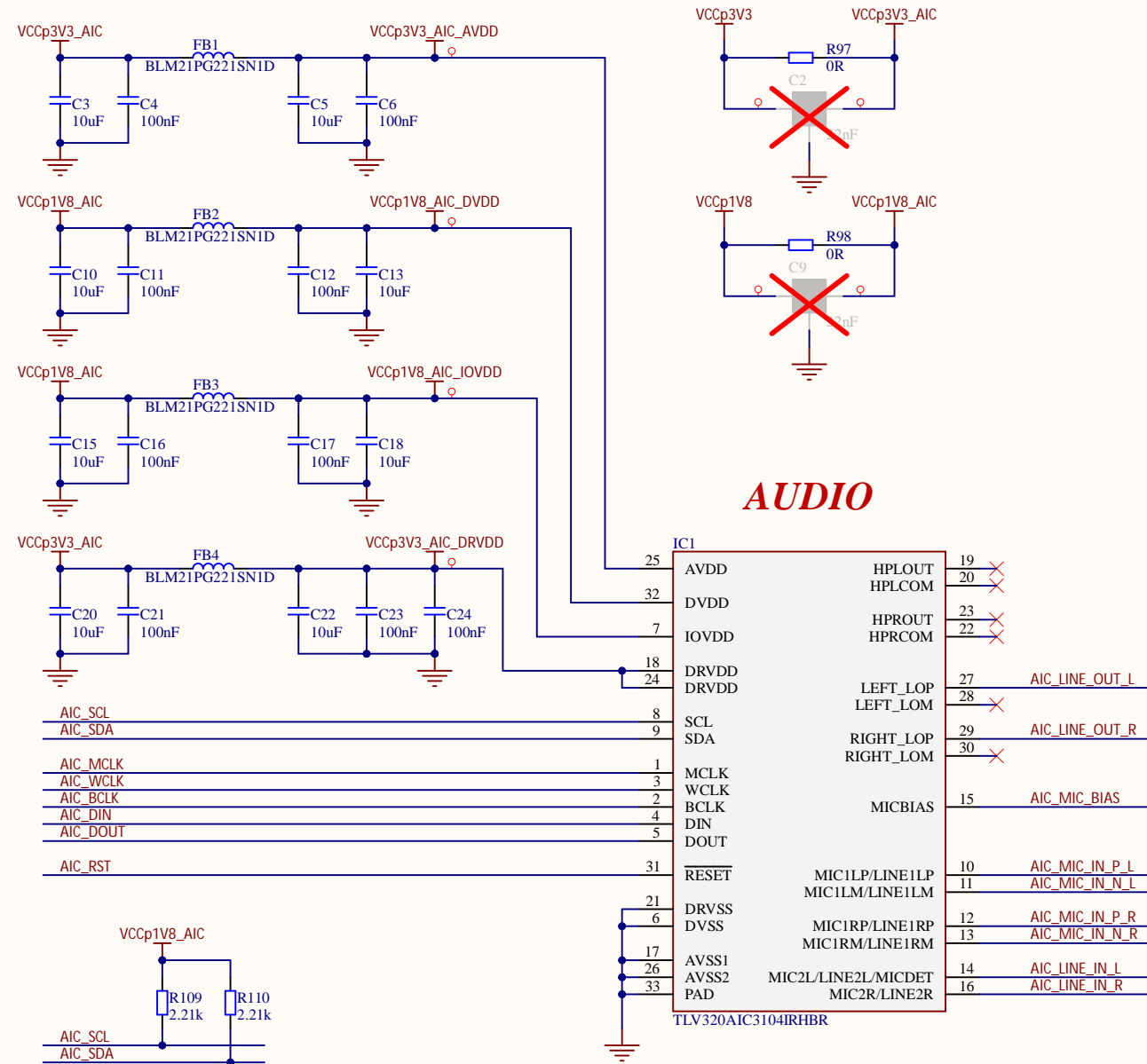


## RASPBERRY Pi HAT EXTENSION



REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [06] - CAMERA AND RPI.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 6 of 30	

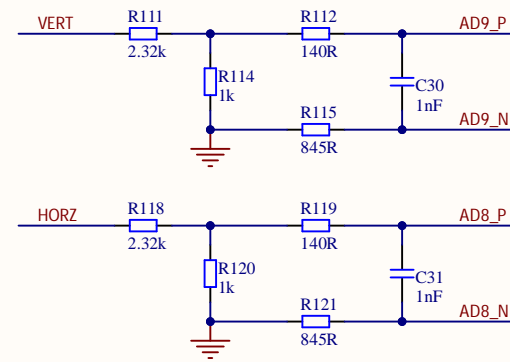
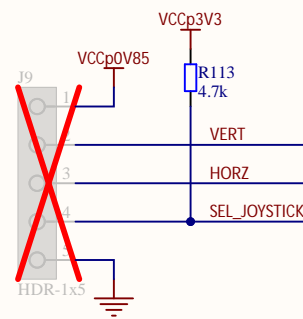
# AUDIO AND MIC



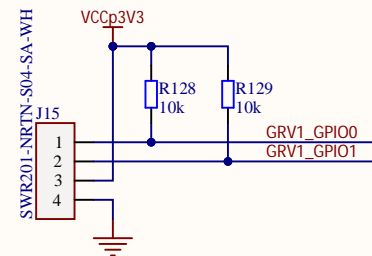
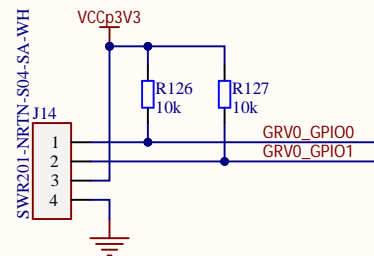
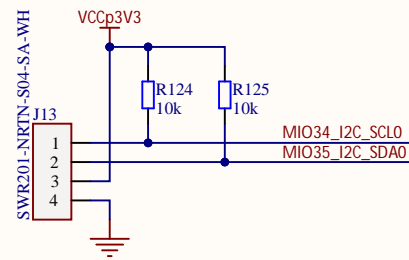
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [07] - AUDIO AND MIC.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 7 of 30	

# ANALOG AND SERVO

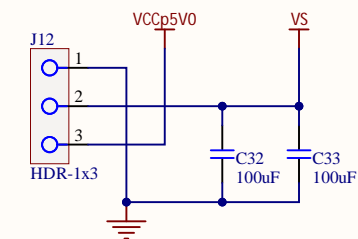
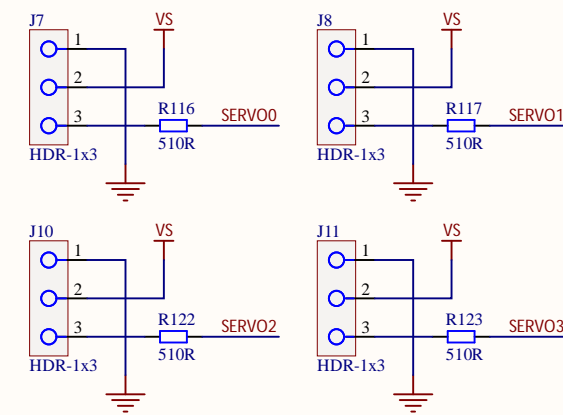
## JOYSTICK



## GROVE

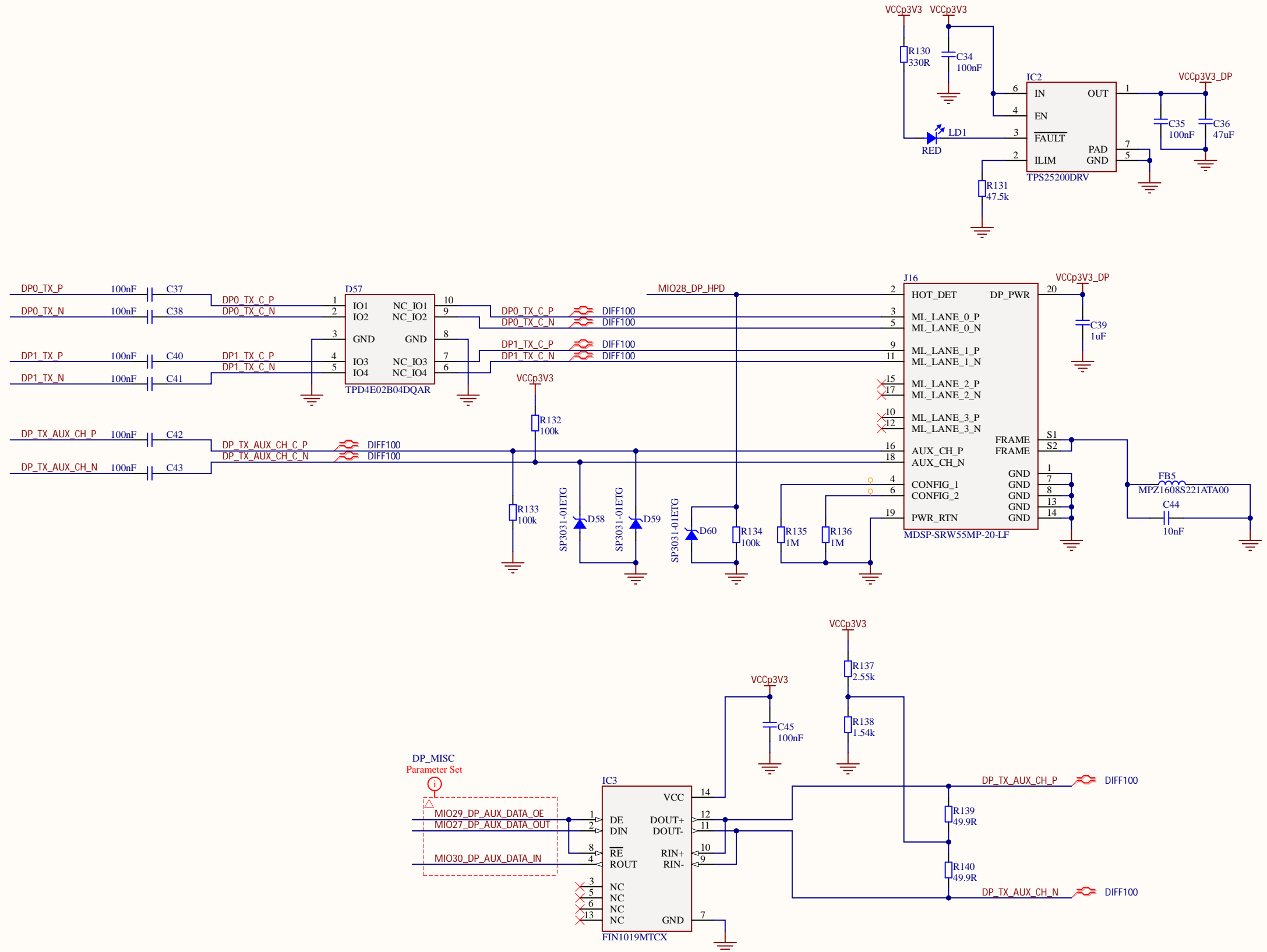


## SERVO



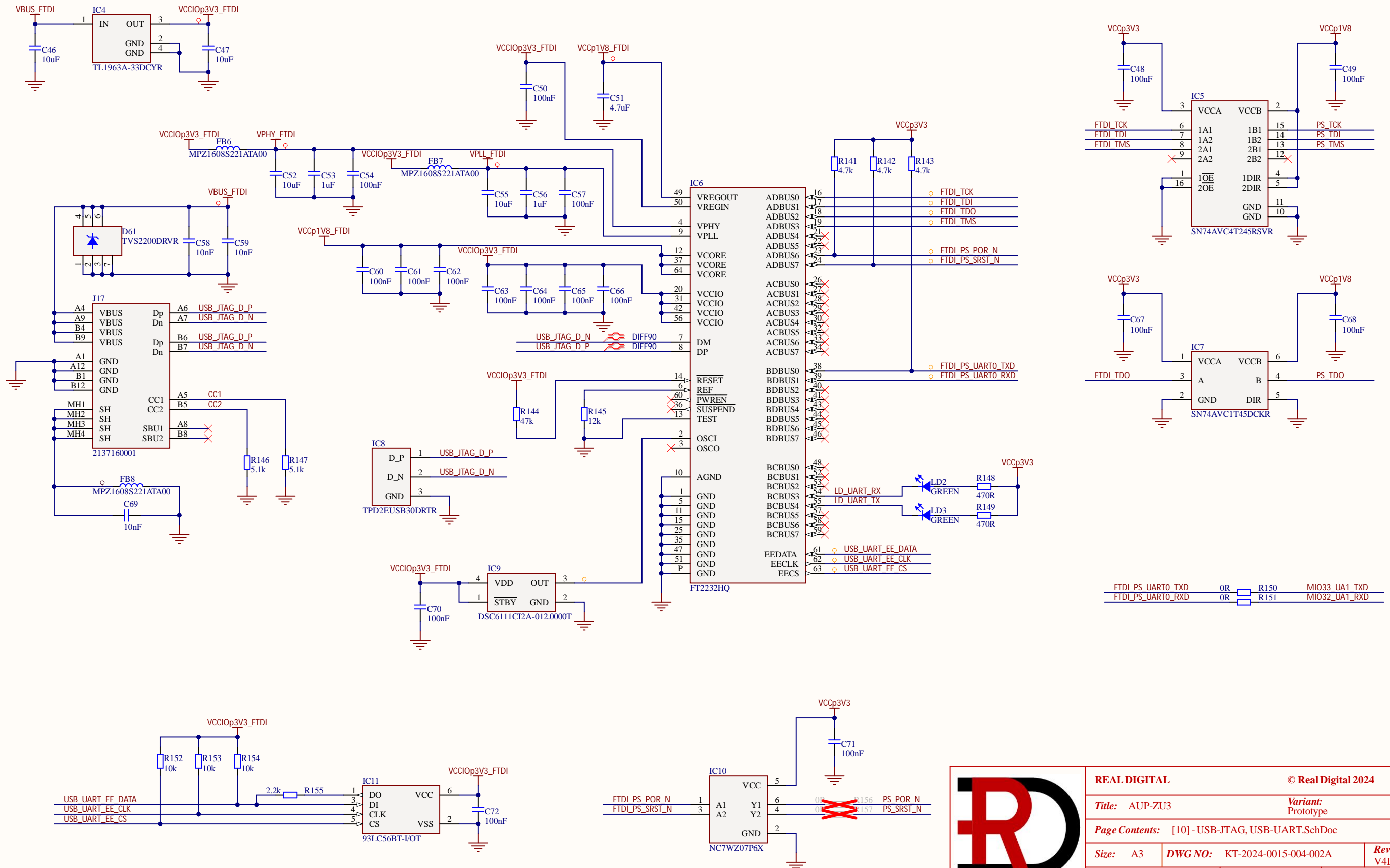
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [08] - ANALOG AND SERVO.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V4I2	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 8 <i>of</i> 30	

# DISPLAY PORT



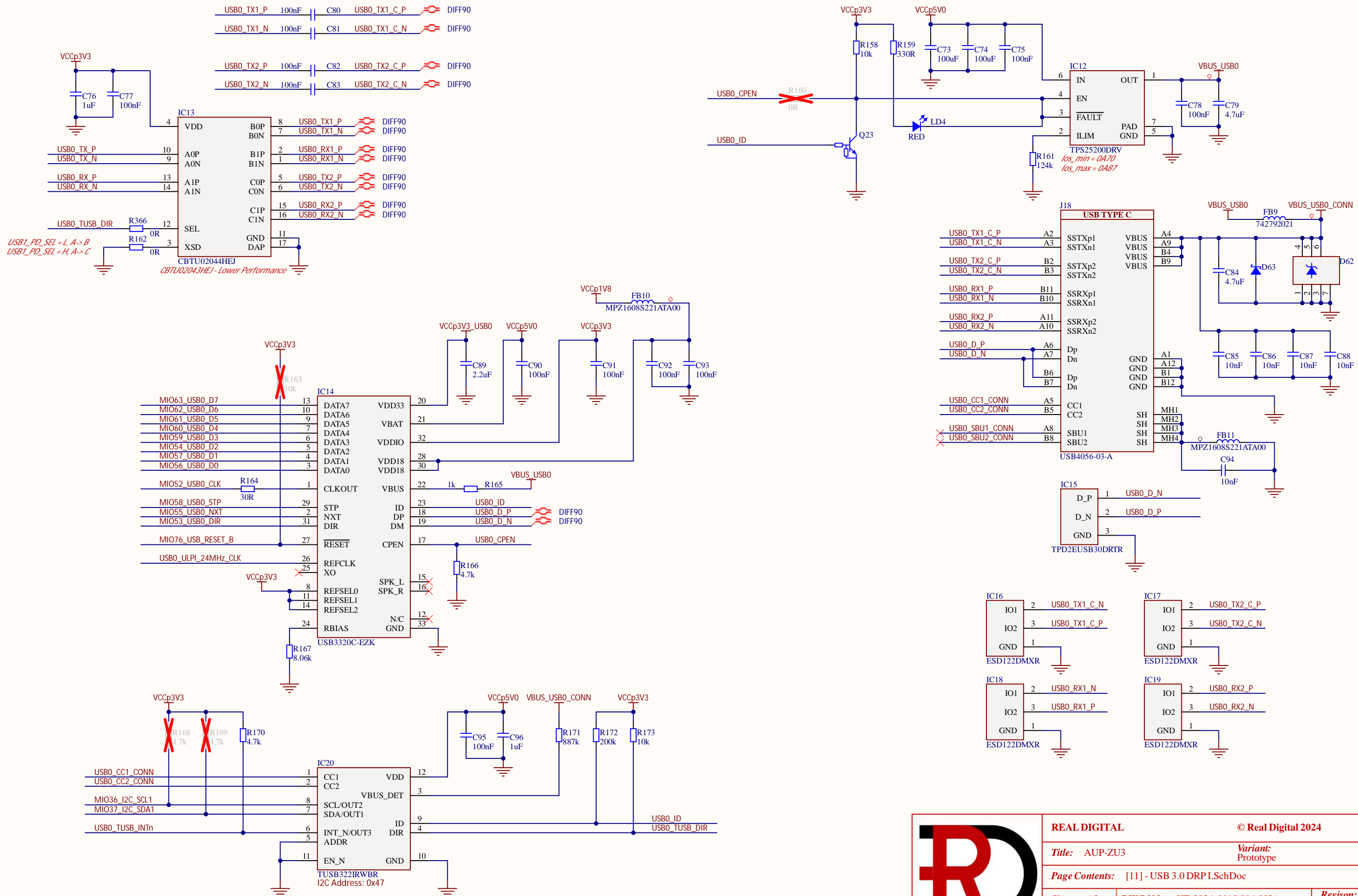
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [09] - DISPLAY PORT.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 9 of 30	

# USB-JTAG, USB-UART



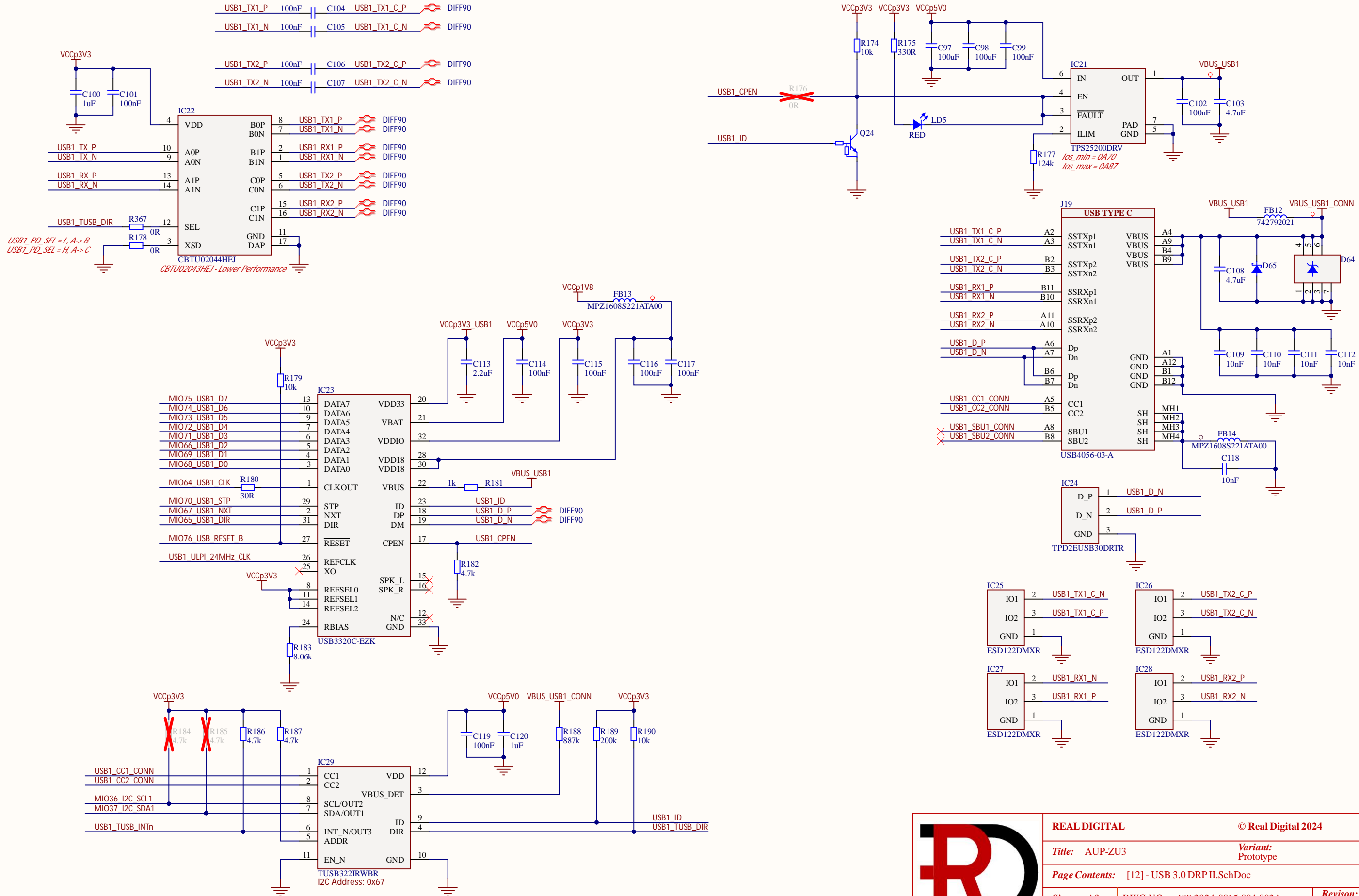
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [10] - USB-JTAG, USB-UART.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 10 of 30	

# USB 3.0 DRP I



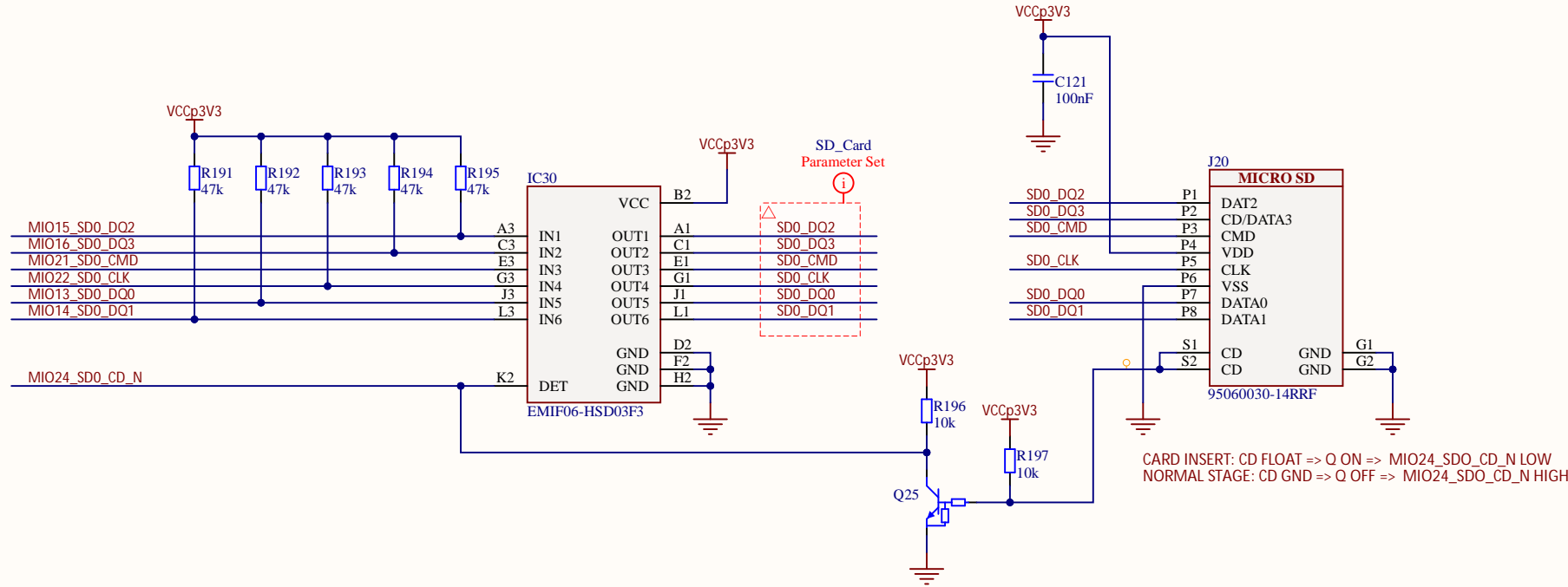
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [11] - USB 3.0 DRP I.Sch.Doc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 11 of 30	

# USB 3.0 DRP II



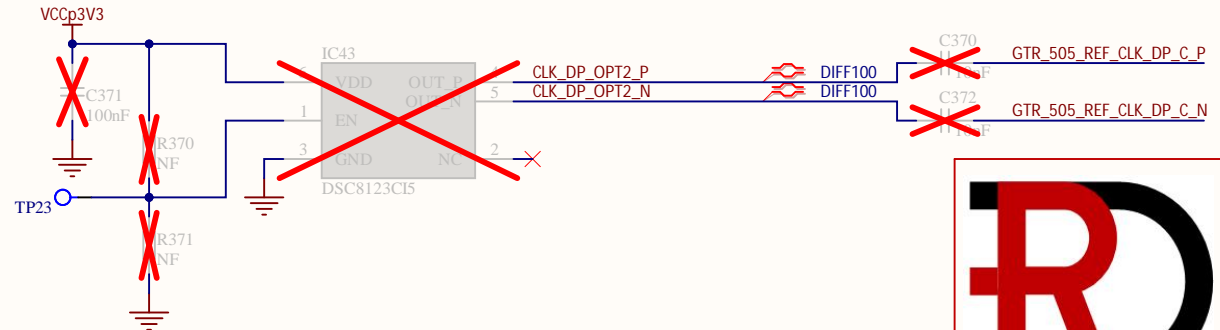
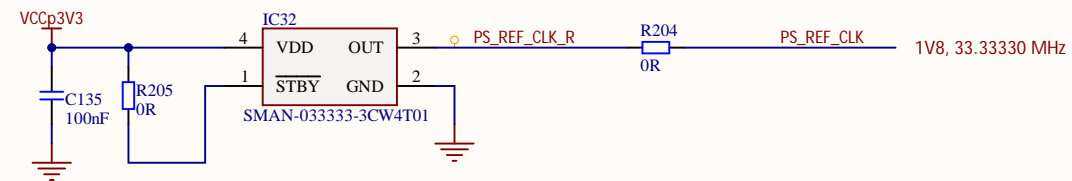
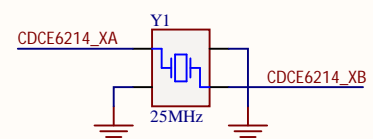
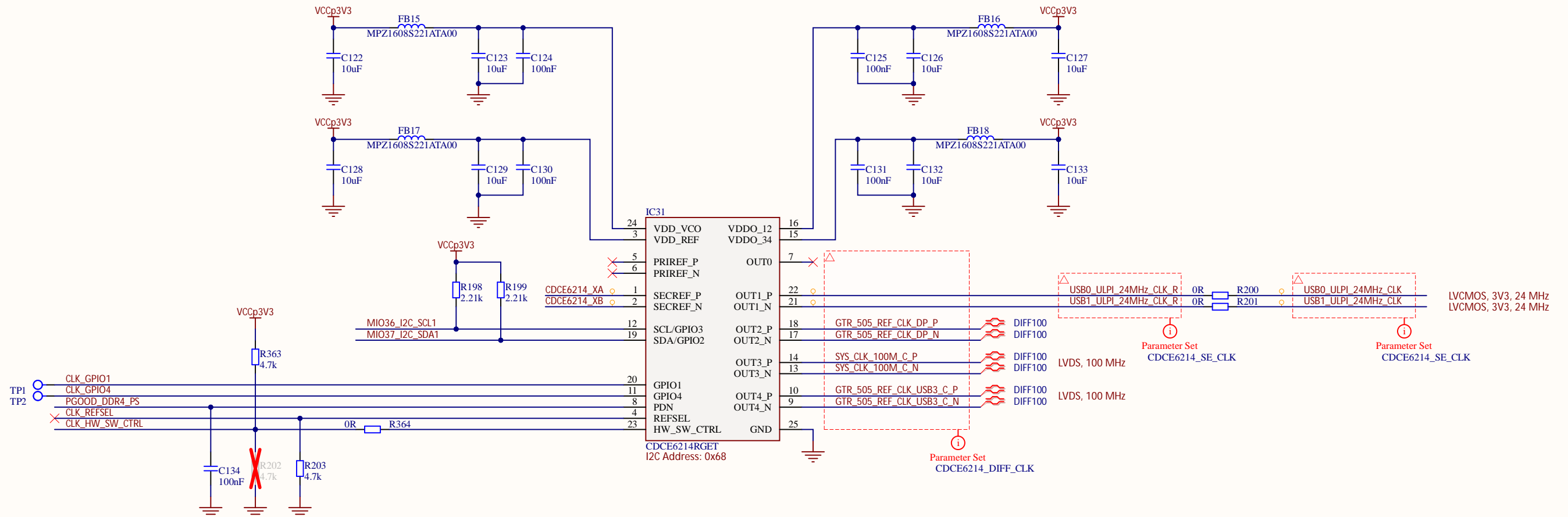
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [12] - USB 3.0 DRP II.Sch.Doc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 12 of 30	

# SD CARD



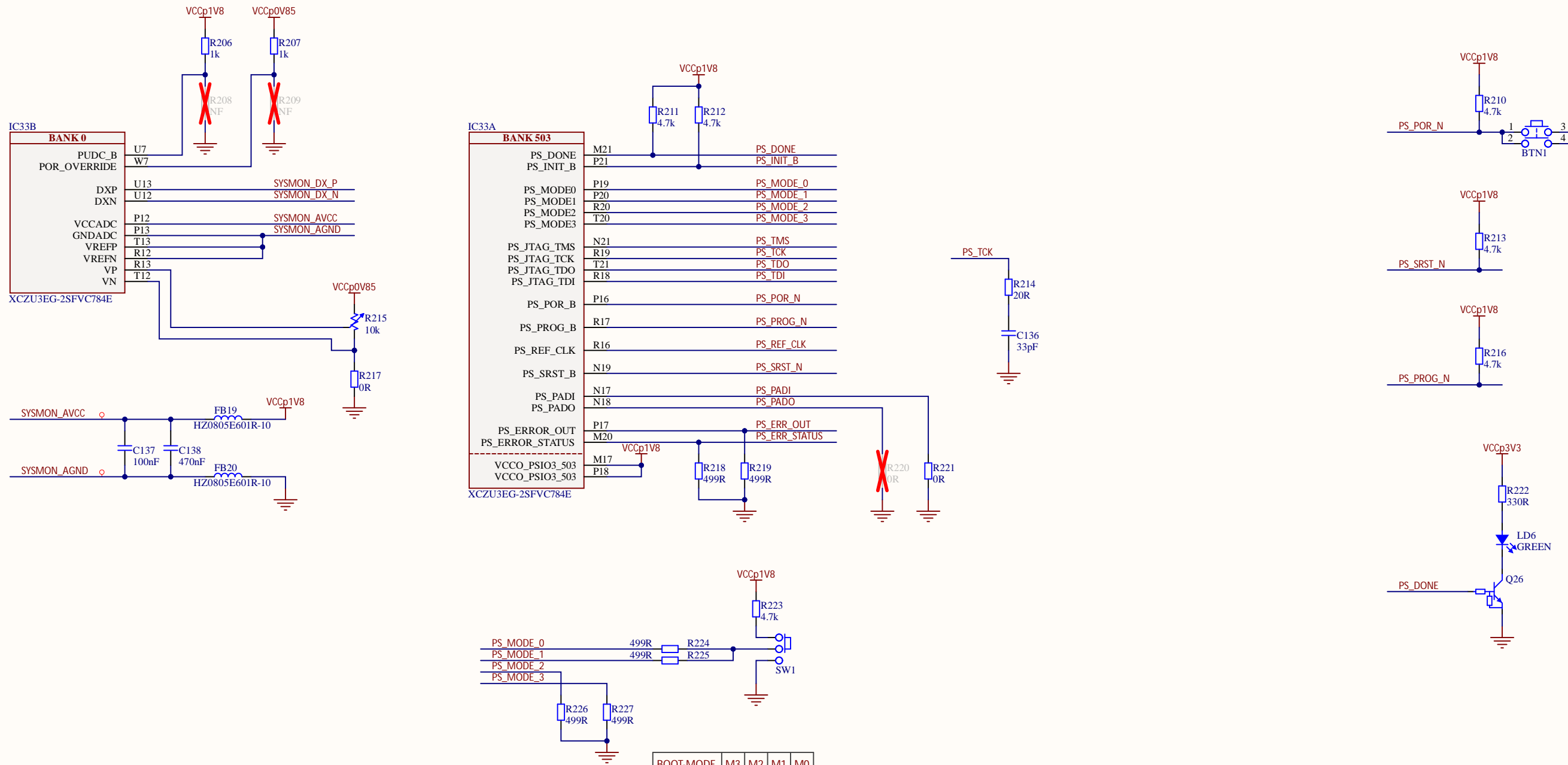
<b>REAL DIGITAL</b>		© Real Digital 2024	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [13] - SD CARD.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V4I2	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 13 of 30	

# CLOCK I:



<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [14] - CLOCK I.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 14 of 30	

# MPSoC CONFIG

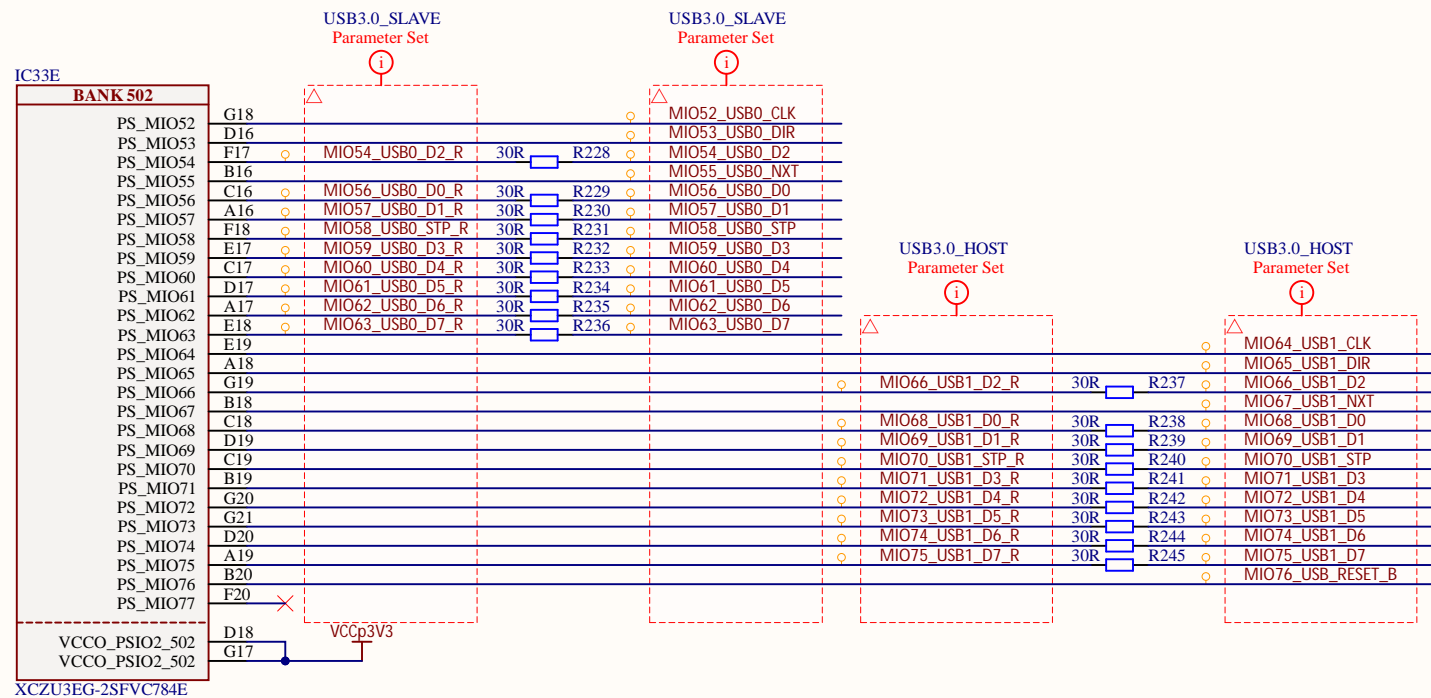
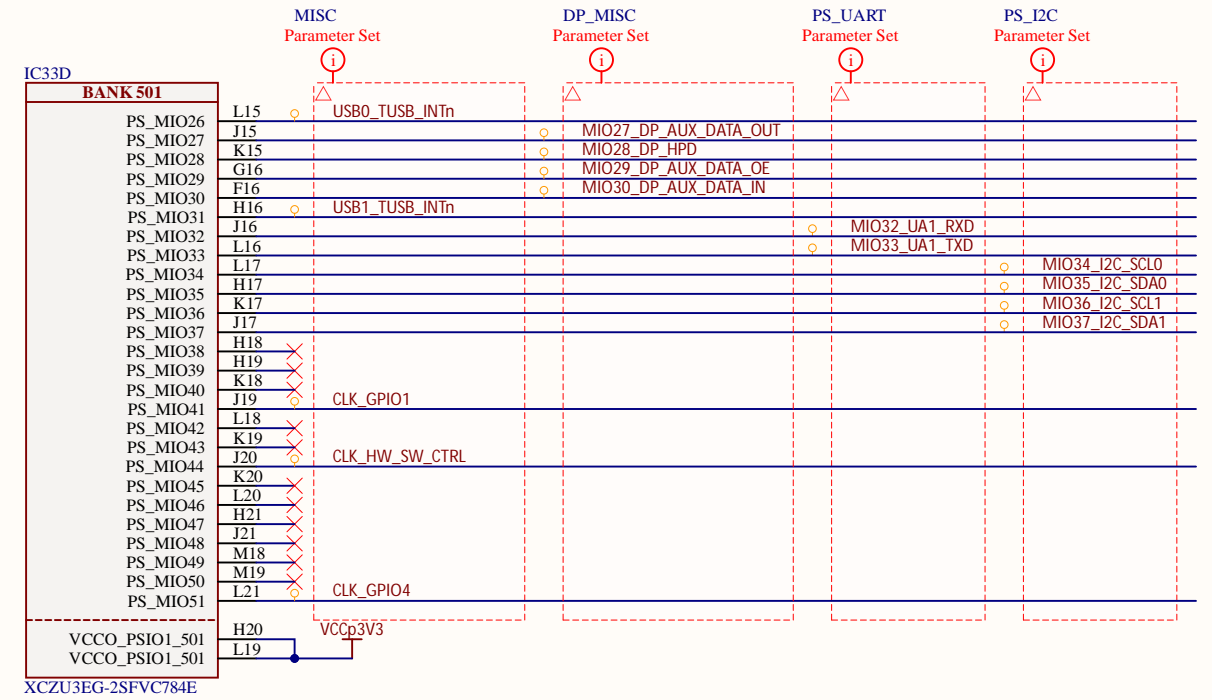
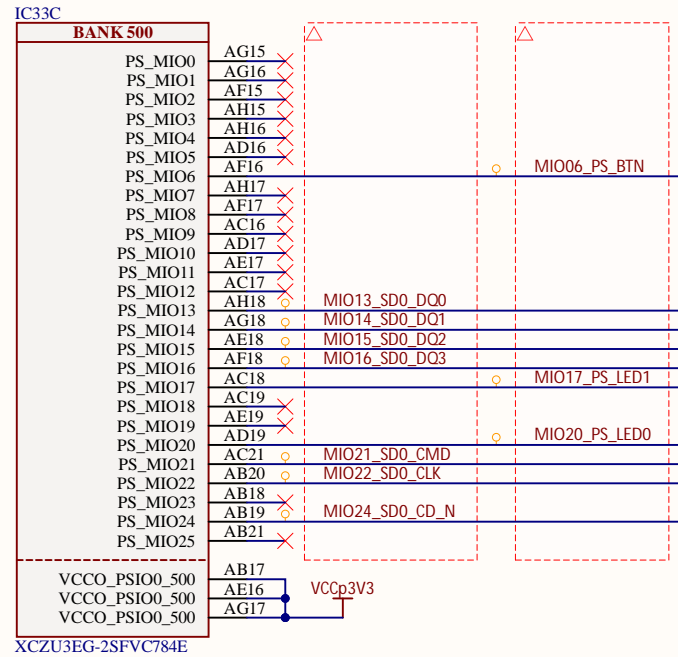


BOOT-MODE	M3	M2	M1	M0
JTAG	L	L	L	L
SD Card	L	L	H	H



<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [15] - MPSoC CONFIG.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 15 of 30	

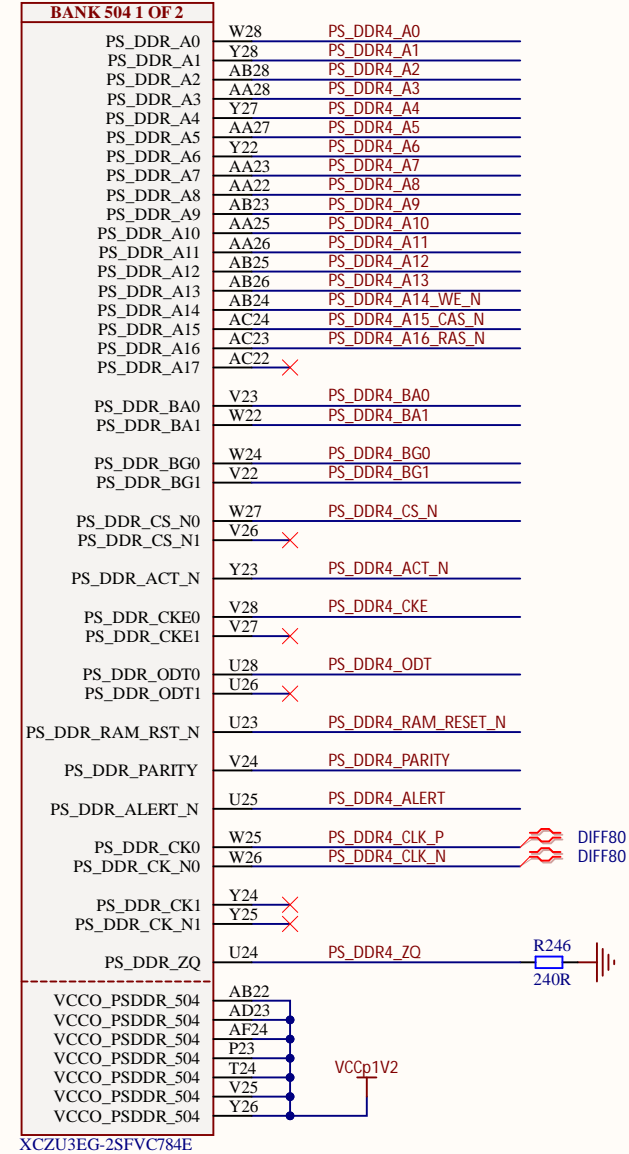
# PS: BANKS 500-502



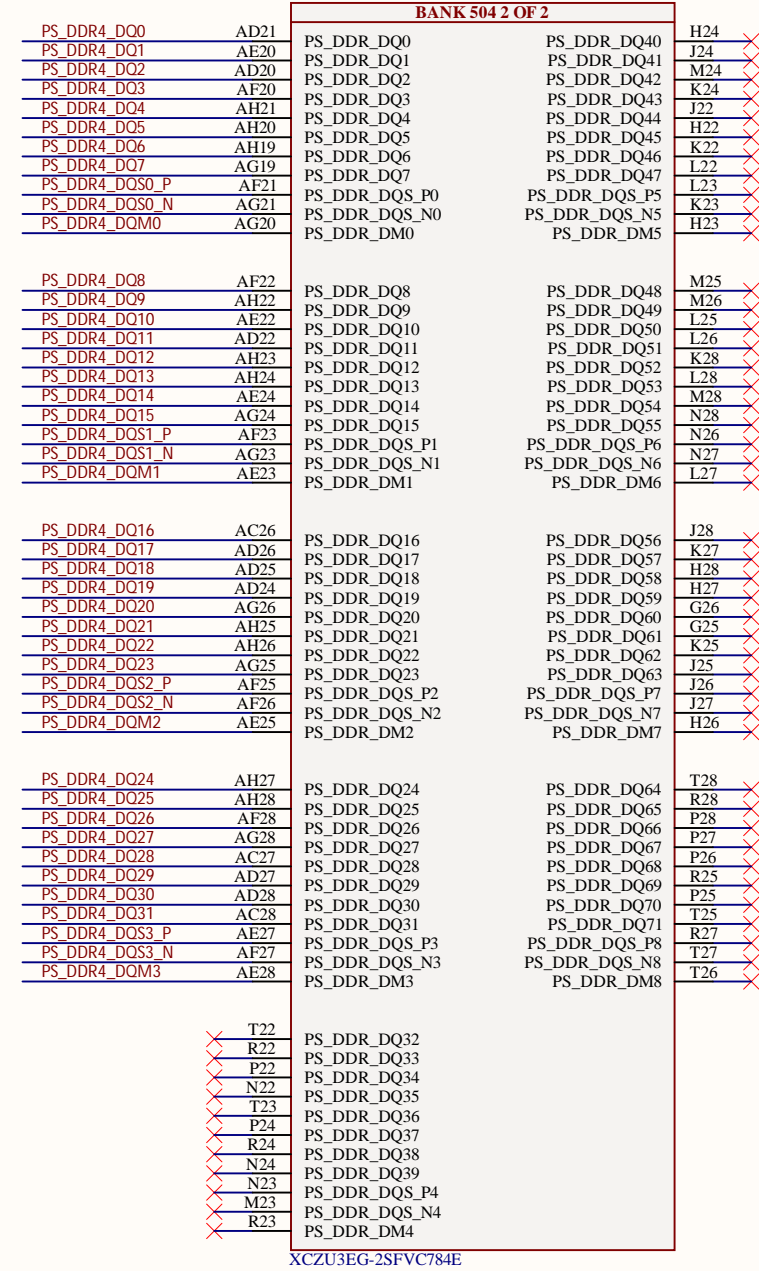
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [16] - PS BANKS 500-502.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 16 of 30	

# PS: BANK 504

IC33F

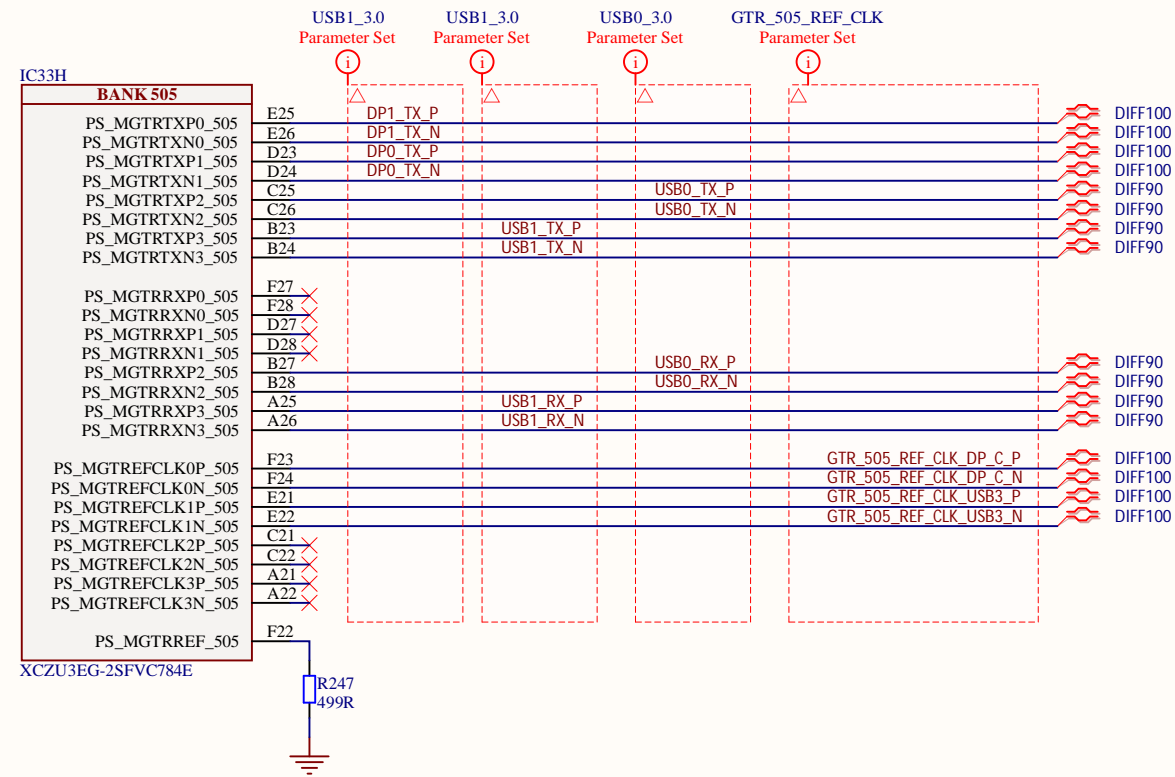


IC33G



REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [17] - PS BANK 504.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 17 of 30	

# PS: MGT

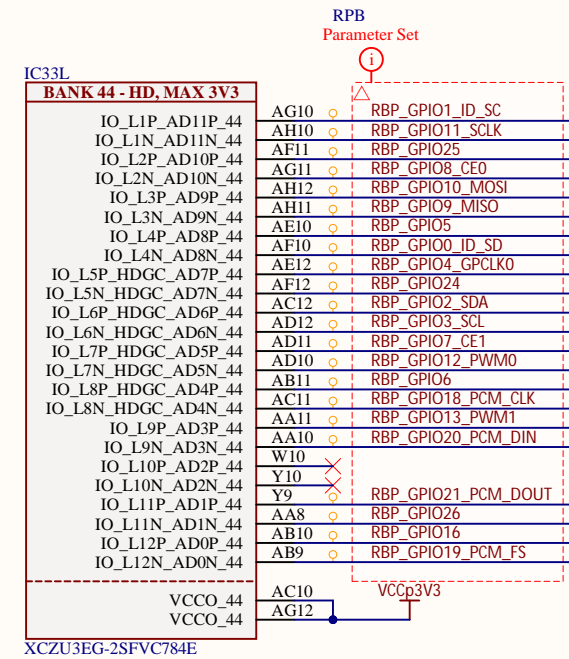
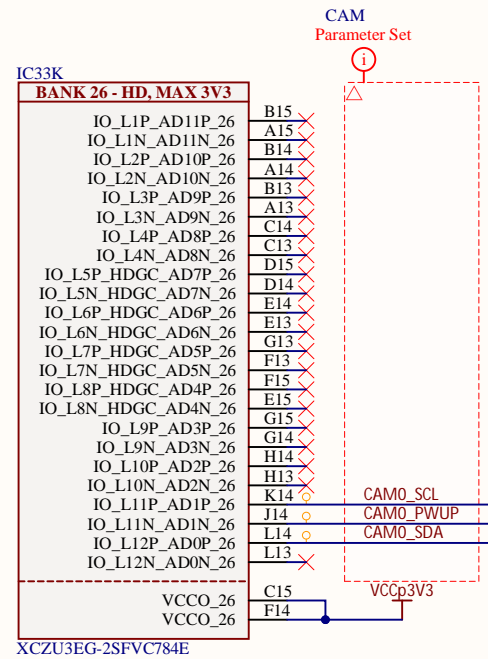
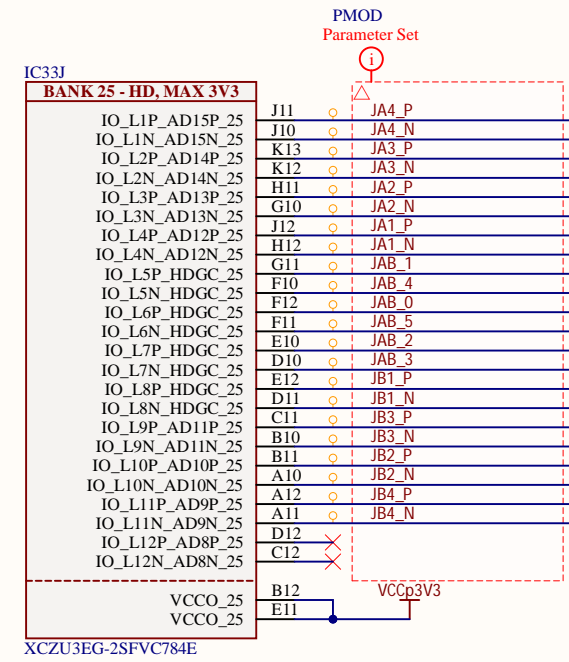
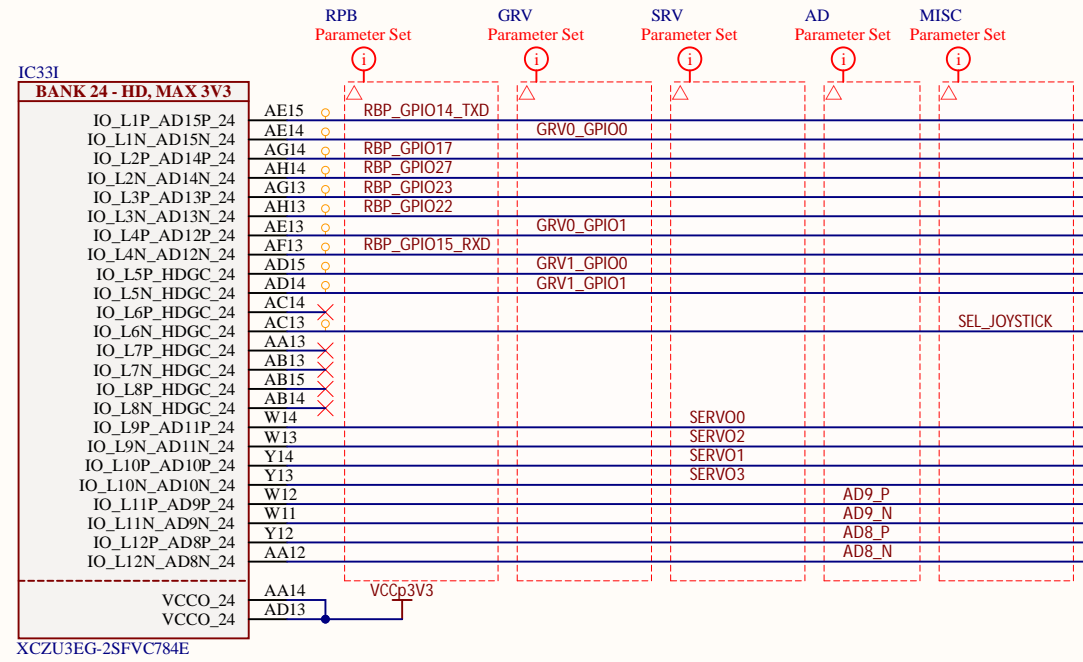


GTR_505_REF_CLK_DP_C_P	10nF	C139	GTR_505_REF_CLK_DP_P
GTR_505_REF_CLK_DP_C_N	10nF	C140	GTR_505_REF_CLK_DP_N
GTR_505_REF_CLK_USB3_C_P	10nF	C141	GTR_505_REF_CLK_USB3_P
GTR_505_REF_CLK_USB3_C_N	10nF	C142	GTR_505_REF_CLK_USB3_N



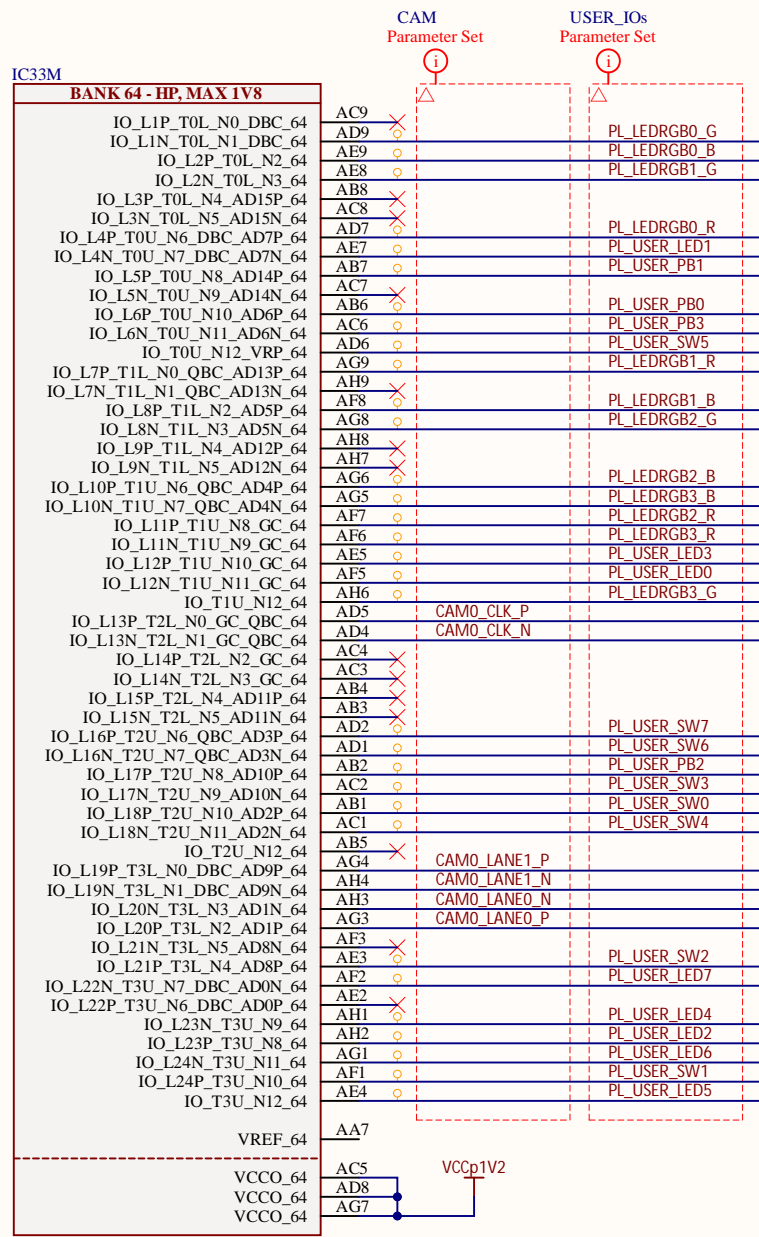
REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [18] - PS MGT.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 18 of 30	

# PL: BANKS 64-66

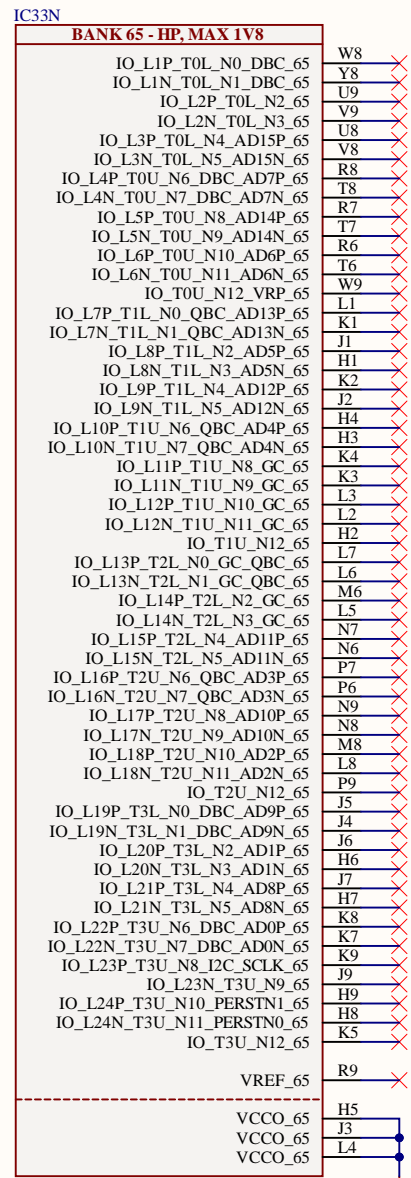


<b>REAL DIGITAL</b>	<b>© Real Digital 2024</b>		
<b>Title:</b> AUP-ZU3	<b>Variant:</b> Prototype		
<b>Page Contents:</b> [19] - PLBANKS 43-46.SchDoc			
<b>Size:</b> A3	<b>DWG NO:</b> KT-2024-0015-004-002A	<b>Revision:</b> V4I2	
<b>Date:</b> 4/28/2026	<b>Checked by:</b> *	<b>Sheet</b> 19 of 30	

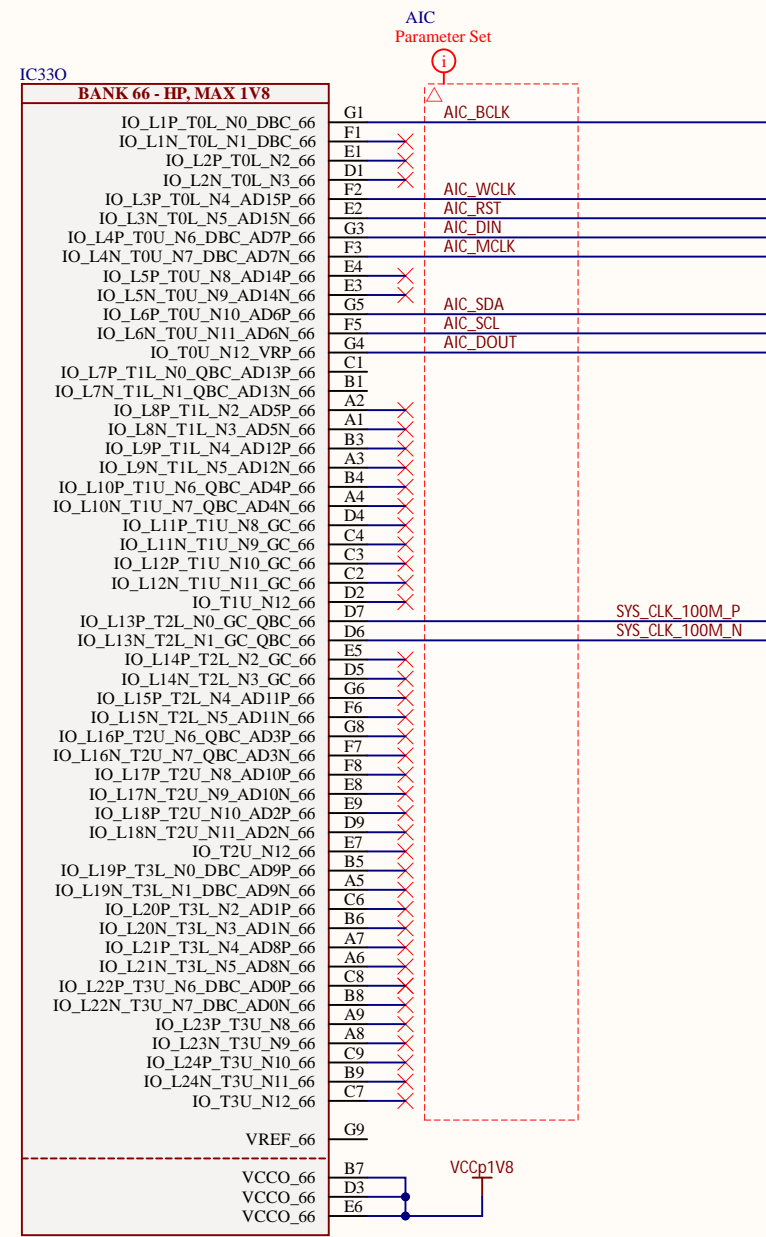
# PL: BANKS 67-69



XCZU3EG-2SFVC784E



XCZU3EG-2SFVC784E

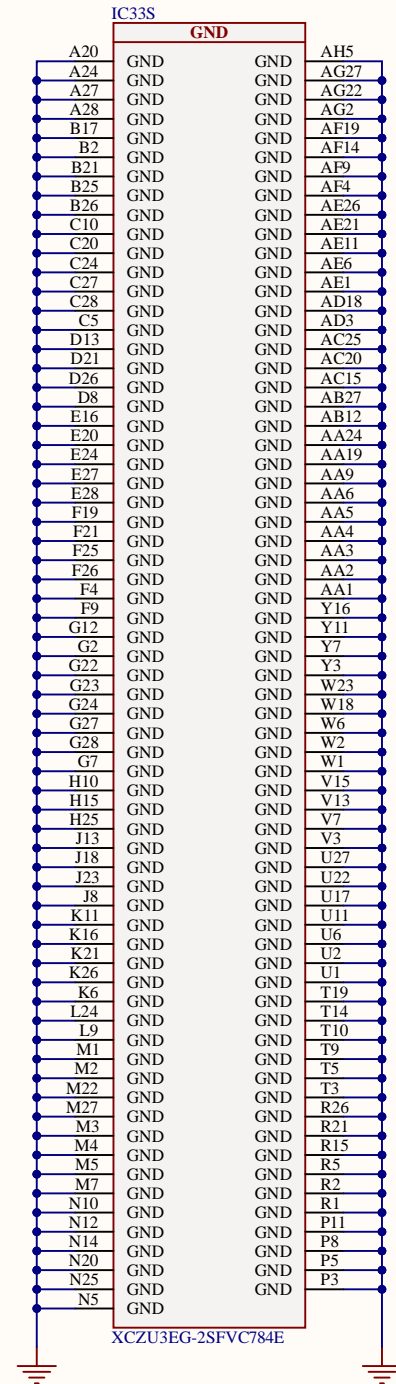
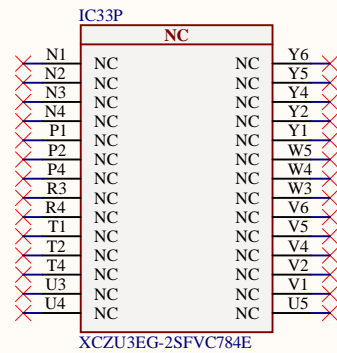
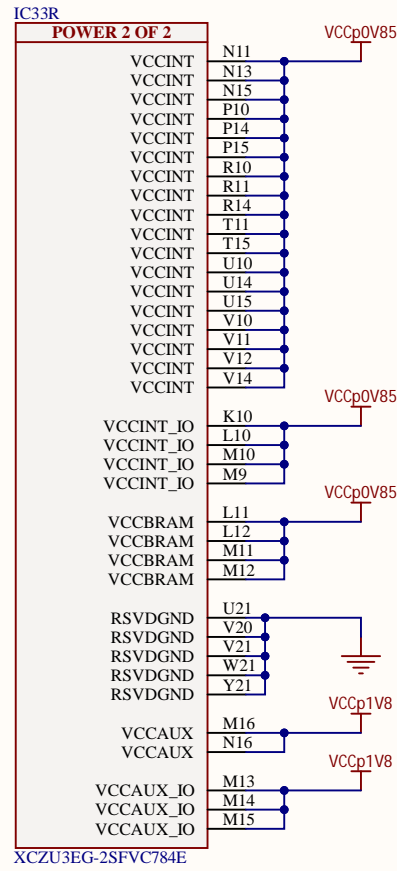
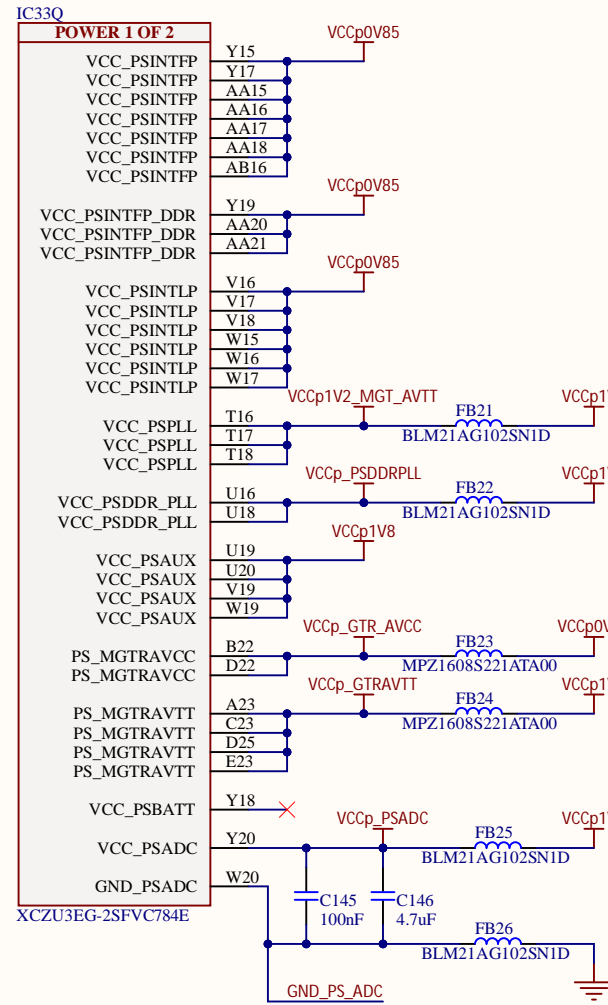


XCZU3EG-2SFVC784E



<b>REAL DIGITAL</b>	<b>© Real Digital 2024</b>		
<b>Title:</b> AUP-ZU3	<b>Variant:</b> Prototype		
<b>Page Contents:</b> [20] - PL BANKS 64-66.SchDoc			
<b>Size:</b> A3	<b>DWG NO:</b> KT-2024-0015-004-002A	<b>Revision:</b> V4I2	
<b>Date:</b> 4/28/2026	<b>Checked by:</b> *	<b>Sheet</b> 20 of 30	

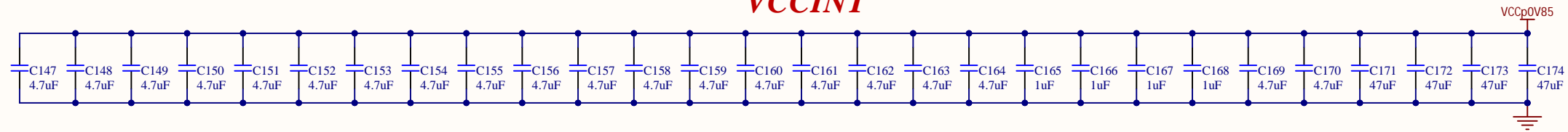
# MPSoC PWR AND GND PINS



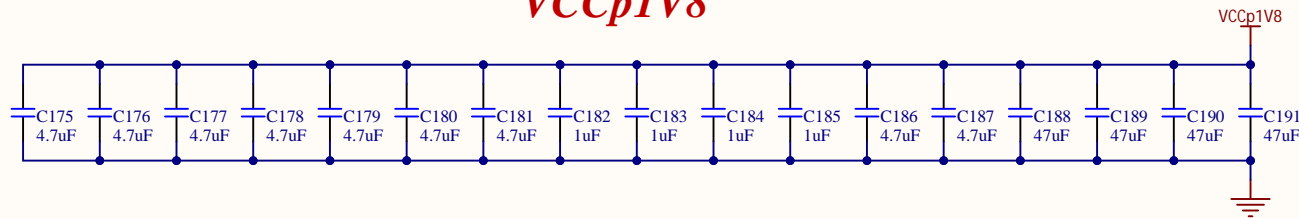
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [21] - MPSoC PWR AND GND PINS.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 21 of 30	

# DECOUPLING

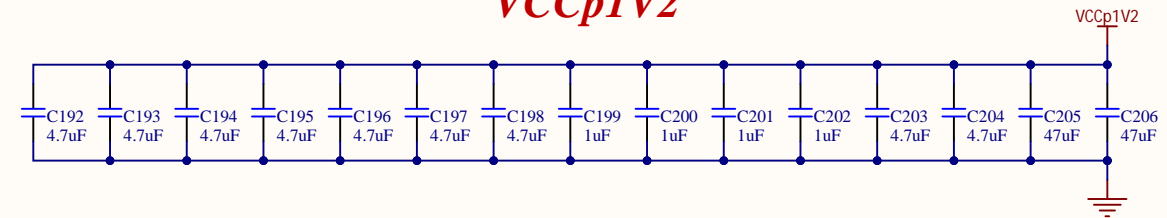
## VCCINT



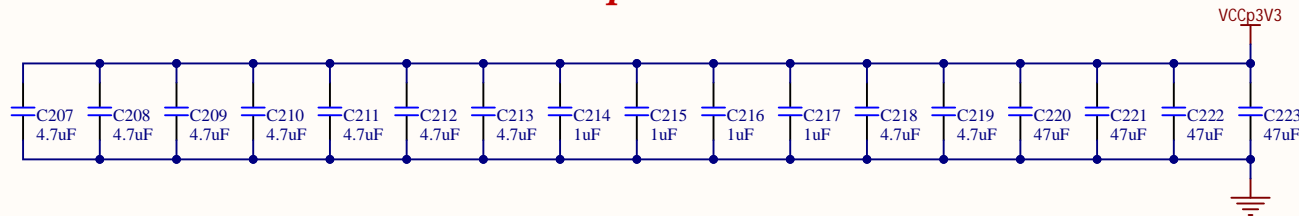
## VCCp1V8



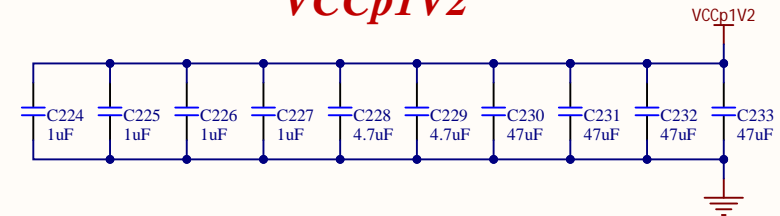
## VCCp1V2



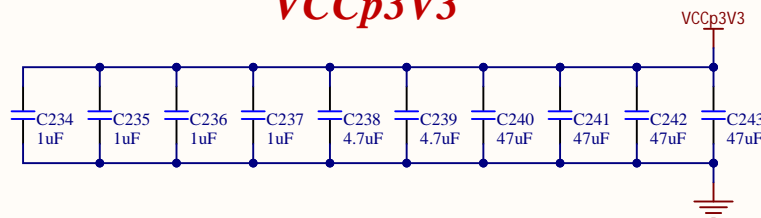
## VCCp3V3



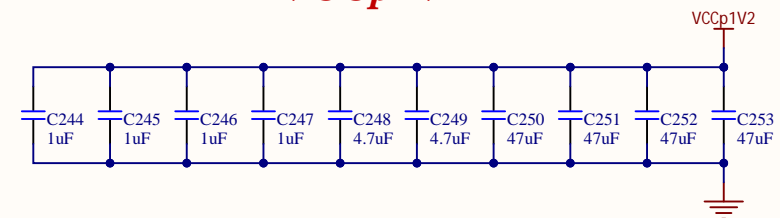
## VCCp1V2



## VCCp3V3

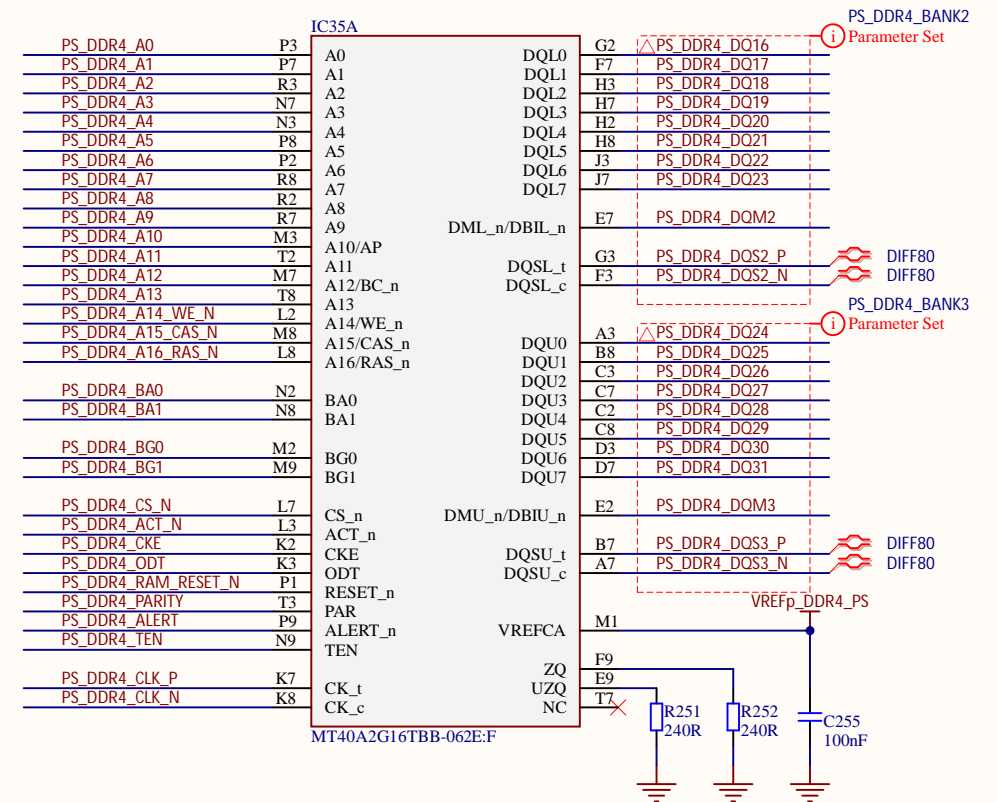
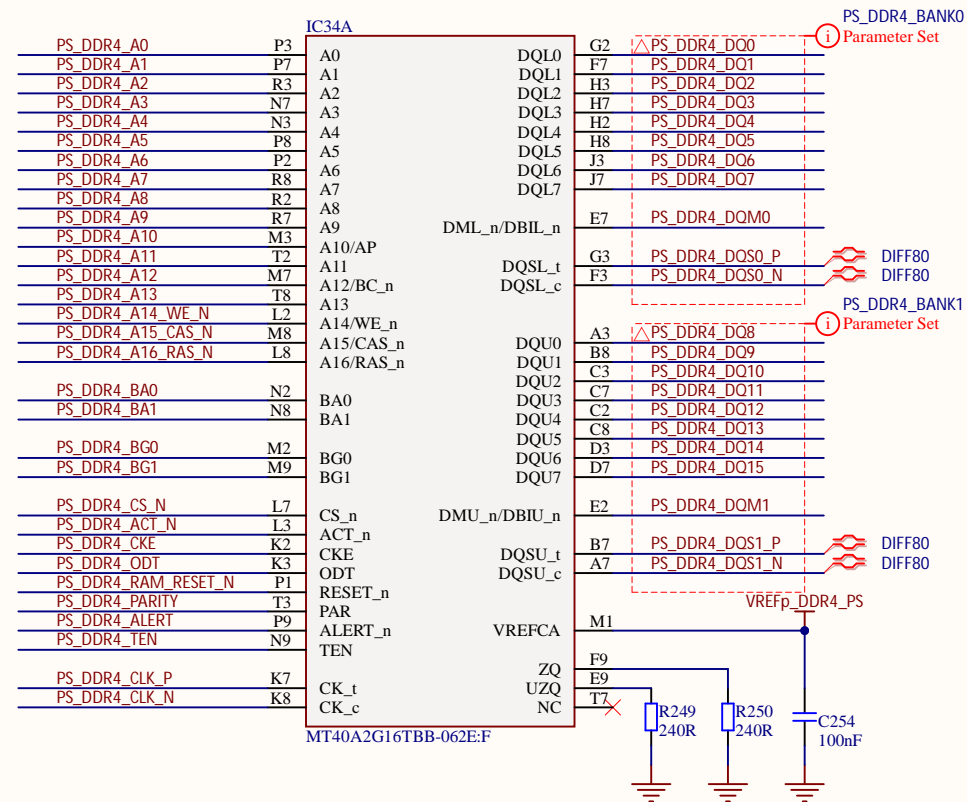


## VCCp1V2



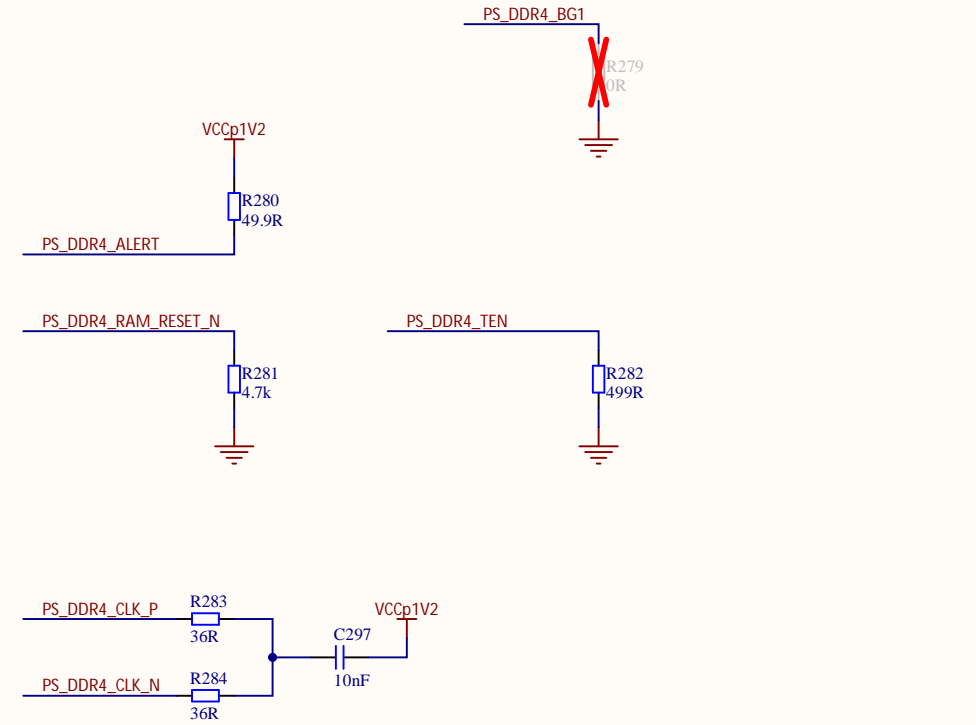
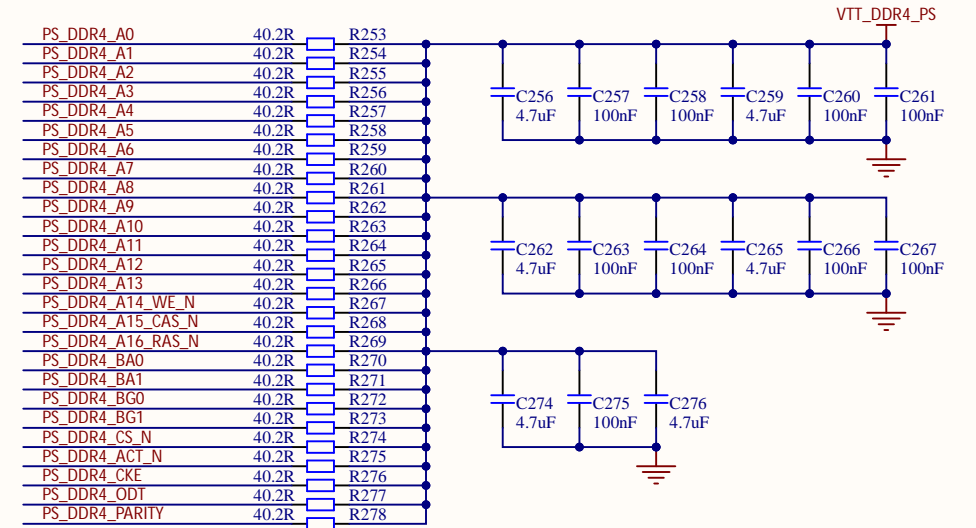
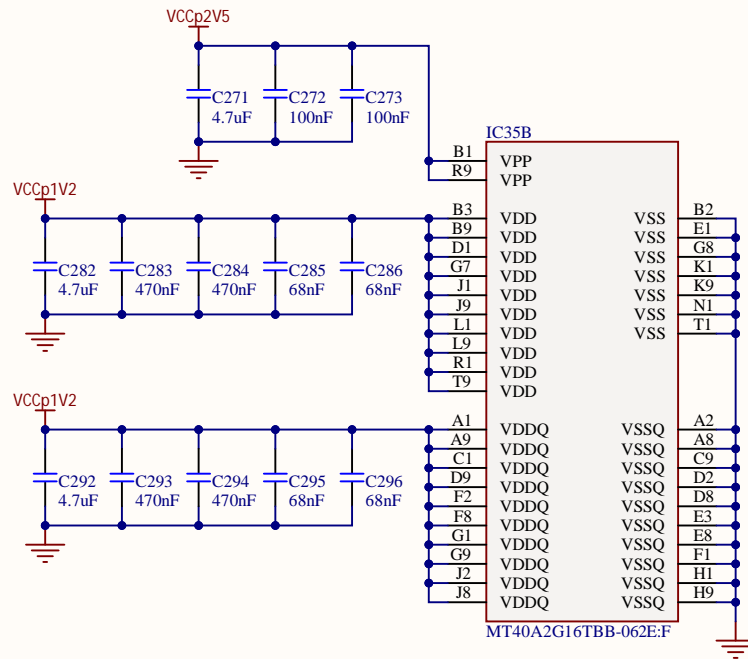
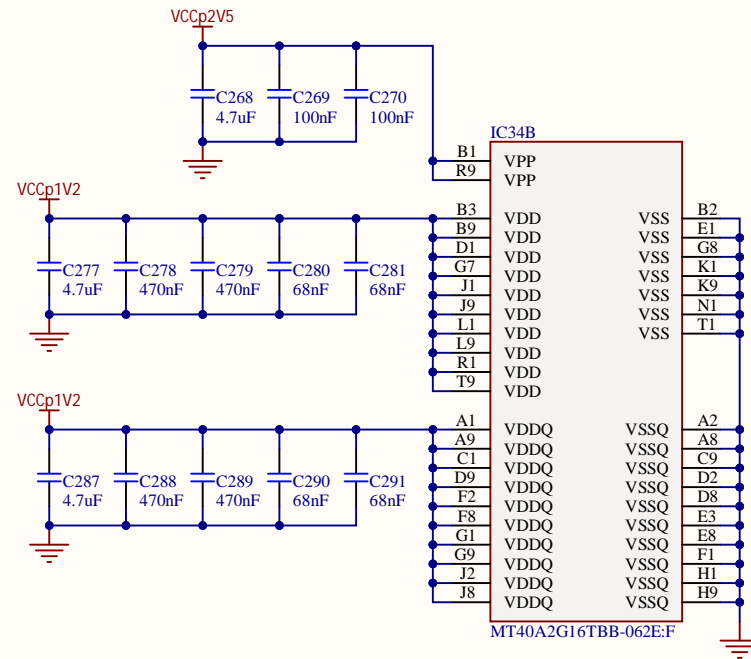
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
<i>Page Contents:</i> [22] - MPSoC DECOUPLING.SchDoc			
<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A	<i>Revision:</i> V4I2	
<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 22 <i>of</i> 30	

# DDR4 MEMORY PS I



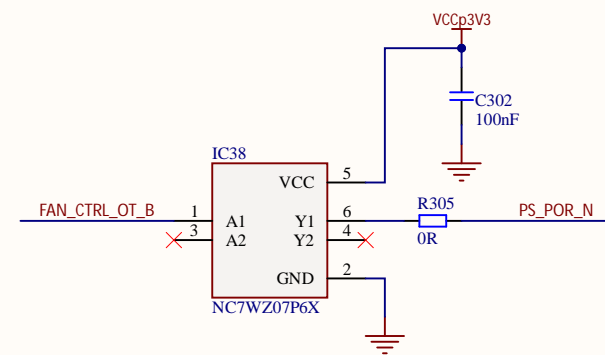
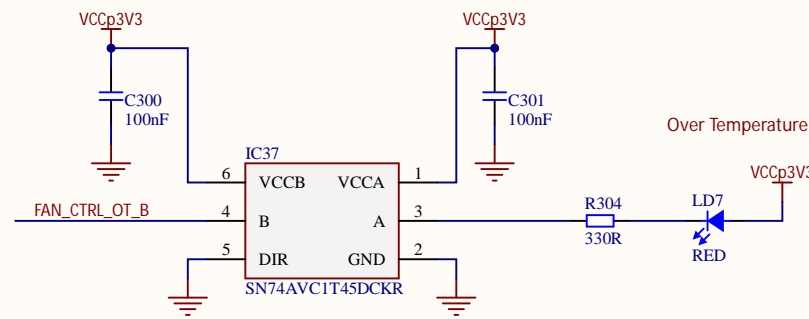
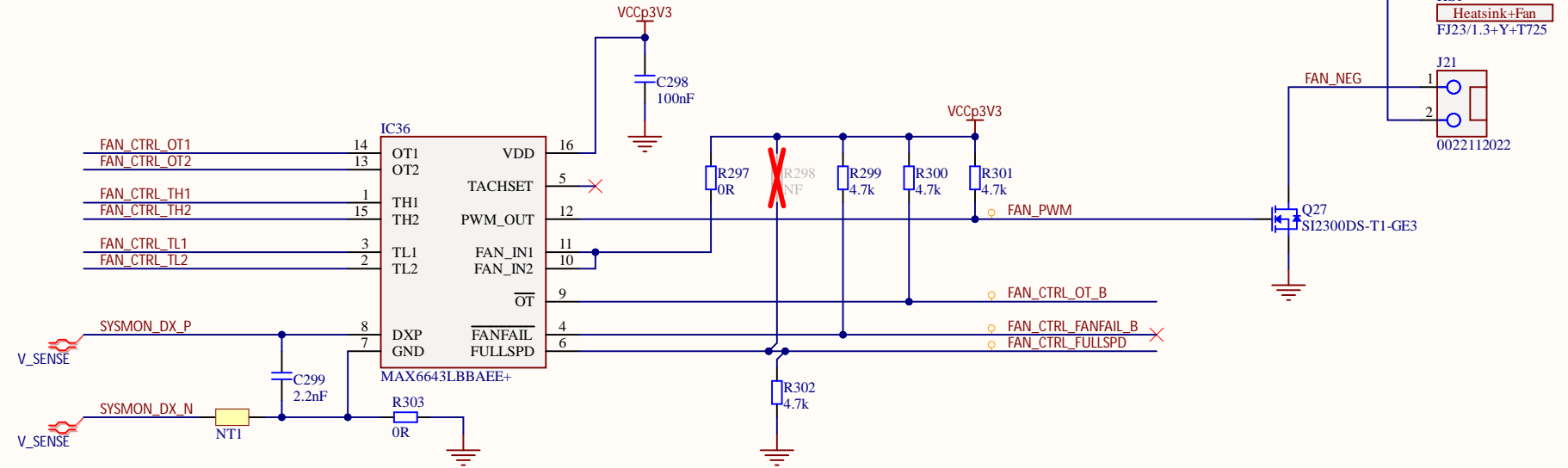
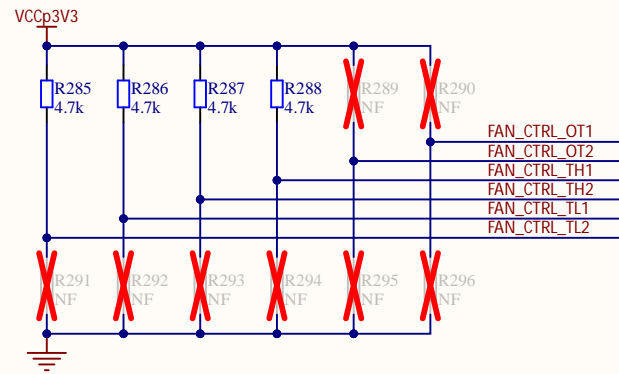
<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [23] - DDR4 MEMORY PS I.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 23 of 30	

# DDR4 MEMORY PS II



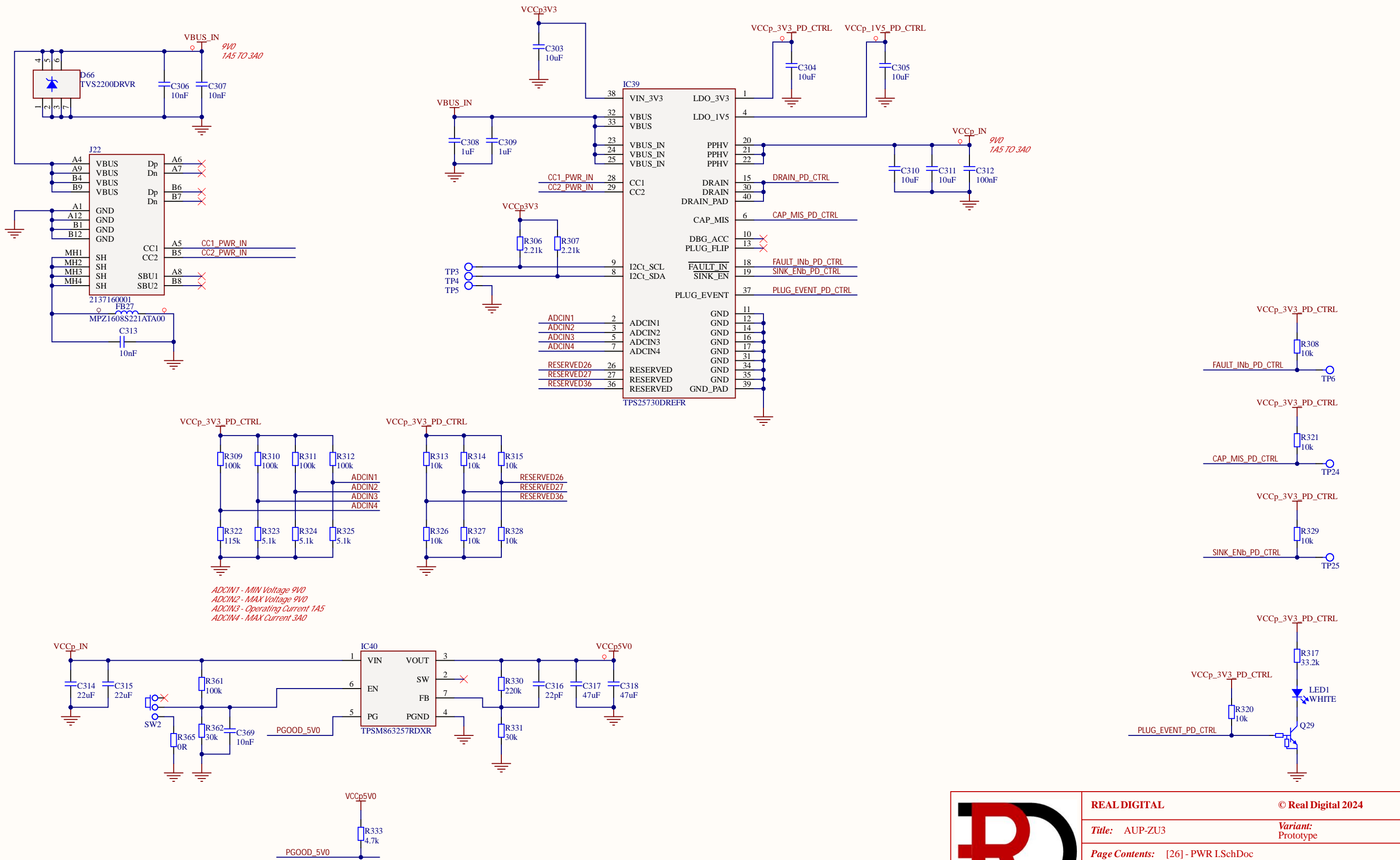
<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [24] - DDR4 MEMORY PS II.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 24 of 30	

# FAN CONTROLLER



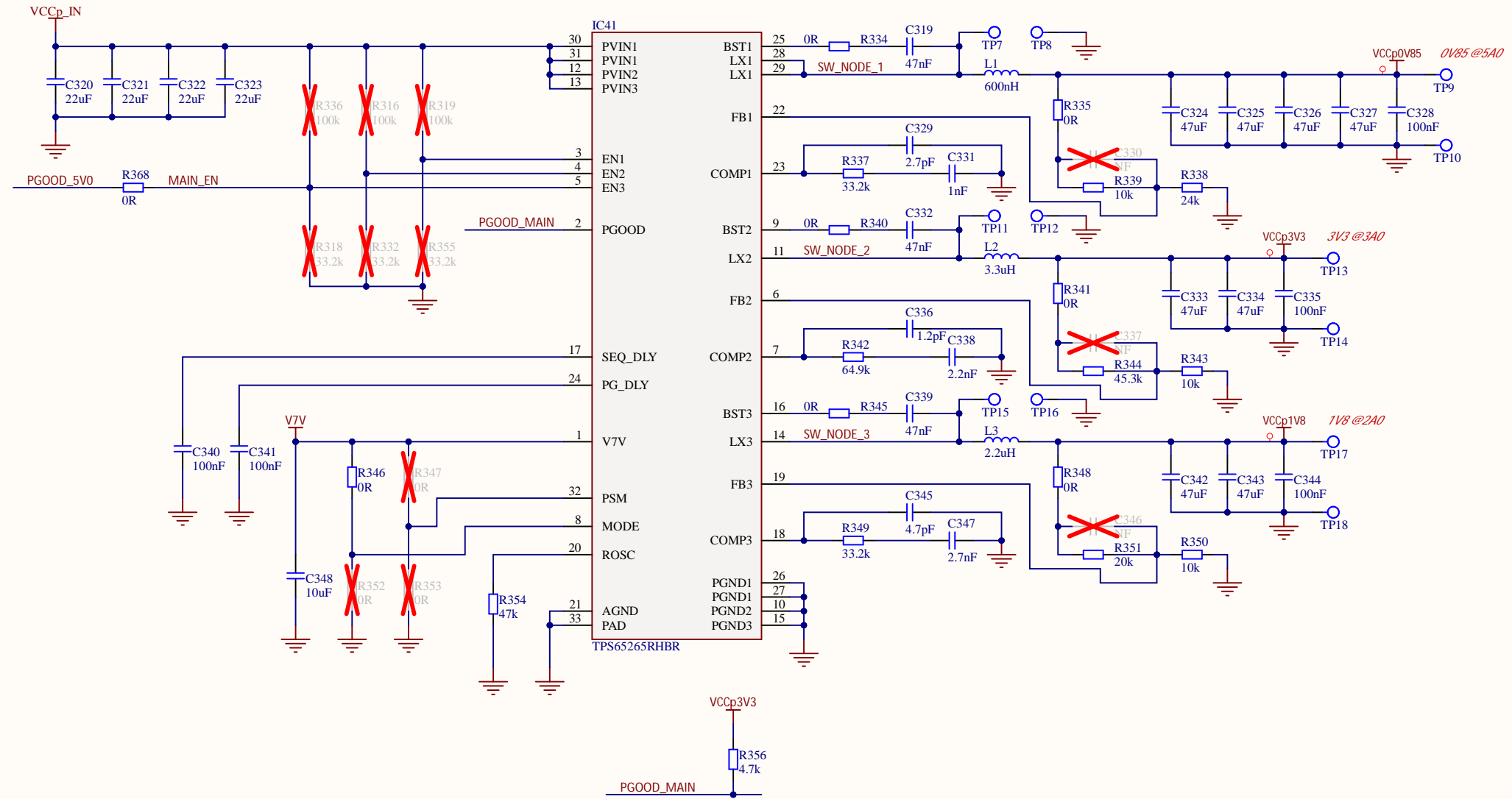
REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [25] - FAN CONTROLLER.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 25 of 30	

# POWER I



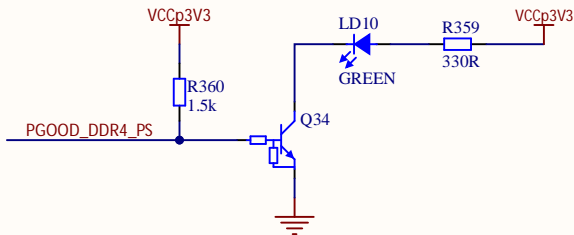
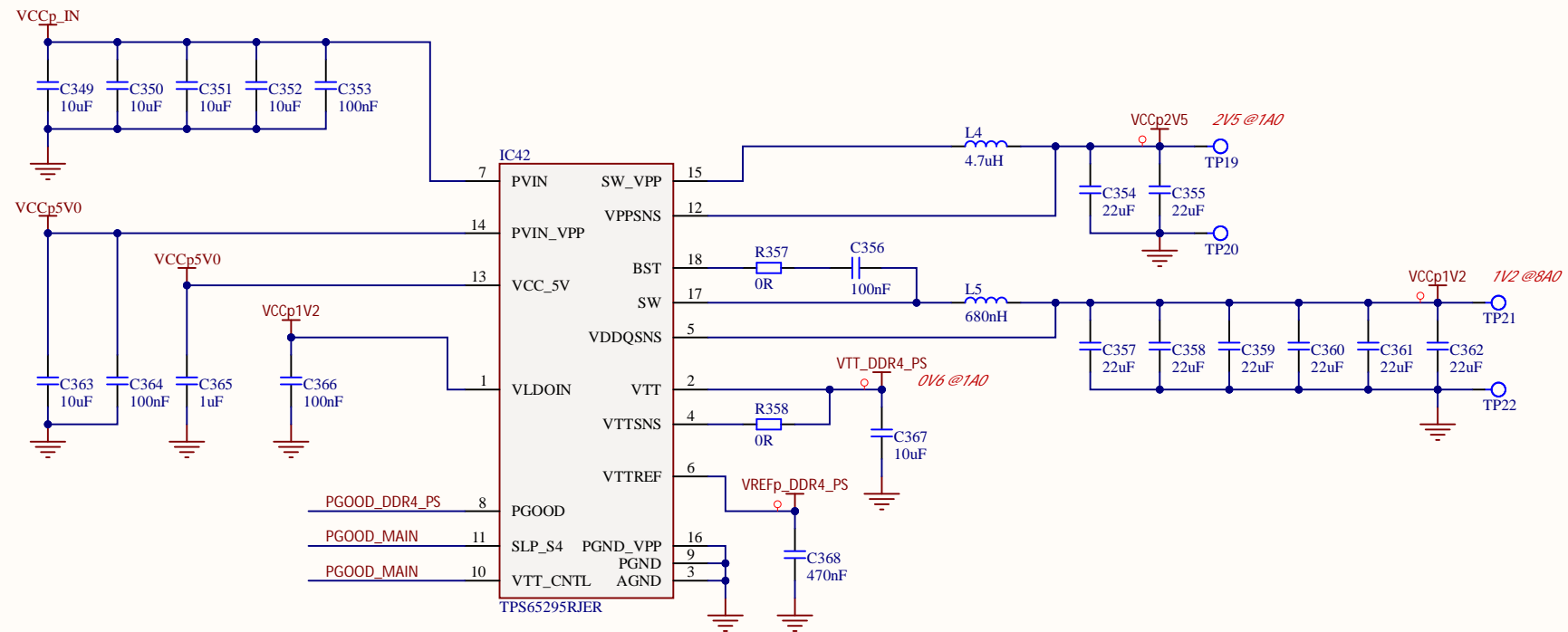
REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [26] - PWR I.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 26 of 30	

# POWER II



<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [27] - PWR II.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 27 of 30	

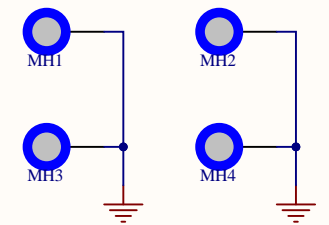
# POWER III



<b>REAL DIGITAL</b>		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [28] - PWR III.SchDoc			
Size: A3	DWG NO: KT-2024-0015-004-002A	Revision: V4I2	
Date: 4/28/2026	Checked by: *	Sheet 28 of 30	


# MECHANICAL AND POWER SEQUENCING

Real Digital  
LG1  
AMD-AUP  
LG2  
MIPI  
LG3



<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
<b>Title:</b> AUP-ZU3		<b>Variant:</b> Prototype	
<b>Page Contents:</b> [29] - MECH AND PWR SEQUENCING.SchDoc			
<b>Size:</b> A3	<b>DWG NO:</b> KT-2024-0015-004-002A	<b>Revision:</b> V4I2	
<b>Date:</b> 4/28/2026	<b>Checked by:</b> *	<b>Sheet</b> 29 <i>of</i> 30	

# DOC: REVISION HISTORY

	<b>REAL DIGITAL</b>		<b>© Real Digital 2024</b>	
	<i>Title:</i> AUP-ZU3		<i>Variant:</i> Prototype	
	<i>Page Contents:</i> [30] - DOC REVISION HISTORY.SchDoc			
	<i>Size:</i> A3	<i>DWG NO:</i> KT-2024-0015-004-002A		<i>Revision:</i> V412
	<i>Date:</i> 4/28/2026	<i>Checked by:</i> *	<i>Sheet</i> 30 <i>of</i> 30	