PROJECT 7: LATCHES AND FLIP-FLOPS

Digital Logic Project Submission Form Revision Date: Sept 28, 2018 RealDigital

I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Print Name _____ Sign Name _____ Date _____

Point Scale
4: Exemplary
3: Complete
2: Incomplete
1: Minor effort
0: Not submitted

#	Deliverable	Wt	Pts	Date	Asst. Signature
Requirements					
1: Simulate the AND Cell SR-Latch					
1	Program demo	1			
2	Verbal questions answered well	1			
2: Simulate the NOR Cell SR-Latch					
1	Program demo	2			
2	Verbal questions answered well	2			
3: Create and Simulate a D-Latch					
1	Program demo	2			
2	Verbal questions answered well	2			
4: Parallel In Parallel Out (PIPO) Shift Register					
1	Program demo	3			
2	Verbal questions answered well	3			
5: Parallel In Serial Out (PISO) Shift Register					
1	Program demo	3			
2	Verbal questions answered well	3			
6: Serial In Parallel Out (SIPO) Shift Register					
1	Program demo	4			
2	Verbal questions answered well	4			
Challenges					
1: Barrel Shifter					
1	Program demo	3			
2	Verbal questions answered well	3			
Extensions					
Describe					
1	Program demo				
2	Verbal questions answered well				
Homework Problems					
1	NAND and NOR Basic Cells	24			
2	D-Latch	10			
3	Timing Diagrams for D-Latch and DFF	12			
4	Complete Timing Diagram	12			
5	Simulate Following Sequence	16			