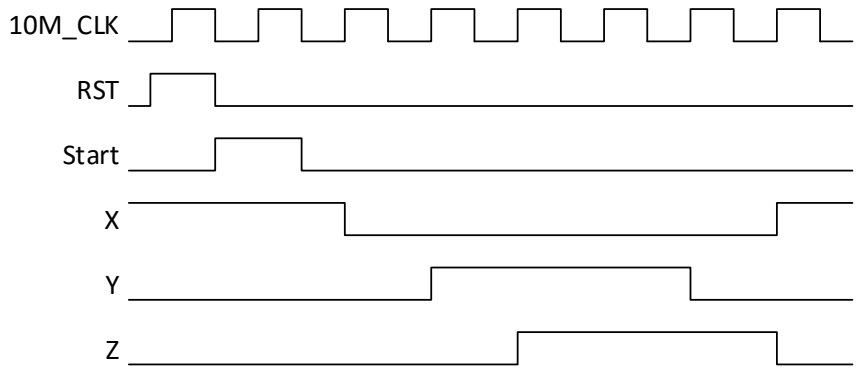
EE324 Fall 2018 Take Home Exercises **Name:_____**

1. (15 points) Design a state diagram to define a circuit that could implement the timing diagram shown. Start, RST, and CLK are inputs, and X, Y, and Z are outputs.



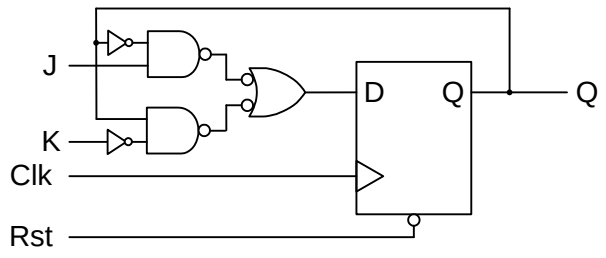
2. (20 points) An input called “GO” is asynchronous pulse generated from an electronic light meter (i.e., not from a mechanical switch). GO will be asserted once per second for a period lasting between 50ns and 500ns, and it is used to initiate the sequence of outputs in the problem above. The output sequence shown must be produced once for each GO pulse, regardless of its length. Design a state diagram for an input processing circuit that can receive the GO pulse and produce a “GO_S” signal that can be reliably used by the state machine, regardless of the length of the original GO pulse. If you use a handshake system (hint!), you must show the handshake signals (and this may require you to modify the state diagram from the problem above – if you do modify the state diagram from above, show the new one below).

3. (10 points) Sketch a block diagram, state diagram, and circuit for the Verilog code shown below. Your circuit should show a D flip-flop together with any other needed logic circuits.

```
module FSM (
   input clk, rst, T
   output Q);

reg Q;

always @ (posedge(clk), posedge(rst))
begin
    if (rst) Q <= 0;
    else Q = Q^T;
end

endmodule
```

4. (4 points) How would you modify the code above to create a synchronous reset?

5. (8 points) Sketch a state diagram for the circuit below.



6. (25 points) Design a state diagram for a circuit that will be used facilitate a psychological experiment. An operator will press an “Image” button to allow the test subject to see an image. The test subject will have two seconds to press an Approve or Disapprove button in response to the image at which point either a Green LED or Red LED will illuminate for two seconds, respectively (Green for approve, Red for disapprove). The circuit should do nothing until receiving an “Image” input from the operator. When this input is received, your state machine must assert a “Timer On” signal for at least 100ns to start a two second timer (the Timer On signal will reset an external timer and start a new two-second interval, regardless of the current state of the timer). The timer will return a 100ns “TC” signal at the end of two seconds. If the subject has pressed the Approve button at any time during the two-second interval, illuminate a Green LED for two seconds. If the subject presses the Disapprove button, illuminate a Red LED for two seconds. If the subject presses neither button by the time the TC signal is received, return to the initial state. You have a 10MHz system clock (i.e., a 100ns period clock).

   Sketch both a Moore Model (12 pnts) and a Mealy model (16 pnts) state diagram. Provide state codes, and ensure the sum and exclusion rules are obeyed.

7. (10 points) A signal wire from the circuit block shown on the right sends out a continuous stream of data bits, with a new bit being produced each falling edge of CLK. Sketch a state diagram for a circuit that can output a “good” signal whenever the sequence 10011 is detected (note sequences can overlap), and an “alert” signal whenever the sequence “100” is detected. Be sure to add state codes to your diagram.