PROJECT 5: STRUCTURAL VERILOG FOR COMBINATIONAL SYSTEMS

Digital Logic Project Submission Form Revision Date: Sept 28, 2018 RealDigital

I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Print Name _____ Sign Name _____ Date _____

Point Scale
4: Exemplary
3: Complete
2: Incomplete
1: Minor effort
0: Not submitted

#	Deliverable	Wt	Pts	Date	Asst. Signature
Requirements					
1: Mux and Demux Circuit					
1	Program demo	2			
2	Verbal questions answered well	2			
2: Design and Implement Single Digit Seven-Segment Display Decoder					
1	Program demo	3			
2	Verbal questions answered well	3			
3: Design and Implement Two-Digit Seven-Segment Display Decoder Using a Button					
1	Program demo	4			
2	Verbal questions answered well	4			
Challenges					
1: Design and Implement Two-Digit Seven-Segment Display Decoder Using a Counter					
1	Program demo	2			
2	Verbal questions answered well	2			
Extensions					
Describe					
1	Program demo				
2	Verbal questions answered well				
Homework Problems					
1	N/A	N/A	N/A	N/A	N/A