Digital Logic Problem Set #7

Revision: August 5, 2025

RealDigital
www.realdigital.org

1. (24 points) Sketch circuits for the NAND and NOR basic cells, and label the S and R inputs and Q output. (Be sure the output Q comes from the proper gate – either the gate driven by Set or the gate driven by Reset – it will only work properly if Q comes from the proper gate). Then sketch their respective block diagrams (being sure to show bubbles on inputs that are asserted low), and complete the truth tables to document their operation.

NAND Basic Cell Circuit

NAND Cell Block Diagram

S	R	Q
0	0	
0	1	
1	0	
1	1	

NAND Cell Truth Table

NOR Basic Cell Circuit

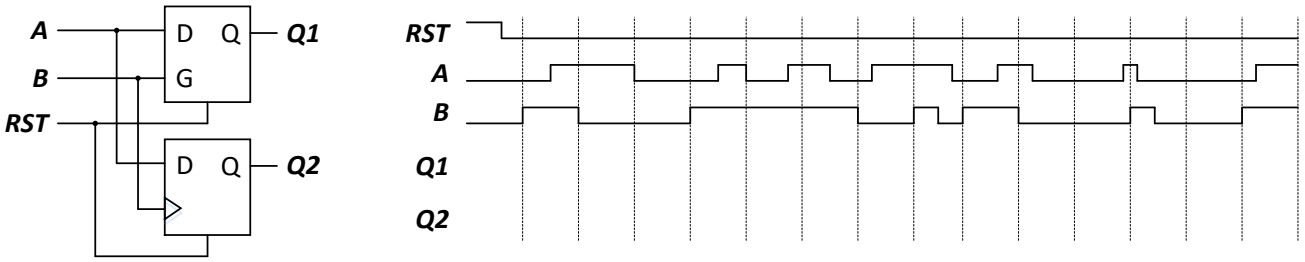
NOR Cell Block Diagram

S	R	Q
0	0	
0	1	
1	0	
1	1	

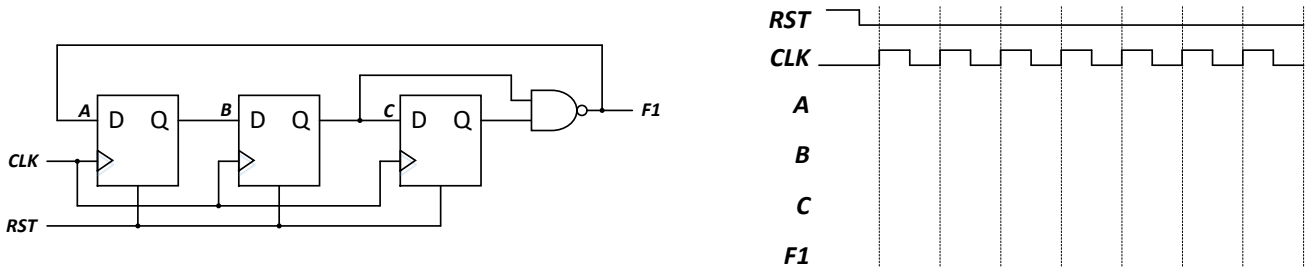
NOR Cell Truth Table

2. (10 points) Sketch the circuit for a D latch based on a NAND basic cell, and then sketch a timing diagram to illustrate its function. Be sure to illustrate all the important states in your timing diagram (hint: there are four).

3. (12 points) Complete the timing diagrams to document the behavior of a D-latch and a D-flip-flop.

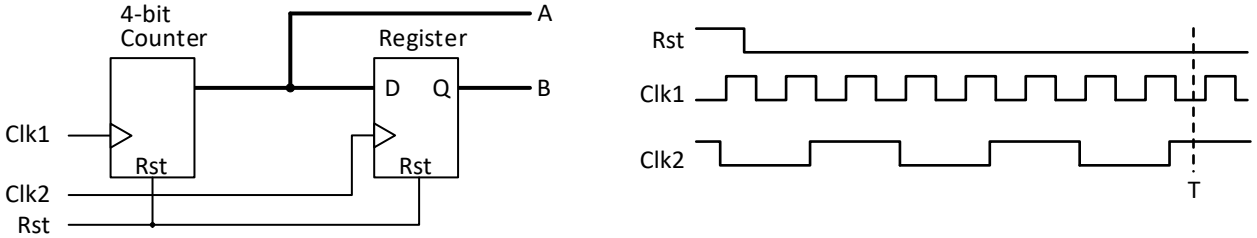


4. (12 points) Complete the timing diagram to show the time course for circuit nodes A, B, C, and F1.



5. (4 points) In the figure below, what are the values at time T for the counter output (A) and the register output (B)?

A _____ B_____



6. (8 points) The four-bit register shown could be used as what type of register? Circle all that apply.

PIPO PISO SIPO SISO