

# 6 Digital Logic Circuit delays and glitches

Submission form revision December 30, 2025

I am submitting my own work, and I accept penalties will be assessed against me if I submit work that isn't mine.

**Point Scale**  
4: Exemplary  
3: Complete  
2: Incomplete  
1: Minor effort  
0: Not submitted

Print Name \_\_\_\_\_ Sign Name \_\_\_\_\_ Date \_\_\_\_\_ Asst. Signature \_\_\_\_\_

<b>Requirements</b>		<b>Pts</b>	<b>x Wt =</b>	<b>Score</b>
1. Simulate a glitch		x	2 =	
2. Change OR gate delay		x	2 =	
3. Change all gate delays		x	2 =	
4. Homework problems		x	2 =	
Total Score (add all rows)				
Leave blank for on-time submission, or: Enter <b>+3</b> if one or more weeks early; Enter <b>-6</b> if one or two weeks late; Enter <b>X</b> if two or more weeks late				
Requirements Possible Score	<b>32</b>	Add the two rows above for the Requirements Earned Score Enter <b>0</b> if more than two weeks late		
<b>Challenges</b>		<b>Pts</b>	<b>x Wt =</b>	<b>Score</b>
1. Decoder delay		x	3 =	
Total Score (add all rows)				
Leave blank for on-time submission, or: Enter <b>+2</b> if one or more weeks early; Enter <b>-4</b> if one or two weeks late; Enter <b>X</b> if two or more weeks late				
Challenges Possible Score	<b>12</b>	Add the two rows above for the Challenges Earned Score, or Leave blank if no challenges submitted, or Enter <b>0</b> if more than two weeks late		