PROJECT 5: STRUCTURAL VERILOG

Digital Logic Project Submission Form

RealDigital

Revision: 2/3/19

I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Print Name _____ Sign Name _____ Date _____

Point Scale
4: Exemplary
3: Complete
2: Incomplete
1: Minor effort
0: Not submitted

#	Deliverable	Wt	Pts	Date	Asst. Signature
Requirements					
1: Mux and Demux Circuit					
	Program demo	2			
	Verbal questions answered well	2			
2: Design and Implement Single Digit Seven-Segment Display Decoder					
	Program demo	3			
	Verbal questions answered well	3			
3: Design and Implement Two-Digit Seven-Segment Display Decoder Using a Button					
	Program demo	4			
	Verbal questions answered well	4			
Challenges					
1: Design and Implement Two-Digit Seven-Segment Display Decoder Using a Counter					
	Program demo	3			
	Verbal questions answered well	3			
Extensions					
1: Describe					
	Program demo				
	Verbal questions answered well				
Homework Problems					
1	Verilog for multiplexor	8			
2	Verilog from minterm equation	8			
3	Verilog from circuit	8			
4	Verilog for decoder	10			
5	Verilog for shifter	15			