PROJECT 11: STOPWATCH

Digital Logic Project Submission Form Revision Date: Sept 28, 2018 RealDigital

I am submitting my own work, and I accept that penalties will be assessed against me if I submit work that isn't mine.

Print Name _____ Sign Name _____ Date _____

Point Scale
4: Exemplary
3: Complete
2: Incomplete
1: Minor effort
0: Not submitted

#	Deliverable	Wt	Pts	Date	Asst. Signature
Requirements					
1: Simulate the Serial Adder and Prove its Correctness					
1	Program demo	1			
2	Verbal questions answered well	1			
2: Stopwatch with Start, Stop, Increment, and Clear Functionality					
1	Program demo	4			
2	Verbal questions answered well	4			
3: State Diagram of the Stopwatch Controller					
1	Program demo	1			
2	Verbal questions answered well	1			
Challenges					
1: Add Timer Feature to Your Stopwatch					
1	Program demo	2			
2	Verbal questions answered well	2			
Extensions					
Describe					
1	Program demo				
2	Verbal questions answered well				
Homework Problems					
1	Modify State Diagrams	10			
2	Fill in Blanks	4			
3	Vending Machine	15			
4	Keypad	15			
5	Sketch Circuit for State Machines	25			
6	Timing Diagram	16			
7	State Diagram based on Verilog Code	25			
8	State Codes	16			